Libraries Guide

Printed in U.S.A.

About This Manual

The Libraries Guide is part of the Alliance Series and Foundation Series online documentation collection.

Manual Contents

This manual contains the following chapters.

- Chapter 1,"Xilinx Unified Libraries"
- Chapter 2,"Selection Guide"
- Chapter 3,"ACC1 to BUFT, 4, 8, 16"
- Chapter 4, "CAPTURE_SPARTAN2 to DECODE32, 64"
- Chapter 5, "FD to FTSRLE"
- Chapter 6, "GND to KEEPER"
- Chapter 7, "LD to NOR12, 16"
- Chapter 8, "OBUF, 4, 8, 16 to ORCY"
- Chapter 9, "PPC405 to ROM256X1"
- Chapter 10, "SOP3-4 to XORCY_L"
- Chapter 11, "X74_42 to X74_521"

Chapter 1,"Xilinx Unified Libraries" discusses the unified libraries, applicable device architectures for each library, contents of the other chapters, general naming conventions, and performance issues.

Chapter 2,"Selection Guide" describes then lists design elements by function that are explained in detail in the "Design Elements" chapters.

Chapters 3 through 11, "Design Elements," provide a graphic symbol, functional description, primitive versus macro table, truth table (when applicable), topology (when applicable), and schematics for macros of the design elements.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this Web site. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging `http://support.xilinx.com/support/techsup/tutorials/index.htm`
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at `http://support.xilinx.com/support/searchtd.htm`
Application Notes	Descriptions of device-specific design techniques and approaches `http://support.xilinx.com/apps/appsweb.htm`
Data Book	Pages from *The Programmable Logic Data Book*, which contain device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging `http://support.xilinx.com/partinfo/databook.htm`
Xcell Journals	Quarterly journals for Xilinx programmable logic users `http://support.xilinx.com/xcell/xcell.htm`
Technical Tips	Latest news, design tips, and patch information for the Xilinx design environment `http://support.xilinx.com/support/techsup/journals/index.htm`

Conventions

This manual uses the following conventions. An example illustrates each convention.

Typographical

The following conventions are used for all documents.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: - 100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement. However, braces "{ }" in Courier bold are not literal and square brackets "[ ]" in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

  `rpt_del_net=`

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *design_name*

  - References to other manuals

    See the *Development System Reference Guide* for more information.

  - Emphasis in text

    If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  `edif2ngd` *[option_name] design_name*

- Braces "{ }" enclose a list of items from which you must choose one or more.

  `lowpwr ={on|off}`

- A vertical bar " | " separates items in a list of choices.

  `lowpwr ={on|off}`

- A vertical ellipsis indicates repetitive material that has been omitted.

```
IOB #1: Name = QOUT'
IOB #2: Name = CLKIN'
.
.
.
```

- A horizontal ellipsis "…." indicates that an item can be repeated one or more times.

  `allow block` *block_name loc1 loc2locn;*

Online Documents

The following conventions are used for online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click the red-underlined text to open the specified cross-reference.
- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click the blue-underlined text to open the specified cross-reference.

Contents

Chapter 3 ACC1 to BUFT, 4, 8, 16

Chapter 4 CAPTURE_SPARTAN2 to DECODE32, 64

Chapter 6 GND to KEEPER

Chapter 7 LD to NOR12, 16

Chapter 8 OBUF, 4, 8, 16 to ORCY

Chapter 9 PPC405 to ROM256X1

Chapter 10 SOP3-4 to XORCY_L

Chapter 11 X74_42 to X74_521

Chapter 1

Xilinx Unified Libraries

This chapter describes the Unified Libraries and the applicable device architectures for each library. It also briefly discusses the contents of the other chapters, the general naming conventions, and performance issues.

- This chapter consists of the following major sections.
- "Overview"
- "Applicable Architectures"
- "Selection Guide"
- "Design Elements"
- "Schematic Examples"
- "Naming Conventions"
- "Attributes and Constraints"
- "Carry Logic"
- "Flip-Flop, Counter, and Register Performance"
- "Unconnected Pins"

Overview

Xilinx maintains software libraries with thousands of functional design elements (primitives and macros) for different device architectures. New functional elements are assembled with each release of development system software. The catalog of design elements is known as the "Unified Libraries." Elements in these libraries are common to all Xilinx device architectures. This "unified" approach means that you can use your circuit design created with "unified" library elements across all current Xilinx device architectures that recognize the element you are using.

Elements that exist in multiple architectures look and function the same, but their implementations might differ to make them more efficient for a particular architecture. A separate library still exists for each architecture (or architectural group) and common symbols are duplicated in each one, which is necessary for simulation (especially board level) where timing depends on a particular architecture.

If you have active designs that were created with former Xilinx library primitives or macros, you may need to change references to the design elements that you were using to reflect the Unified Libraries' elements.

The *Libraries Guide* describes the primitive and macro logic elements available in the Unified Libraries for the Xilinx FPGA and CPLD devices. Common logic functions can be implemented with these elements and more complex functions can be built by combining macros and primitives. Several hundred design elements (primitives and

macros) are available across multiple device architectures, providing a common base for programmable logic designs.

This libraries guide provides a functional selection guide, describes the design elements, and addresses attributes, constraints, and carry logic.

Applicable Architectures

Design elements for the Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex -II, Virtex-II PRO, XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II libraries are included in the Xilinx Unified Libraries. Each library supports specific device architectures. For detailed information on the architectural families referenced below and the devices in each, refer to the current version of *The Programmable Logic Data Book* (an online version is available from the Xilinx web site, http://support.xilinx.com).

XC9000 Library

The information appearing under the title XC9000 pertains to the following CPLD device families:

- XC9500
- XC9500XL
- XC9500XV

CoolRunner Library

There are two CoolRunner families:

- CoolRunner XPLA3
- CoolRunner-II

Spartan-II Library

The information appearing under the title Spartan-II pertains to the Spartan-II and Spartan-IIE families.

Virtex Library

The information appearing under the title Virtex pertains to the Virtex family XCV* devices and to the Virtex-E and Virtex-EM families (XCV*E devices).

Virtex-II Library

The information appearing under the title Virtex-II pertains to the Virtex-II and Virtex-II PROfamilies (XC2V* devices).

Selection Guide

The "Selection Guide" chapter briefly describes, then tabularly lists the logic elements that are explained in detail in the "Design Elements" sections. The tables included in this section are organized into functional categories. They list the available elements in each category along with a brief description of each element and an applicability table identifying which libraries (Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex -II,

Virtex-II PRO, XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II) contain the element.

Design Elements

Design elements are organized in alphanumeric order, with all numeric suffixes in ascending order. For example, FDR precedes FDRS, and ADD4 precedes ADD8, which precedes ADD16.

- The following information is provided for each library element.
- Graphic symbol
- Applicability table (with primitive versus macro identification)
- Functional description
- Truth table (when applicable)
- Topology (when applicable)
- Schematic for macros

Schematic Examples

Schematics are included for each library if the implementation differs.

Design elements with bused or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic — generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

Naming Conventions

Examples of the general naming conventions for the unified library elements are shown in the following figures.

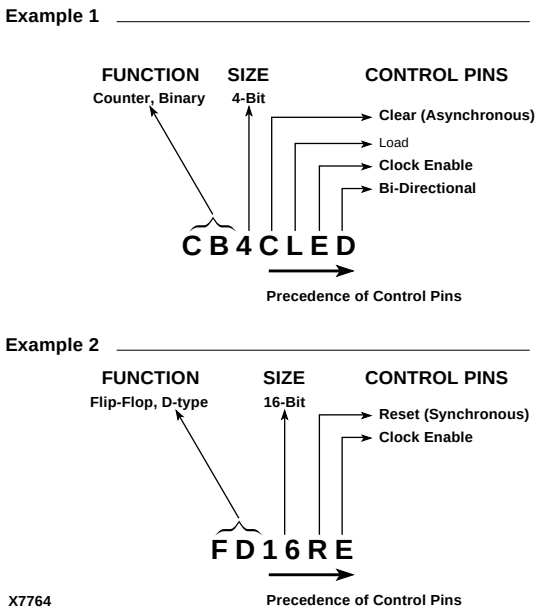


Figure 1-1 Naming Conventions

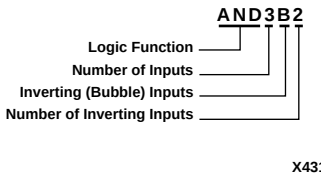


Figure 1-2 Combinatorial Naming Conventions

Refer to the "Selection Guide" chapter for examples of functional component naming conventions.

Attributes and Constraints

Attributes and constraints are instructions placed components or nets to indicate their placement, implementation, naming, directionality, and so forth. The *Constraints Guide* provides information on all attributes and constraints.

Carry Logic

The Spartan-II, Virtex, and Virtex-II architectures include dedicated carry logic components.

Spartan-II, Spartan-IIE, Virtex, and Virtex-E

Carry Logic for Spartan-II, Spartan-IIE, Virtex, and Virtex-E is a simple structure associated with each look up table. The design entry library contains the following dedicated carry logic primitives MUXCY, MUXCY_D, MUXCY_L, XORCY, XORCY_D, and XORCY_L. The function performed is determined by their connectivity and the contents of the look up table.

For detailed information on Carry Logic in Virtex and Spartan-II, refer to *The Programmable Logic Data Book* available on the Xilinx web site, http://support.xilinx.com.

Virtex-II and Virtex-II PRO

The dedicated carry logic primitives for Virtex-II and Virtex-II PRO are MUXCY, MUXCY_D, MUXCY_L, XORCY, XORCY_D, XORCY_L, and ORCY.

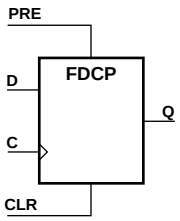
For detailed information on Carry Logic in Virtex-II and Virtex-II PRO, refer to *The Programmable Logic Data Book* available on the Xilinx web site, http://support.xilinx.com.

Flip-Flop, Counter, and Register Performance

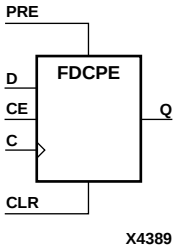
All counter, register, and storage functions are derived from the flip-flops are available in the Configurable Logic Blocks (CLBs).

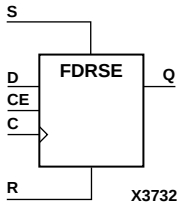
The D flip-flop is the basic building block for all architectures. Differences occur from the availability of asynchronous Clear (CLR) and Preset (PRE) inputs, and the source of the synchronous control signals, such as, Clock Enable (CE), Clock (C), Load enable (L), synchronous Reset (R), and synchronous Set (S). The basic flip-flop configuration for each architecture follows.

The basic XC9000 flip-flops have both Clear and Preset inputs.



Virtex and Spartan-II have two basic flip-flop types. One has both Clear and Preset inputs and one has both asynchronous and synchronous control functions.





The asynchronous and synchronous control functions, when used, have a priority that is consistent across all devices and architectures. These inputs can be either active-High or active-Low as defined by the macro. The priority, from highest to lowest is as follows.

- Asynchronous Clear (CLR)
- Asynchronous Preset (PRE)
- Synchronous Set (S)
- Synchronous Reset (R)
- Clock Enable (CE)

Note The asynchronous CLR and PRE inputs, by definition, have priority over all the synchronous control and clock inputs.

For FPGA families, the Clock Enable (CE) function is implemented using two different methods in the Xilinx Unified Libraries; both are shown in Figure 1-3.

- In method 1, CE is implemented by connecting the CE pin of the macro directly to the dedicated Enable Clock (EC) pin of the internal Configurable Logic Block (CLB) flip-flop. This allows one CE per CLB. CE takes precedence over the L, S, and R inputs. All flip-flops with asynchronous clear or preset use this method.
- In method 2, CE is implemented using function generator logic. This allows two CEs per CLB. CE has the same priority as the L, S, and R inputs. All flip-flops with synchronous set or reset use this method.

The method used in a particular macro is indicated by the inclusion of asynchronous clear, asynchronous preset, synchronous set, or synchronous reset in the macro's description.

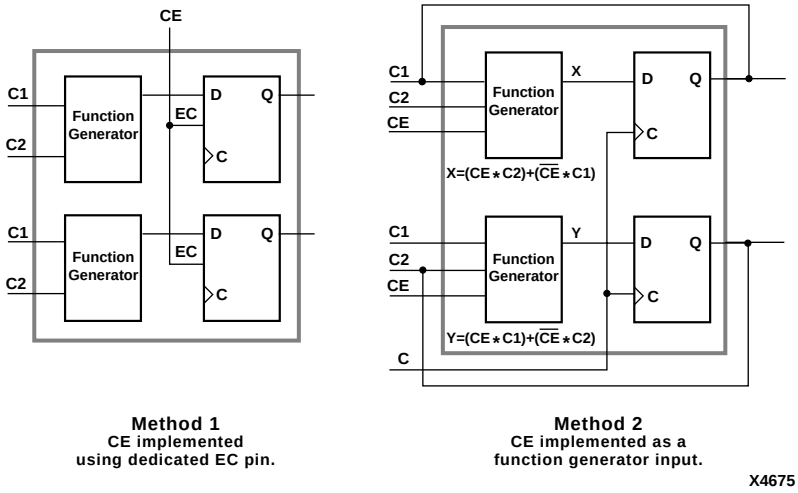


Figure 1-3 Clock Enable Implementation Methods

Unconnected Pins

Xilinx recommends that you *always* connect input pins in your designs. This ensures that front end simulation functionally matches back end timing simulation. If an input pin is left unconnected, mapper errors may result.

If an output pin is left unconnected in your design, the corresponding function is trimmed. If the component has only one output, the entire component is trimmed. If the component has multiple outputs, the portion that drives the output is trimmed. As an example of the latter case, if the overflow pin (OFL) in an adder macro is unconnected, the logic that generates that term is trimmed, but the rest of the adder is retained (assuming all of the sum outputs are connected).

Chapter 2

Selection Guide

This chapter provides a CLB count for the design elements in each library plus a list of the Relationally Placed Modules (RPMs) by family. It also categorizes, by function, the logic elements that are described in detail in the "Design Elements" sections.

The chapter contains two major sections.

- "CLB / Slice Count"
- "Functional Categories"

CLB/Slice Count

Configurable Logic Blocks (CLBs) implement most of the logic in an FPGA.

Each Virtex and Spartan-II CLB contains two slices. Each Virtex-II CLB contains four slices. In the following table, the numbers for Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO are the number of slices required to implememt the component.

The following CLB / Slice Count table lists FPGA design elements in alphanumeric order with the number of CLBs or slices needed for their implementation in each applicable library. Refer to the "Applicable Architectures" section of the "Xilinx Unified Libraries" chapter for information on the specific device architectures supported in each library.

Note This information is for reference only. The actual count could vary, depending upon the switch settings of the implementation tools; for example, the effort level in PAR (Place and Route).

The asterisks for the RAM16X1D and RAM16X1D_1 in the Virtex-II and Virtex-II PRO column indicate that these two design elements consume 1/2 of two slices.

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
ACC4	5	5	6
ACC8	9	9	10
ACC16	17	17	18
ADD4	3	3	3
ADD8	5	5	5
ADD16	9	9	9
ADSU4	3	3	3
ADSU8	5	5	5
ADSU16	9	9	9

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
AND2	1	1	1
AND3	1	1	1
AND4	1	1	1
AND5	1	1	1
AND6	1	1	1
AND7	1	1	1
AND8	2	2	2
AND9	2	2	2
AND12	2	2	2
AND16	2	2	2
BRLSHFT4	8	8	4
BRLSHFT8	12	12	12
BSCAN_SPARTAN2	-	-	-
BSCAN_VIRTEX	-	-	-
BSCAN_VIRTEX2	-	-	-
BUF	-	-	-
BUF4	-	-	-
BUF8	-	-	-
BUF16	-	-	-
BUFCF	-	-	-
BUFE	-	-	-
BUFE4	-	-	-
BUFE8	-	-	-
BUFE16	-	-	-
BUFG	-	-	-
BUFGCE	-	-	-
BUFGCE_1	-	-	-
BUFGDLL	-	-	-
BUFGMUX	-	-	-
BUFGMUX_1	-	-	-
BUFGP	-	-	-
BUFT	-	-	-
BUFT4	-	-	-
BUFT8	-	-	-
BUFT16	-	-	-
CAPTURE_SPARTAN2	-	-	-
CAPTURE_VIRTEX	-	-	-
CAPTURE_VIRTEX2	-	-	-
CB2CE	2	2	3

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
CB2CLE	3	3	3
CB2CLED	3	3	3
CB2RE	2	2	3
CB4CE	3	3	4
CB4CLE	5	5	5
CB4CLED	6	6	7
CB4RE	3	3	4
CB8CE	6	6	7
CB8CLE	9	9	10
CB8CLED	12	12	12
CB8RE	6	6	7
CB16CE	13	13	14
CB16CLE	18	18	19
CB16CLED	24	24	25
CB16RE	13	13	14
CC8CE	8	8	5
CC8CLE	9	9	9
CC8CLED	9	9	17
CC8RE	9	9	9
CC16CE	16	16	9
CC16CLE	17	17	17
CC16CLED	17	17	33
CC16RE	17	17	17
CD4CE	3	3	4
CD4CLE	5	5	5
CD4RE	3	3	4
CD4RLE	7	7	7
CJ4CE	2	2	4
CJ4RE	2	2	4
CJ5CE	3	3	5
CJ5RE	3	3	5
CJ8CE	4	4	4
CJ8RE	4	4	4
CLKDLL	-	-	-
CLKDLLE	-	-	-
CLKDLLHF	-	-	-
COMP2	1	1	1
COMP4	2	2	2
COMP8	3	3	4

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
COMP16	6	6	9
COMPM2	1	1	2
COMPM4	5	5	5
COMPM8	11	11	13
COMPM16	24	24	32
COMPMC8	8	8	8
COMPMC16	16	16	16
CR8CE	8	8	8
CR16CE	16	16	16
CY_INIT	-	-	-
CY_MUX	-	-	-
D2_4E	2	2	2
D3_8E	4	4	4
D4_16E	16	16	16
DCM	-	-	-
DEC_CC4	1	1	1
DEC_CC8	1	1	1
DEC_CC16	2	2	2
DECODE4	1	1	1
DECODE8	2	2	2
DECODE16	2	2	2
DECODE32	4	4	4
DECODE64	8	8	8
F5_MUX	-	-	-
F5MAP	-	-	-
FD	1	1	1
FD_1	1	1	1
FD4CE	2	2	4
FD4RE	2	2	4
FD8CE	4	4	4
FD8RE	4	4	4
FD16CE	8	8	8
FD16RE	8	8	8
FDC	1	1	1
FDC_1	1	1	1
FDCE	1	1	1
FDCE_1	1	1	1
FDCP	1	1	1
FDCP_1	1	1	1

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
FDCPE	1	1	1
FDCPE_1	1	1	1
FDDRCPE	-	-	-
FDDRRSE	-	-	-
FDE	1	1	1
FDE_1	1	1	1
FDP	1	1	1
FDP_1	1	1	1
FDPE	1	1	1
FDPE_1	1	1	1
FDR	1	1	1
FDR_1	1	1	1
FDRE	1	1	1
FDRE_1	1	1	1
FDRS	1	1	1
FDRS_1	1	1	1
FDRSE	1	1	1
FDRSE_1	1	1	1
FDS	1	1	1
FDS_1	1	1	1
FDSE	1	1	1
FDSE_1	1	1	1
FJKC	1	1	1
FJKCE	1	1	1
FJKP	1	1	1
FJKPE	1	1	1
FJKRSE	1	1	1
FJKSRE	1	1	1
FMAP	-	-	-
FTC	1	1	1
FTCE	1	1	1
FTCLE	1	1	1
FTCLEX	1	1	1
FTP	1	1	1
FTPE	1	1	1
FTPLE	1	1	1
FTRSE	1	1	1
FTRSLE	2	2	1
FTSRE	1	1	1

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
FTSRLE	2	2	2
GND	-	-	-
GT_AURORA_n	-	-	-
GT_CUSTOM_n	-	-	-
GT_ETHERNET_n	-	-	-
GT_FIBRE_CHAN_n	-	-	-
GT_INFINIBAND_n	-	-	-
GT_XAUI_n	-	-	-
IBUF	-	-	-
IBUF4	-	-	-
IBUF8	-	-	-
IBUF16	-	-	-
IBUF_selectIO	-	-	-
IBUFDS	-	-	-
IBUFG	-	-	-
IBUFG_selectIO	-	-	-
IBUFGDS	-	-	-
ICAP_VIRTEX2	-	-	-
IFD	-	-	-
IFD_1	-	-	-
IFD4	-	-	-
IFD8	-	-	-
IFD16	-	-	-
IFDDRCPE	-	-	-
IFDDRRSE	-	-	-
IFDI	-	-	-
IFDI_1	-	-	-
IFDX	-	-	-
IFDX4	-	-	-
IFDX8	-	-	-
IFDX16	-	-	-
IFDX_1	-	-	-
IFDXI	-	-	-
IFDXI_1	-	-	-
ILD	1	1	1
ILD_1	1	1	1
ILD4	2	2	2
ILD8	4	4	4
ILD16	8	8	8

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
ILDI	-	-	-
ILDI_1	-	-	-
ILDX	-	-	-
ILDX4	-	-	-
ILDX8	-	-	-
ILDX16	-	-	-
ILDX_1	-	-	-
ILDXI	-	-	-
ILDXI_1	-	-	-
INV	1	1	1
INV4	1	1	1
INV8	1	1	1
INV16	1	1	1
IOBUF	-	-	-
IOBUF_selectIO	-	-	-
IOPAD	-	-	-
IOPAD4	-	-	-
IOPAD8	-	-	-
IOPAD16	-	-	-
IPAD	-	-	-
IPAD4	-	-	-
IPAD8	-	-	-
IPAD16	-	-	-
JTAGPPC	-	-	-
KEEPER	-	-	-
LD	-	-	1
LD_1	1	1	1
LD4	2	2	4
LD8	4	4	4
LD16	8	8	8
LD4CE	2	2	4
LD8CE	4	4	4
LD16CE	8	8	8
LDC	1	1	1
LDC_1	1	1	1
LDCE	1	1	1
LDCE_1	1	1	1
LDCP	1	1	1
LDCP_1	1	1	1

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
LDCPE	1	1	1
LDCPE_1	1	1	1
LDE	1	1	1
LDE_1	1	1	1
LDP	1	1	1
LDP_1	1	1	1
LDPE	1	1	1
LDPE_1	1	1	1
LUT1	1	1	1
LUT2	1	1	1
LUT3	1	1	1
LUT4	1	1	1
LUT1_D	1	1	1
LUT2_D	1	1	1
LUT3_D	1	1	1
LUT4_D	1	1	1
LUT1_L	1	1	1
LUT2_L	1	1	1
LUT3_L	1	1	1
LUT4_L	1	1	1
M2_1	1	1	1
M2_1B1	1	1	1
M2_1B2	1	1	1
M2_1E	1	1	1
M4_1E	1	1	1
M8_1E	2	2	2
M16_1E	5	5	5
MULT_AND	-	-	-
MULT18X18	-	-	-
MULT18X18S	-	-	-
MUXCY	-	-	-
MUXCY_D	-	-	-
MUXCY_L	-	-	-
MUXF5	-	-	-
MUXF5_D	-	-	-
MUXF5_L	-	-	-
MUXF6	-	-	-
MUXF6_D	-	-	-
MUXF6_L	-	-	-

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
MUXF7	-	-	-
MUXF7_D	-	-	-
MUXF7_L	-	-	-
MUXF8	-	-	-
MUXF8_D	-	-	-
MUXF8_L	-	-	-
NAND2	1	1	1
NAND3	1	1	1
NAND4	1	1	1
NAND5	1	1	1
NAND6	1	1	1
NAND7	1	1	1
NAND8	2	2	2
NAND9	2	2	2
NAND12	2	2	2
NAND16	2	2	2
NOR2	1	1	1
NOR3	1	1	1
NOR4	1	1	1
NOR5	1	1	1
NOR6	1	1	1
NOR7	1	1	1
NOR8	2	2	2
NOR9	2	2	2
NOR12	2	2	2
NOR16	2	2	2
OBUF	-	-	-
OBUF4	-	-	-
OBUF8	-	-	-
OBUF16	-	-	-
OBUF_selectIO	-	-	-
OBUFDS	-	-	-
OBUFE	-	-	-
OBUFE4	-	-	-
OBUFE8	-	-	-
OBUFE16	-	-	-
OBUFT	-	-	-
OBUFT4	-	-	-
OBUFT8	-	-	-

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
OBUFT16	-	-	-
OBUFT_selectIO	-	-	-
OBUFTDS	-	-	-
OFD	-	-	-
OFD_1	-	-	-
OFD4	-	-	-
OFD8	-	-	-
OFD16	-	-	-
OFDDRCPE	-	-	-
OFDDRRSE	-	-	-
OFDDRTCPE	-	-	-
OFDDRTRSE	-	-	-
OFDE	-	-	-
OFDE_1	-	-	-
OFDE4	-	-	-
OFDE8	-	-	-
OFDE16	-	-	-
OFDI	-	-	-
OFDI_I	-	-	-
OFDT	-	-	-
OFDT_1	-	-	-
OFDT4	-	-	-
OFDT8	-	-	-
OFDT16	-	-	-
OFDX	-	-	-
OFDX4	-	-	-
OFDX8	-	-	-
OFDX16	-	-	-
OFDX_1	-	-	-
OFDXI	-	-	-
OFDXI_I	-	-	-
OPAD	-	-	-
OPAD4	-	-	-
OPAD8	-	-	-
OPAD16	-	-	-
OR2	1	1	1
OR3	1	1	1
OR4	1	1	1
OR5	1	1	1

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
OR6	1	1	1
OR7	1	1	1
OR8	2	2	2
OR9	2	2	2
OR12	2	2	2
OR16	2	2	2
ORCY	-	-	-
PPC405	-	-	-
PULLDOWN	-	-	-
PULLUP	-	-	-
RAM16X1D	1	1	2*
RAM16X1D_1	1	1	2*
RAM16X1S	1	1	1
RAM16X1S_1	1	1	1
RAM16X2D	2	2	4
RAM16X2S	2	2	2
RAM16X4D	4	4	8
RAM16X4S	4	4	3
RAM16X8D	8	8	16
RAM16X8S	8	8	5
RAM32X1D	-	-	2
RAM32X1D_1	-	-	2
RAM32X1S	1	1	1
RAM32X1S_1	1	1	1
RAM32X2S	2	2	2
RAM32X4S	8	8	3
RAM32X8S	-	-	6
RAM64X1D	-	-	4
RAM64X1D_1	-	-	4
RAM64X1S	-	-	2
RAM64X1S_1	-	-	2
RAM64X2S	-	-	4
RAM128X1S	-	-	4
RAM128X1S_1	-	-	4
RAMB4_Sn	-	-	-
RAMB4_Sm_Sn	-	-	-
RAMB16_Sn	-	-	-
RAMB16_Sm_Sn	-	-	-

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
ROM16X1	1	1	1
ROM32X1	1	1	1
ROM64X1	2	2	2
ROM128X1	-	-	4
ROM256X1	-	-	8
SOP3	1	1	1
SOP4	1	1	1
SR4CE	2	2	4
SR4CLE	3	3	3
SR4CLED	5	5	5
SR4RE	2	2	4
SR4RLE	3	3	3
SR4RLED	5	5	5
SR8CE	4	4	4
SR8CLE	5	5	5
SR8CLED	9	9	9
SR8RE	4	4	4
SR8RLE	5	5	5
SR8RLED	9	9	9
SR16CE	8	8	8
SR16CLE	9	9	9
SR16CLED	17	17	17
SR16RE	8	8	8
SR16RLE	9	9	9
SR16RLED	17	17	17
SRL16	1	1	1
SRL16_1	1	1	1
SRL16E	1	1	1
SRL16E_1	1	1	1
SRLC16	-	-	1
SRLC16_1	-	-	1
SRLC16E	-	-	1
SRLC16E_1	-	-	1
STARTUP_SPARTAN2	-	-	-
STARTUP_VIRTEX	-	-	-
STARTUP_VIRTEX2	-	-	-
UPAD	-	-	-
VCC	-	-	-
XNOR2	1	1	1

Table 2-1 CLB/Slice Count for FPGA Components

	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO
Name	**Number of Slices to Implement**		
XNOR3	1	1	1
XNOR4	1	1	1
XNOR5	1	1	1
XNOR6	1	1	1
XNOR7	1	1	1
XNOR8	2	2	2
XNOR9	2	2	2
XOR2	1	1	1
XOR3	1	1	1
XOR4	1	1	1
XOR5	1	1	1
XOR6	1	1	1
XOR7	1	1	1
XOR8	2	2	2
XOR9	2	2	2
XORCY	-	-	-
XORCY_D	-	-	-
XORCY_L	-	-	-

* The RAM16X1D and RAM16X1D_1 consume 1/2 of two slices.

Functional Categories

This section categorizes, by function, the logic elements that are described in detail in the “Design Elements” sections. Each category is briefly described. Tables under each category identify all the available elements for the function and indicate which libraries include the element.

Elements are listed in alphanumeric order under each category. There are a number of standard TTL 7400-type functions in the different libraries. All 7400-type functions start with an “X74” prefix and are listed after all other elements. The numeric sequence following the “X74” prefix uses ascending numbers, for example, X74_42 precedes X74_138.

Refer to the “Applicable Architectures“ section of the “Xilinx Unified Libraries” chapter for information on the specific device families that use each library. "N / A" column means that the element does not apply.

"RPM" refers to Relatinally Placed Macros. RPMs are “soft” macros that contain relative location constraint (RLOC) information. The Xilinx libraries contain three types of elements.

- Primitives are basic logical elements such as AND2 and OR2 gates.
- Soft macros are schematics made by combining primitives and sometimes other soft macros.
- Relationally placed macros (RPMs) are soft macros that contain relative location constraint (RLOC) information, carry logic symbols, and FMAP symbols, where appropriate.

The last item mentioned above, RPMs, applies only to FPGA families.

The relationally placed macro (RPM) library uses RLOC constraints to define the order and structure of the underlying design primitives. Because these macros are built upon standard schematic parts, they do not have to be translated before simulation. The components that are implemented as RPMs are listed in the “CLB / Slice Count” section.

Designs created with RPMs can be functionally simulated. RPMs can, but need not, include all the following elements.

- FMAPs and CLB-grouping attributes to control mapping. FMAPs have pin-lock attributes, which allow better control over routing.
- Relative location (RLOC) constraints to provide placement structure. They allow positioning of elements relative to each other.
- Carry logic primitive symbols.

The RPM library offers the functionality and precision of the hard macro library with added flexibility. You can optimize RPMs and merge other logic within them. The elements in the RPM library allow you to access carry logic easily and to control mapping and block placement. Because RPMs are a superset of ordinary macros, you can design them in the normal design entry environment. They can include any primitive logic. The macro logic is fully visible to you and can be easily back-annotated with timing information.

The functional categories in this section are as follows.

- Arithmetic Functions
- Buffers

- Comparators
- Counters
- Data Registers
- Decoders
- Edge Decoders
- Encoders
- Flip-Flops
- General
- Input/Output Flip-Flops
- Input/Output Functions
- Input Latches
- Latches
- Logic Primitives
- Map Elements
- Memory Elements
- Multiplexers
- Shift Registers
- Shifters

Note When converting your design between FPGA families, use elements that have equivalent functions in each of the architectural families (libraries) to minimize re-designing.

Arithmetic Functions

There are three types of arithmetic functions: accumulators (ACC), adders (ADD), and adder / subtracters (ADSU). With an ADSU, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated. The following figure shows the ADSU carry-out and overflow boundaries.

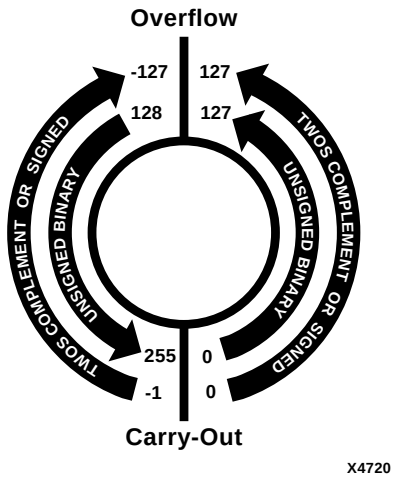


Figure 2-1 ADSU Carry-Out and Overflow Boundaries

ACC1		1-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

ACC4, 8, 16		4-, 8-, 16-Bit Loadable Cascadable Accumulators with Carry-In, Carry-Out, and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

ADD1		1-Bit Full Adder with Carry-In and Carry-Out			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

ADD4, 8, 16		4-, 8-, 16-Bit Cascadable Full Adders with Carry-In, Carry-Out, and Overflow			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

ADSU1		1-Bit Cascadable Adder / Subtracter with Carry-In, Carry-Out			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

ADSU4, 8, 16		4-, 8-, 16-Bit Cascadable Adders / Subtracters with Carry-In, Carry-Out, and Overflow			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	N / A	RPM	Macro	Macro	Macro

MULT18X18		18 x 18 Signed Multiplier			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Primitive	N / A	N / A	N / A

MULT18X18S		18 x 18 Signed Multiplier			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Primitive	N / A	N / A	N / A

X74_280		9-Bit Odd / Even Parity Generator / Checker			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_283		4-Bit Full Adder with Carry-In and Carry-Out			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro*	Macro	Macro

*not supported for XC9500XL and XC9500XV devices

Buffers

The buffers in this section route high fanout signals, 3-state signals, and clocks inside a PLD device. The “” section later in this chapter covers off-chip interfaces.

BUF		General-Purpose Buffer			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

BUF4, 8, 16		4-, 8-, 16-Bit General-Purpose Buffers			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

BUFCF		Fast Connect Buffer			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

BUFE, 4, 8, 16		Internal 3-State Buffers with Active High Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500***	**CoolRunner XPLA3**	**CoolRunner-II**
BUFE -- Primitive BUFE4, 8, 16 -- Macro	Primitive Macro	Primitive Macro	Primitive Macro	Primitive Macro	Primitive Macro

* not supported for XC9500XL and XC9500XV devices

BUFG		Global Clock Buffer			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

BUFGCE		Global Clock MUX with Clock Enable and Output State 0			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Macro	N / A	N / A	N / A

BUFGCE_1		Global Clock MUX Buffer with Clock Enable and Output State 1			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Macro	N / A	N / A	N / A

BUFGDLL		Clock Delay Locked Loop Buffer			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

BUFGMUX		Global Clock MUX Buffer with Output State 0			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	√	N / A	N / A	N / A

BUFGMUX_1		Global Clock MUX with Output State 1			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Primitive	N / A	N / A	N / A

BUFGP		Primary Global Buffer for Driving Clocks or Longlines (Four per PLD Device)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

BUFGSR		Global Set / Reset Input Buffer			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Primitive	Primitive	Primitive

BUFGTS		Global 3-State Input Buffer			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Primitive	Primitive	Primitive

BUFT, 4, 8, 16		Internal 3-State Buffers with Active-Low Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500**	**CoolRunner XPLA3**	**CoolRunner-II**
BUFT-- Primitive	Primitive	Primitive	Primitive*	Primitive	Primitive
BUFT4, 8, 16 -- Macro	Macro	Macro	Macro*	Macro	Macro

*not supported for XC9500XL and XC9500XV devices

Comparators

There are two types of comparators, identity (COMP) and magnitude (COMPM).

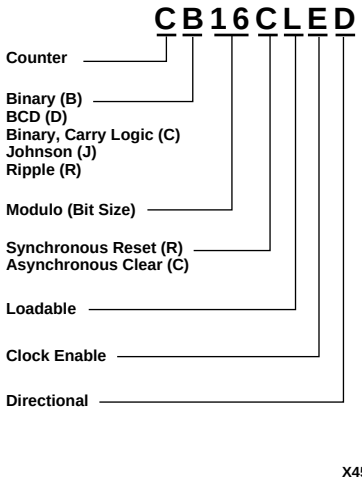


Figure 2-2 Comparator Naming Convention

COMP2, 4, 8, 16		2-, 4-, 8-, 16-Bit Identity Comparators			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

COMPM2, 4, 8, 16		2-, 4-, 8-, 16-Bit Magnitude Comparators			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

COMPMC8, 16		8-, 16-Bit Magnitude Comparators			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

X74_L85		4-Bit Expandable Magnitude Comparator			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

X74_518		8-Bit Identity Comparator with Active-Low Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

X74_521		8-Bit Identity Comparator with Active-Low Enable and Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

Counters

There are six types of counters with various synchronous and asynchronous inputs. The name of the counter defines the modulo or bit size, the counter type, and which control functions are included. The counter naming convention is shown in the following figure.

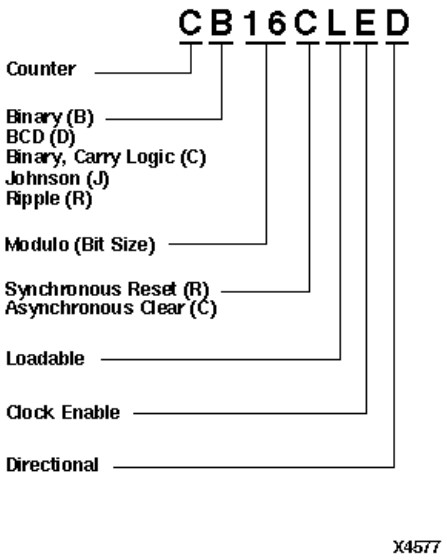


Figure 2-3 Counter Naming Convention

A carry-lookahead design accommodates large counters without extra gating. On TTL 7400-type counters with trickle clock enable (ENT), parallel clock enable (ENP), and ripple carry-out (RCO), both the ENT and ENP inputs must be High to count. ENT is propagated forward to enable RCO, which produces a High output with the approximate duration of the QA output. The following figure illustrates a carry-lookahead design.

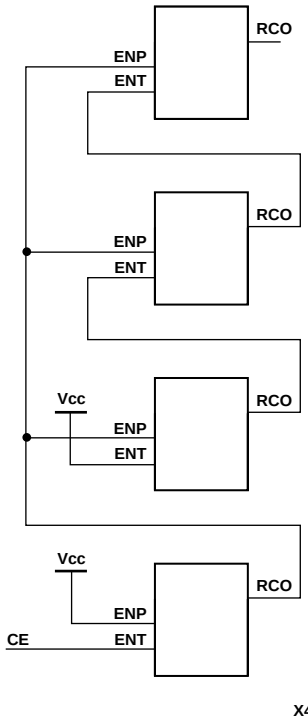


Figure 2-4 Carry-Lookahead Design

The RCO output of the first stage of the ripple carry is connected to the ENP input of the second stage and all subsequent stages. The RCO output of the second stage and all subsequent stages is connected to the ENT input of the next stage. The ENT of the second stage is always enabled / tied to VCC. CE is always connected to the ENT input of the first stage. This cascading method allows the first stage of the ripple carry to be built as a prescaler. In other words, the first stage is built to count very fast.

CB2CE, CB4CE, CB8CE, CB16CE		2-, 4-, 8-, 16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CB2CLE, CB4CLE, CB8CLE, CB16CLE		2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CB2CLED, CB4CLED, CB8CLED, CB16CLED		2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CB2RE, CB4RE, CB8RE, CB16RE		2-, 4-, 8-, 16-Bit Cascadable Binary Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CB2RLE, CB4RLE, CB8RLE, CB16RLE		2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

CB2X1, CB4X1, CB8X1, CB16X1		2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

CB2X2, CB4X2, CB8X2, CB16X2		2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

CBD2CE, CBD4CE, CBD8CE, CBD16CE		2-, 4-, 8-,16-Bit Cascadable Dual Edge Triggered Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CBD2CLE, CBD4CLE, CBD8CLE, CBD16CLE		2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CBD2CLED, CBD4CLED, CBD8CLED, CBD16CLED		2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CBD2RE, CBD4RE, CBD8RE, CBD16RE		2-, 4-, 8-, 16-Bit Cascadable Dual Edge Triggered Binary Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CBD2RLE, CBD4RLE, CBD8RLE, CBD16RLE		2-, 4-, 8-, 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CBD2X1, CBD4X1, CBD8X1, CBD16X1**C**		2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CBD2X2, CBD4X2, CBD8X2, CBD16X2		2-, 4-, 8-, and 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CC8CE, CC16CE		8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

CC8CLE, CC16CLE		8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N/A	N/A	N/A

CC8CLED, CC16CLED		8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N/A	N/A	N/A

CC8RE, CC16RE		8-, 16-Bit Cascadable Binary Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N / A	N / A	N / A

CD4CE		4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CD4CLE		4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CD4RE		4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CD4RLE		4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CDD4CE					
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	N / A	N / A	√

CDD4CLE		4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	N / A	N / A	Macro

CDD4RE		4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	N / A	N / A	Macro

CDD4RLE		4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CDD4CE		4-, 5-, 8-Bit Johnson Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CJ4CE, CJ5CE, CJ8CE		4-, 5-, 8-Bit Johnson Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CJ4RE, CJ5RE, CJ8RE		4-, 5-, 8-Bit Johnson Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CJD4CE, CJD5CE, CJD8CE		4-, 5-, 8-Bit Dual Edge Triggered Johnson Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
√	√	√	√	√	√

CJD4RE, CJD5RE, CJD8RE		4-, 5-, 8-Bit Dual Edge Triggered Johnson Counters with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

CR8CE, CR16CE		8-, 16-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

CRD8CE, CRD16CE		8-, 16-Bit Dual-Edge Triggered Binary Ripple Counters with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

X74_160		4-Bit BCD Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_161		4-Bit Binary Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_162		4-Bit BCD Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_163		4-Bit Binary Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_168		4-Bit BCD Bidirectional Counter with Parallel and Trickle Clock Enables and Active-Low Load Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_390		4-Bit BCD / Bi-Quinary Ripple Counter with Negative-Edge Clocks and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

Data Registers

There are three TTL 7400-type data registers designed to function exactly as the TTL elements for which they are named.

X74_174		6-Bit Data Register with Active-Low Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_273		8-Bit Data Register with Active-Low Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_377		8-Bit Data Register with Active-Low Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

Decoders

Decoder names, shown in the following figure, indicate the number of inputs and outputs and wherther or not an enable is available. Decoders with an enable can be used as multiplexers. This group includes some standard TTL 7400-type decoders whose names have an “X74” prefix.

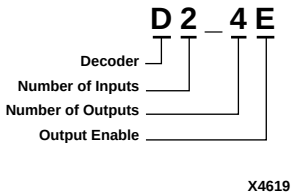


Figure 2-5 Decoder Naming Convention

D2_4E		2- to 4-Line Decoder / Demultiplexer with Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

D3_8E		3- to 8-Line Decoder / Demultiplexer with Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

D4_16E		4- to 16-Line Decoder / Demultiplexer with Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

DEC_CC4, 8, 16		4-, 8-, 16-Bit Active Low Decoders			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

X74_42		4- to 10-Line BCD-to-Decimal Decoder with Active-Low Outputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_138		3- to 8-Line Decoder / Demultiplexer with Active-Low Outputs and Three Enables			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_139		2- to 4-Line Decoder / Demultiplexer with Active-Low Outputs and Active-Low Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_154		4- to 16-Line Decoder / Demultiplexer with Two Enables and Active-Low Outputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

Edge Decoders

Edge decoders are open-drain wired-AND gates that are available in different bit sizes.

DECODE4, 8, 16		4-, 8-, 16-Bit Active-Low Decoders			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N/A	N/A	N/A

DECODE32, 64		32- and 64-Bit Active-Low Decoders			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N/A	N/A	N/A

Encoders

There are two priority encoders (ENCPR) that function like the TTL 7400-type elements they are named after. There is a 10- to 4-line BCD encoder and an 8- to 3-line binary encoder.

X74_147		10- to 4-Line Priority Encoder with Active-Low Inputs and Outputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_148		8- to 3-Line Cascadable Priority Encoder with Active-Low Inputs and Outputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

Flip-Flops

There are three types of flip-flops (D, J-K, toggle) with various synchronous and asynchronous inputs. Some are available with inverted clock inputs and/or the ability to set in response to global set/reset rather than reset. The naming convention shown in the following figure provides a description for each flip-flop. D-type flip-flops are available in multiples of up to 16 in one macro.

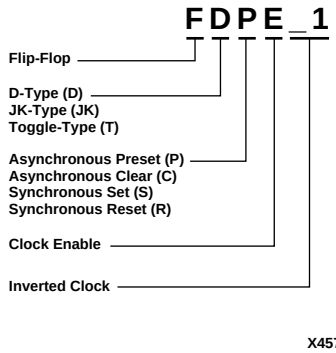


Figure 2-6 Flip-Flop Naming Convention

FD		D Flip-Flop			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FD_1		D Flip-Flop with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

FD4, 8, 16		Multiple D Flip-Flops			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

FD4CE, FD8CE, FD16CE		4-, 8-, 16-Bit Data Registers with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

FD4RE, FD8RE, FD16RE		4-, 8-, 16-Bit Data Registers with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

FDC		D Flip-Flop with Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDC_1		D Flip-Flop with Negative-Edge Clock and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

FDCE		D Flip-Flop with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

FDCE_1		D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

FDCP		D Flip-Flop with Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

FDCP_1		D Flip-Flop with Negative-Edge Clock and Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

FDCPE		D Flip-Flop with Clock Enable and Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDCPE_1		D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

FDD		Dual Edge Triggered D Flip-Flop			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDD4,8,16		Multiple Dual Edge Triggered D Flip-Flops			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDD4CE, FDD8CE, FDD16CE		4-, 8-, 16-Bit Dual Edge Triggered Data Registers with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FD4RE, FD8RE, FD16RE		4-, 8-, 16-Bit Dual Edge Triggered Data Registers with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDC		D Dual Edge Triggered Flip-Flop with Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDCE		Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

FDDCP		Dual Edge Triggered D Flip-Flop Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

FDDCPE		Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

FDDP		Dual Edge Triggered D Flip-Flop with Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

FDDPE		Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

FDDR		Dual Edge Triggered D Flip-Flop with Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDRCPE		Dual Data Rate D Flip-Flop with Clock Enable and Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

FDDRE		Dual Edge Triggered D Flip-Flop with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDRRSE		Dual Data Rate D Flip-Flop with Clock Enable and Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

FDDRS		Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDRSE		Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDS		Dual Edge Triggered D Flip-Flop with Synchronous Set			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDSE		D Flip-Flop with Clock Enable and Synchronous Set			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDSR		Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDDSRE		Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FDE		D Flip-Flop with Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

FDE_1		D Flip-Flop with Negative-Edge Clock and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

FDP		D Flip-Flop with Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDP_1		D Flip-Flop with Negative-Edge Clock and Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

FDPE		D Flip-Flop with Clock Enable and Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

FDPE_1		D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

FDR		D Flip-Flop with Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDR_1		D Flip-Flop with Negative-Edge Clock and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

FDRE		D Flip-Flop with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDRE_1		D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

FDRS		D Flip-Flop with Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDRS_1		D Flip-Flop with Negative-Clock Edge and Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

FDRSE		D Flip-Flop with Synchronous Reset and Set and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDRSE_1		D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

FDS		D Flip-Flop with Synchronous Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDS_1		D Flip-Flop with Negative-Edge Clock and Synchronous Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

FDSE		D Flip-Flop with Clock Enable and Synchronous Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Macro	Macro

FDSE_1		D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

FDSR		D Flip-Flop with Synchronous Set and Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

FDSRE		D Flip-Flop with Synchronous Set and Reset and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

FJKC		J-K Flip-Flop with Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

FJKCE		J-K Flip-Flop with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

FJKCP		J-K Flip-Flop with Asynchronous Clear and Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

FJKCPE		J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

FJKP		J-K Flip-Flop with Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FJKPE		J-K Flip-Flop with Clock Enable and Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FJKRSE		J-K Flip-Flop with Clock Enable and Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FJKSRE		J-K Flip-Flop with Clock Enable and Synchronous Set and Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTC		Toggle Flip-Flop with Toggle Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTCE		Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTCLE		Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTCLEX		**Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear**			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N/A	N/A	N/A

FTCE		Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Primitive	Primitive	Primitive

FTCP		Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Primitive	Primitive	Primitive

FTCPE		Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

FTCPLE		Loadable Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	Macro	Macro	Macro

FTDCE		Dual Edge Triggered Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FTDCLE		Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FTDCLEX		Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FTDCP		Dual Edge Triggered Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FTDRSLE		Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

FTP		Toggle Flip-Flop with Toggle Enable and Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTPE		Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTPLE		Toggle / Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTRSE		Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTRSLE		Toggle / Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTSRE		Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

FTSRLE		Toggle / Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	Macro	Macro	Macro

General

General elements include FPGA configuration functions, oscillators, boundary scan logic, and other functions not classified in other sections.

BSCAN_SPARTAN2		Spartan2 Boundary Scan Logic Control Circuit			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	N/A	N/A	N/A	N/A	N/A

BSCAN_VIRTEX		Virtex Boundary Scan Logic Control Circuit			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	Primitive	N/A	N/A	N/A	N/A

BSCAN_VIRTEX2		Virtex2 Boundary Scan Logic Control Circuit			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

CAPTURE_SPARTAN2		Spartan-II Register State Capture for Bitstream Readback			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	N/A	N/A	N/A	N/A	N/A

CAPTURE_VIRTEX		Virtex Register State Capture for Bitstream Readback			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	Primitive	N/A	N/A	N/A	N/A

CAPTURE_VIRTEX2		Virtex-II Register State Capture for Bitstream Readback			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

CLK_DIV2,4,6,8,10,12,14,16		Global Clock Divider			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

CLK_DIV2,4,6,8,10,12,14,16R		Global Clock Divider with Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

CLK_DIV2,4,6,8,10,12,14,16RSD		Global Clock Divider with Synchronous Reset and Start Delay			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

CLK_DIV2,4,6,8,10,12,14,16SD		Global Clock Divider with Start Delay			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Primitive

CLKDLL		Clock Delay Locked Loop			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive*	N/A	N/A	N/A	N/A

* Use CLKDLLE for Virtex-E Devices

CLKDLLE		Clock Delay Locked Loop with Expanded Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	Primitive*	N/A	N/A	N/A	N/A

* Use CLKDLLE for Virtex-E Devices

CLKDLLHF		High Frequency Clock Delay Locked Loop			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive*	N/A	N/A	N/A	N/A

*Use CLKDLLE for Virtex-E devices

DCM		Digital Clock Manager			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

GND		Ground-Connection Signal Tag			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

ICAP_VIRTEX2		User Interface to Virtex2 Internal Configuration Access Port			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

JTAGPPC		JTAG Primitive for the Power PCl			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive*	N/A	N/A	N/A

* Not supported for Virtex-II. Only supported for Virtex-II PRO

KEEPER		KEEPER Symbol			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LUT1, 2, 3, 4		1-, 2-, 3-, 4-Bit Look-Up-Table with General Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LUT1_D, LUT2_D, LUT3_D, LUT4_D		1-, 2-, 3-, 4-Bit Look-Up-Table with Dual Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LUT1_L, LUT2_L, LUT3_L, LUT4_L		1-, 2-, 3-, 4-Bit Look-Up-Table with Local Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

PPC405		Primitive for Power PC Core			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO***	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

* Not supported for Virtex-II. Only for Virtex-II PRO.

PULLDOWN		Resistor to GND for Input Pads			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

PULLUP		Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

STARTUP_SPARTAN2		Spartan2 User Interface to Global Clock, Reset, and 3-State Controls			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	N/A	N/A	N/A	N/A	N/A

STARTUP_VIRTEX		Virtex User Interface to Global Clock, Reset, and 3-State Controls			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	Primitive	N/A	N/A	N/A	N/A

STARTUP_VIRTEX2		Virtex2 User Interface to Global Clock, Reset, and 3-State Controls			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

UPAD		Schematic-Level Table of Basic Timing Specification Groups			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

VCC		VCC-Connection Signal Tag			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

Input/Output Flip-Flops

Input/Output flip-flops are configured in IOBs. They include flip-flops whose outputs are enabled by 3-state buffers, flip-flops that can be set upon global set/reset rather than reset, and flip-flops with inverted clock inputs. The naming convention specifies each flip-flop function and is illustrated in the following figure.

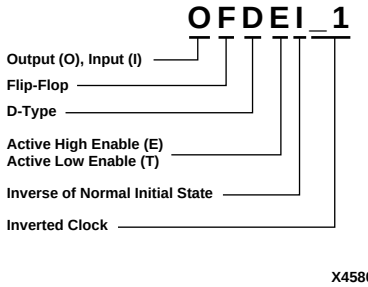


Figure 2-7 Input/Output Flip-Flop Naming Convention

IFD, 4, 8, 16		Single- and Multiple-Input D Flip-Flop			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

IFD_1		Input D Flip-Flop with Inverted Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

IFDDRCPE		Dual Data Rate Input D Flip-Flop with Clock Enable and Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Macro	N/A	N/A	N/A

IFDDRRSE		Dual Data Rate Input D Flip-Flop with Synchronous Reset and Set and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Macro	N/A	N/A	N/A

IFDI		Input D Flip-Flop (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

IFDI_1		Input D Flip-Flop with Inverted Clock (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

IFDX, 4, 8, 16		Single- and Multiple-Input D Flip-Flops with Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

IFDX_1		Input D Flip-Flop with Inverted Clock and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

IFDXI		Input D Flip-Flop with Clock Enable (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

IFDXI_1		Input D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

OFD, 4, 8, 16		Single- and Multiple-Output D Flip-Flops			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

OFD_1		Output D Flip-Flop with Inverted Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

OFDDRCPE		Dual Data Rate Output D Flip-Flop with Clock Enable and Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Macro	N / A	N / A	N / A

OFDDRRSE		Dual Data Rate Output D Flip-Flop with Synchronous Reset and Set and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Macro	N / A	N / A	N / A

OFDDRTCPE		Dual Data Rate D Flip-Flop with Active-Low 3--State Output Buffer, Clock Enable, and Asynchronous Preset and Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Macro	N / A	N / A	N / A

OFDDRTRSE		Dual Data Rate D Flip-Flop with Active -Low 3-State Output Buffer, Synchronous Reset and Set, and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Macro	N / A	N / A	N / A

OFDE, 4, 8, 16		D Flip-Flops with Active-High Enable Output Buffers			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

OFDE_1		D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

OFDI		Output D Flip-Flop (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

OFDI_1		Output D Flip-Flop with Inverted Clock (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

OFDT, 4, 8, 16		Single and Multiple D Flip-Flops with Active-Low 3-State Output Buffers			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

OFDT_1		D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

OFDX, 4, 8, 16		Single- and Multiple-Output D Flip-Flops with Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
√	√	√	N / A	N / A	N / A

OFDX_1		Output D Flip-Flop with Inverted Clock and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

OFDXI		Output D Flip-Flop with Clock Enable (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

OFDXI_1		Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

Input/Output Functions

Input/Output Block (IOB) resources are configured into various I/O primitives and macros for convenience, such as, output buffers (OBUFs) and output buffers with an enable (OBUFEs). Pads used to connect the circuit to PLD device pins are also included.

Virtex and Spartan2 have multiple variants (primitives) to choose from for each selectI/O buffer. The I/O interface for each variant corresponds to a specific I/O standard.

GT_AURORA_n		Gigabit Transceiver for High-Speed I/O			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO***	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

*Not supported for Virtex-II. Only supported for Virtex-II PRO

GT_CUSTOM		Gigabit Transceiver for High-Speed I/O			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO***	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

*Not supported for Virtex-II. Only supported for Virtex-II PRO

GT_ETHERNET_n		Gigabit Transceiver for High-Speed I/O			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO***	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

*Not supported for Virtex-II. Only supported for Virtex-II PRO

GT_FIBRE_CHAN_n		Gigabit Transceiver for High-Speed I/O			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO***	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

*Not supported for Virtex-II. Only supported for Virtex-II PRO

GT_INFINIBAND_n		Gigabit Transceiver for High-Speed I/O			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO***	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

*Not supported for Virtex-II. Only supported for Virtex-II PRO

GT_XAUI_n		10-Gigabit Transceiver for High-Speed I/O			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO***	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

*Not supported for Virtex-II. Only supported for Virtex-II PRO

IBUF, 4, 8, 16		Single- and Multiple-Input Buffers			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
IBUF -- Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IBUF4, 8, 16 -- Macro	Macro	Macro	Macro	Macro	Macro

IBUF_selectIO		Single Input Buffer with Selectable I/O Interface (multiple primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

IBUFDS		Differential Signaling Input Buffer with Selectable I/O Interface			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

IBUFG, IBUFG_selectIO		Dedicated Input Buffer with Selectable I/O Interface (multiple primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

IBUFGDS		Dedicated Differential Signaling Input Buffer with Selectable I/O Interface			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

IOBUF, IOBUF_selectIO		Bi-Directional Buffer with Selectable I/0 Interface (multiple primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
√	√	√	N/A	N/A	N/A

IOPAD, 4, 8, 16		Single- and Multiple-Input/Output Pads			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

IPAD, 4, 8, 16		Single- and Multiple-Input Pads			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
IPAD -- Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IPAD4, 8, 16 -- Macro	Macro	Macro	Macro	Macro	Macro

JTAGPPC		JTAG Primitive for the Power PC			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO***	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

Not supported fro Virtex-II. Only supported for Virtex-II PRO.

OBUF, 4, 8, 16		Single- and Multiple-Output Buffers			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
OBUF -- Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OBUF4, 8, 16 -- Macro	Macro	Macro	Macro	Macro	Macro

OBUF_selectIO		Single Output Buffer with Selectable I/O Interface (multiple primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

OBUFDS		Differential Signaling Output Buffer with Selectable I/O Interface			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

OBUFE, 4, 8, 16		3-State Output Buffers with Active-High Output Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
OBUFE -- Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUFE4, 8, 16 -- Macro	Macro	Macro	Macro	Macro	Macro

OBUFT, 4, 8, 16		Single and Multiple 3-State Output Buffers with Active Low Output Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
OBUFT -- Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OBUFT4, 8, 16 -- Macro	Macro	Macro	Macro	Macro	Macro

OBUFT_selectIO		Single 3-State Output Buffer with Active-Low Output Enable and Selectable I/O Interface (multiple primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

OBUFTDS		3-State Output Buffer with Differential Signaling, Active-Low Output Enable, and Selectable I/O Interface			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

OPAD, 4, 8, 16		Single- and Multiple-Output Pads			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
OPAD -- Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OPAD4, 8, 16 -- Macro	Macro	Macro	Macro	Macro	Macro

UPAD		Connects the I/O Node of an IOB to the Internal PLD Circuit			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

Input Latches

Single and multiple input latches can hold transient data entering a chip. Input latches use the same naming convention as I/O flip-flops.

ILD, 4, 8, 16		Transparent Input Data Latches			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

ILD_1		Transparent Input Data Latch with Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

ILDI		Transparent Input Data Latch (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

ILDI_1		Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

ILDX, 4, 8, 16		Transparent Input Data Latches			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

ILDX_1		Transparent Input Data Latch with Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

ILDXI		Transparent Input Data Latch (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

ILDXI_1		Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

Latches

Latches (LD) are available for all architectures.

LD		Transparent Data Latch			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Primitive	Primitive

LD_1		Transparent Data Latch with Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LD4, 8, 16		Multiple Transparent Data Latches			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

LDC		Transparent Data Latch with Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Primitive	Primitive

LDC_1		Transparent Data Latch with Asynchronous Clear and Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDCE		Transparent Data Latch with Asynchronous Clear and Gate Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDCE_1		Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LD4CE, LD8CE, LD16CE		Transparent Data Latches with Asynchronous Clear and Gate Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

LDCP		Transparent Data Latch with Asynchronous Clear and Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Primitive	Primitive

LDCP_1		Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDCPE		Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDCPE_1		Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDE		Transparent Data Latch with Gate Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDE_1		Transparent Data Latch with Gate Enable and Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDP		Transparent Data Latch with Asynchronous Preset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Macro	Primitive	Primitive

LDP_1		Transparent Data Latch with Asynchronous Preset and Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDPE		Transparent Data Latch with Asynchronous Preset and Gate Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

LDPE_1		Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

Logic Primitives

Combinatorial logic gates that implement the basic Boolean functions are available in all architectures with up to five inputs in all combinations of inverted and non-inverted inputs, and with six to nine inputs non-inverted.

AND2-9		2- to 9-Input AND Gates with Inverted and Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

AND12, 16		12- and 16-Input AND Gates with Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N / A	N / A	N / A

INV, 4, 8, 16		Single and Multiple Inverters			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
INV -- Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
INV4, 8, 16 -- Macro	Macro	Macro	Macro	Macro	Macro

MULT_AND		Fast Multiplier AND			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

MULT18X18		18 x 18 Signed Multiplier			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Primitive	N / A	N / A	N / A

MULT18X18S		18 x 18 Signed Multiplier -- Registered Version			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Primitive	N / A	N / A	N / A

NAND2-9		2- to 9-Input NAND Gates with Inverted and Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

NAND12, 16		12- and 16-Input NAND Gates with Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N/A	N/A	N/A

NOR2-9		2- to 9-Input NOR Gates with Inverted and Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

NOR12, 16		12 and 16-Input NOR Gates with Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N/A	N/A	N/A

OR2-9		2- to 9-Input OR Gates with Inverted and Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

OR12, 16		12- and 16-Input OR Gates with Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
RPM	RPM	RPM	N/A	N/A	N/A

ORCY		OR with Carry Logic			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

SOP3-4		Sum of Products			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

XNOR2-9		2- to 9-Input XNOR Gates with Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
XNOR2, 3, 4, 5 -- Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR6, 7, 8, 9 -- RPM	RPM	RPM	Macro	Macro	Macro

XOR2-9		2- to 9-Input XOR Gates with Non-Inverted Inputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
XOR2, 3, 4, 5 -- Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XOR6, 7, 8, 9 -- RPM	RPM	RPM	Macro	Macro	Macro

XORCY		XOR for Carry Logic with General Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

XORCY_D		XOR for Carry Logic with Dual Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

XORCY_L		XOR for Carry Logic with Local Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

Map Elements

Map elements are used in conjunction with logic symbols to constrain the logic to particular CLBs or particular F or H function generators.

FMAP		F Function Generator Partitioning Control Symbol			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

Memory Elements

In the Virtex, Virtex-E, Spartan-II, and Spartan-IIE architectures, a number of static RAMs are defined as primitives. These 16- or 32-word RAMs are 1, 2, 4, and 8 bits wide. T.

The Virtex, Virtex-E, Spartan-II, and Spartan-IIE architectures have dedicated blocks of on-chip 4096-bit single-port and dual-port synchronous RAM. Each port is configured to a specific data width. There are five single-port block RAM primitives and 30 dual-port block RAM primitives.

RAM16X1D		16-Deep by 1-Wide Static Dual Port Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

RAM16X1D_1		16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

RAM16X1S		16-Deep by 1-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

RAM16X1S_1		16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

RAM16X2D		16-Deep by 2-Wide Static Dual Port Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

RAM16X2S		16-Deep by 2-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Primitive	N/A	N/A	N/A

RAM16X4D		16-Deep by 4-Wide Static Dual Port Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N/A	N/A	N/A

RAM16X4S		16-Deep by 4-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Primitive	N / A	N / A	N / A

RAM16X8D		16-Deep by 8-Wide Static Dual Port Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	N / A	N / A	N / A

RAM16X8S		16-Deep by 8-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Primitive	N / A	N / A	N / A

RAM32X1D		32-Deep by 1-Wide Static Dual Port Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Primitive	N / A	N / A	N / A

RAM32X1D_1		32-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	Primitive	N / A	N / A	N / A

RAM32X1S		32-Deep by 1-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

RAM32X1S_1		32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N / A	N / A	N / A

RAM32X2S		32-Deep by 2-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Primitive	N / A	N / A	N / A

RAM32X4S		32-Deep by 4-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Primitive	N/A	N/A	N/A

RAM32X8S		32-Deep by 8-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Primitive	N/A	N/A	N/A

RAM64X1D		64-Deep by 1-Wide Static Dual Port Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

RAM64X1D_1		64-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

RAM64X1S		64-Deep by 1-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

RAM64X1S_1		64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

RAM64X2S		64-Deep by 2-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

RAM128X1S		128-Deep by 1-Wide Static Synchronous RAM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

RAM128X1S_1		128-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

RAMB4_Sn		4096-Bit Single-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 8, or 16 Bits (5 primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	N/A	N/A	N/A	N/A

RAMB4_Sm_Sn		4096-Bit Dual-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 8, or 16 Bits (15 primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	N/A	N/A	N/A	N/A

RAMB16_Sn		16384-Bit Data Memory and 2048-Bit Parity Memory, Single-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 9, 18, or 36 Bits (6 primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

RAMB16_Sm_Sn		16384-Bit Data Memory and 2048-Bit Parity Memory, Dual-Port Synchronous Block RAM with Port Width (m or n) Configured to 1, 2, 4, 9, 18, or 36 Bits (21 primitives)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

ROM16X1		16-Deep by 1-Wide ROM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

ROM32X1		32-Deep by 1-Wide ROM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

ROM64X1		64-Deep by 1-Wide ROM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

ROM128X1		128-Deep by 1-Wide ROM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

ROM256X1		256-Deep by 1-Wide ROM			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

Multiplexers

The multiplexer naming convention shown in the following figure indicates the number of inputs and outputs and whether or not an enable is available. There are a number of TTL 7400-type multiplexers that have active-Low or inverted outputs.

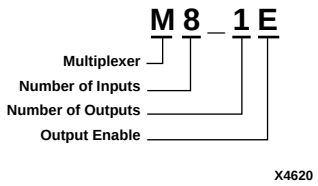


Figure 2-8 Multiplexer Naming Convention

M2_1		2-to-1 Multiplexer			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

M2_1B1		2-to-1 Multiplexer with D0 Inverted			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

M2_1B2		2-to-1 Multiplexer with D0 and D1 Inverted			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

M2_1E		2-to-1 Multiplexer with Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

M4_1E		4-to-1 Multiplexer with Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

M8_1E		8-to-1 Multiplexer with Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

M16_1E		16-to-1 Multiplexer with Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

MUXCY		2-to-1 Multiplexer for Carry Logic with General Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

MUXCY_D		2-to-1 Multiplexer for Carry Logic with Dual Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

MUXCY_L		2-to-1 Multiplexer for Carry Logic with Local Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

MUXF5		2-to-1 Lookup Table Multiplexer with General Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

MUXF5_D		2-to-1 Lookup Table Multiplexer with Dual Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

MUXF5_L		2-to-1 Lookup Table Multiplexer with Local Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

MUXF6		2-to-1 Lookup Table Multiplexer with General Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
√	√	√	N/A	N/A	N/A

MUXF6_D		2-to-1 Lookup Table Multiplexer with Dual Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

MUXF6_L		2-to-1 Lookup Table Multiplexer with Local Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

MUXF7		2-to-1 Lookup Table Multiplexer with General Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

MUXF7_D		2-to-1 Lookup Table Multiplexer with Dual Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

MUXF7_L		2-to-1 Lookup Table Multiplexer with Local Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

MUXF8		2-to-1 Lookup Table Multiplexer with General Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

MUXF8_D		2-to-1 Lookup Table Multiplexer with Dual Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

MUXF8_L		2-to-1 Lookup Table Multiplexer with Local Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

X74_150		16-to-1 Multiplexer with Active-Low Enable and Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_151		8-to-1 Multiplexer with Active-Low Enable and Complementary Outputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_152		8-to-1 Multiplexer with Active-Low Output			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_153		Dual 4-to-1 Multiplexer with Active-Low Enables and Common Select Input			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_157		Quadruple 2-to-1 Multiplexer with Common Select and Active-Low Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_158		Quadruple 2-to-1 Multiplexer with Common Select, Active-Low Enable, and Active-Low Outputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_298		Quadruple 2-Input Multiplexer with Storage and Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_352		Dual 4-to-1 Multiplexer with Active-Low Enables and Outputs			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

Shift Registers

Shift registers are available in a variety of sizes and capabilities. The naming convention shown in the following figure illustrates available features.

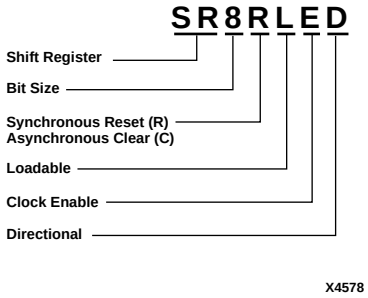


Figure 2-9 Shift Register Naming Convention

SR4CE, SR8CE, SR16CE		4-, 8-, 16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

SR4CLE, SR8CLE, SR16CLE		4-, 8-, 16-Bit Loadable Serial / Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

SR4CLED, SR8CLED, SR16CLED		4-, 8-, 16-Bit Shift Registers with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

SR4RE, SR8RE, SR16RE		4-, 8-, 16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

SR4RLE, SR8RLE, SR16RLE		4-, 8-, 16-Bit Loadable Serial / Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

SR4RLED, SR8RLED, SR16RLED		4-, 8-, 16-Bit Shift Registers with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

SRD4CE, SRD8CE, SRD16CE		4-, 8-, 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Registers with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

SRD4CLE, SRD8CLE, SRD16CLE		4-, 8-, 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Registers with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

SRD4CLED, SRD8CLED, SRD16CLED		4-, 8-, 16-Bit Dual Edge Triggered Shift Registers with Clock Enable and Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

SRD4RE, SRD8RE, SRD16RE		4-, 8-, 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Registers with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

SRD4RLE, SRD8RLE, SRD16RLE		4-, 8-, 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Registers with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

SRD4RLED, SRD8RLED, SRD16RLED		4-, 8-, 16-Bit Dual Edge Triggered Shift Registers with Clock Enable and Synchronous Reset			
Spartan-II, Spartan-IIE	**Virtex, VirtexE**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	N/A	N/A	N/A	Macro

SRL16		16-Bit Shift Register Look-Up-Table (LUT)			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

SRL16_1		16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

SRL16E		16-Bit Shift Register Look-Up-Table (LUT) with Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

SRL16E_1		16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Primitive	Primitive	Primitive	N/A	N/A	N/A

SRLC16		16-Bit Shift Register Look-Up-Table (LUT) with Carry			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

SRLC16_1		16-Bit Shift Register Look-Up-Table (LUT) with Carry and Negative-Edge Clock			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

SRLC16E		16-Bit Shift Register Look-Up-Table (LUT) with Carry and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

SRLC16E_1		16-Bit Shift Register Look-Up-Table (LUT) with Carry, Negative-Clock Edge, and Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N/A	N/A	Primitive	N/A	N/A	N/A

X74_164		8-Bit Serial-In Parallel-Out Shift Register with Active-Low Asynchronous Clear			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_165S		8-Bit Loadable Serial / Parallel-In Parallel-Out Shift Register with Clock Enable			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_194		4-Bit Loadable Bidirectional Serial / Parallel-In Parallel-Out Shift Register			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

X74_195		4-Bit Loadable Serial / Parallel-In Parallel-Out Shift Register			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
N / A	N / A	N / A	Macro	Macro	Macro

Shifters

Shifters are barrel shifters (BRLSHFT) of four and eight bits.

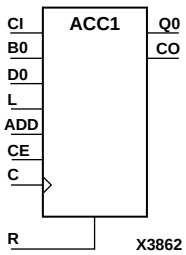
BRLSHFT4, 8		4-, 8-Bit Barrel Shifters			
Spartan-II, Spartan-IIE	**Virtex, Virtex-E**	**Virtex-II, Virtex-II PRO**	**XC9500/XV/XL**	**CoolRunner XPLA3**	**CoolRunner-II**
Macro	Macro	Macro	Macro	Macro	Macro

ACC1 to BUFT, 4, 8, 16

ACC1

1-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



ACC1 can add or subtract a 1-bit unsigned-binary word to or from the contents of a 1-bit data register and store the results in the register. The register can be loaded with a 1-bit word. The synchronous reset (R) has priority over all other inputs and, when High, causes the output to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low. The accumulator is asynchronously cleared, outputs Low, when power is applied. For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Load

When the load input (L) is High, CE is ignored and the data on the input D0 is loaded into the 1-bit register during the Low-to-High clock (C) transition.

Add

When control inputs ADD and CE are both High, the accumulator adds a 1-bit word (B0) and carry-in (CI) to the contents of the 1-bit register. The result is stored in the register and appears on output Q0 during the Low-to-High clock transition. The carry-out (CO) is not registered synchronously with the data output. CO always reflects the accumulation of input B0 and the contents of the register, which allows cascading of ACC1s by connecting CO of one stage to CI of the next stage. In add mode, CO acts as a carry-out, and CO and CI are active-High.

Subtract

When ADD is Low and CE is High, the 1-bit word B0 and CI are subtracted from the contents of the register. The result is stored in the register and appears on output Q0 during the Low-to-High clock transition. The carry-out (CO) is not registered synchronously with the data output. CO always reflects the accumulation of input B0 and the contents of the register, which allows cascading of ACC1s by connecting CO of one stage to CI of the next stage. In subtract mode, CO acts as a borrow, and CO and CI are active-Low.

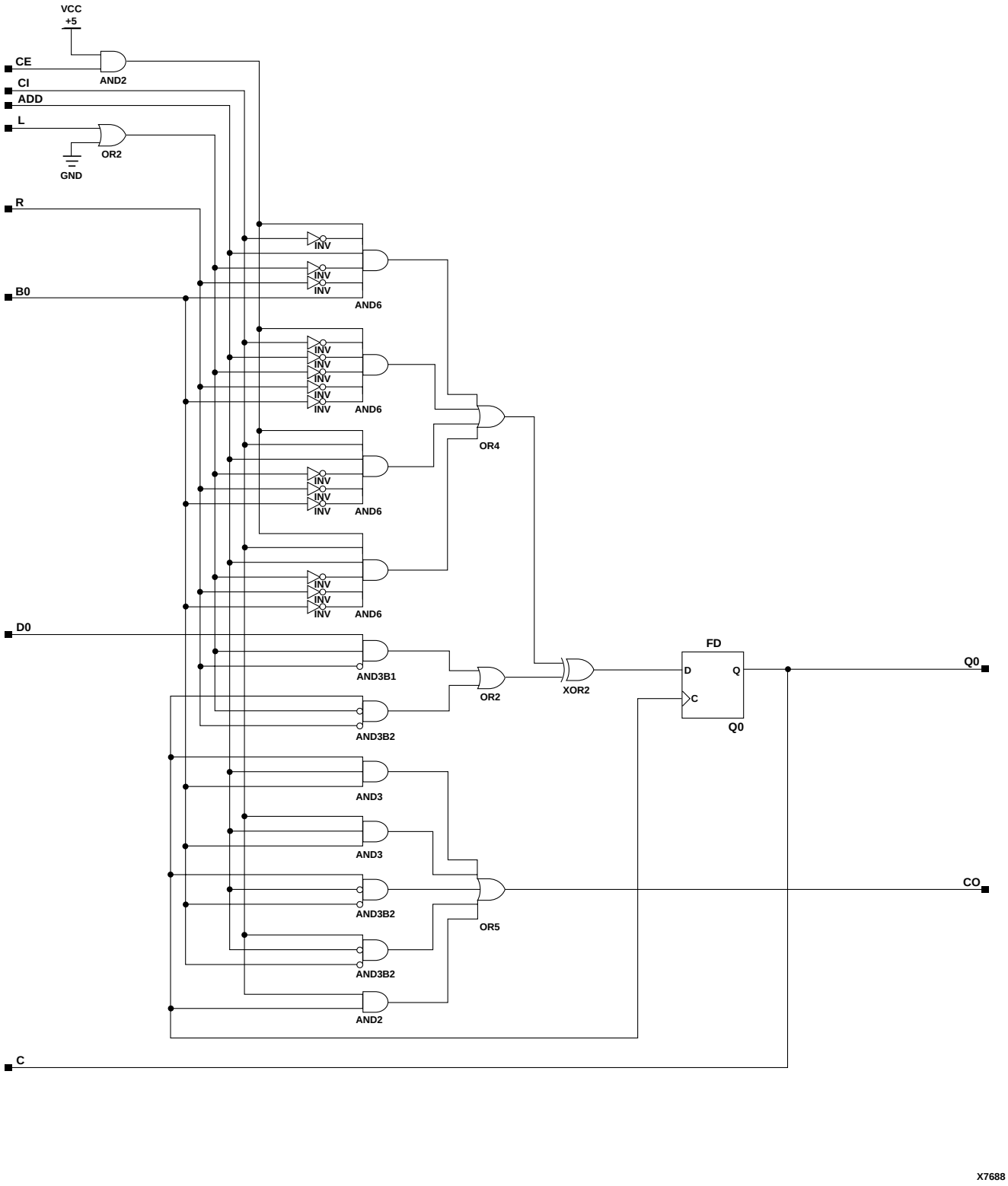
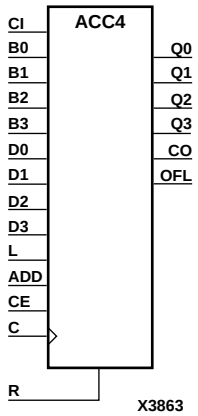


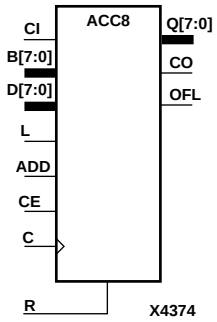
Figure 3-1 ACC1 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

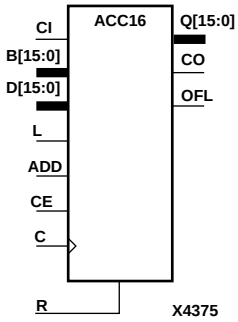
ACC4, 8, 16

4-, 8-, 16-Bit Loadable Cascadable Accumulators with Carry-In, Carry-Out, and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







ACC4, ACC8, ACC16 can add or subtract a 4-, 8-, 16-bit unsigned-binary, respectively or twos-complement word to or from the contents of a 4-, 8-, 16-bit data register and store the results in the register. The register can be loaded with the 4-, 8-, 16-bit word.

The synchronous reset (R) has priority over all other inputs, and when High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

The accumulator is asynchronously cleared, outputs Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Load

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC4 loads the data on inputs D3 – D0 into the 4-bit register. ACC8 loads the data on D7 – D0 into the 8-bit register. ACC16 loads the data on inputs D15 – D0 into the 16-bit register.

Unsigned Binary Versus Twos Complement

ACC4, ACC8, ACC16 can operate, respectively, on either 4-, 8-, 16-bit unsigned binary numbers or 4-, 8-, 16-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when “overflow” occurs. Unsigned binary uses CO, while twos complement uses OFL to determine when “overflow” occurs.

Unsigned Binary Operation

For unsigned binary operation, ACC4 can represent numbers between 0 and 15, inclusive; ACC8 between 0 and 255, inclusive; and ACC16 between 0 and 65535, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder / subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 – B0 for ACC4, B7 – B0 for ACC8, B15 – B0 for ACC16) and the contents of the register. This allows cascading of ACC4s, ACC8s, or ACC16s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows.

```
unsigned overflow = CO XOR ADD
```

Ignore OFL in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, ACC4 can represent numbers between -8 and +7, inclusive; ACC8 between -128 and +127, inclusive; ACC16 between -32768 and +32767, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 – B0 for ACC4, B7 – B0 for ACC8, B15 – B0 for ACC16) and the contents of the register, which allows cascading of ACC4s, ACC8s, or ACC16s by connecting OFL of one stage to CI of the next stage.

Ignore CO in twos-complement operation.

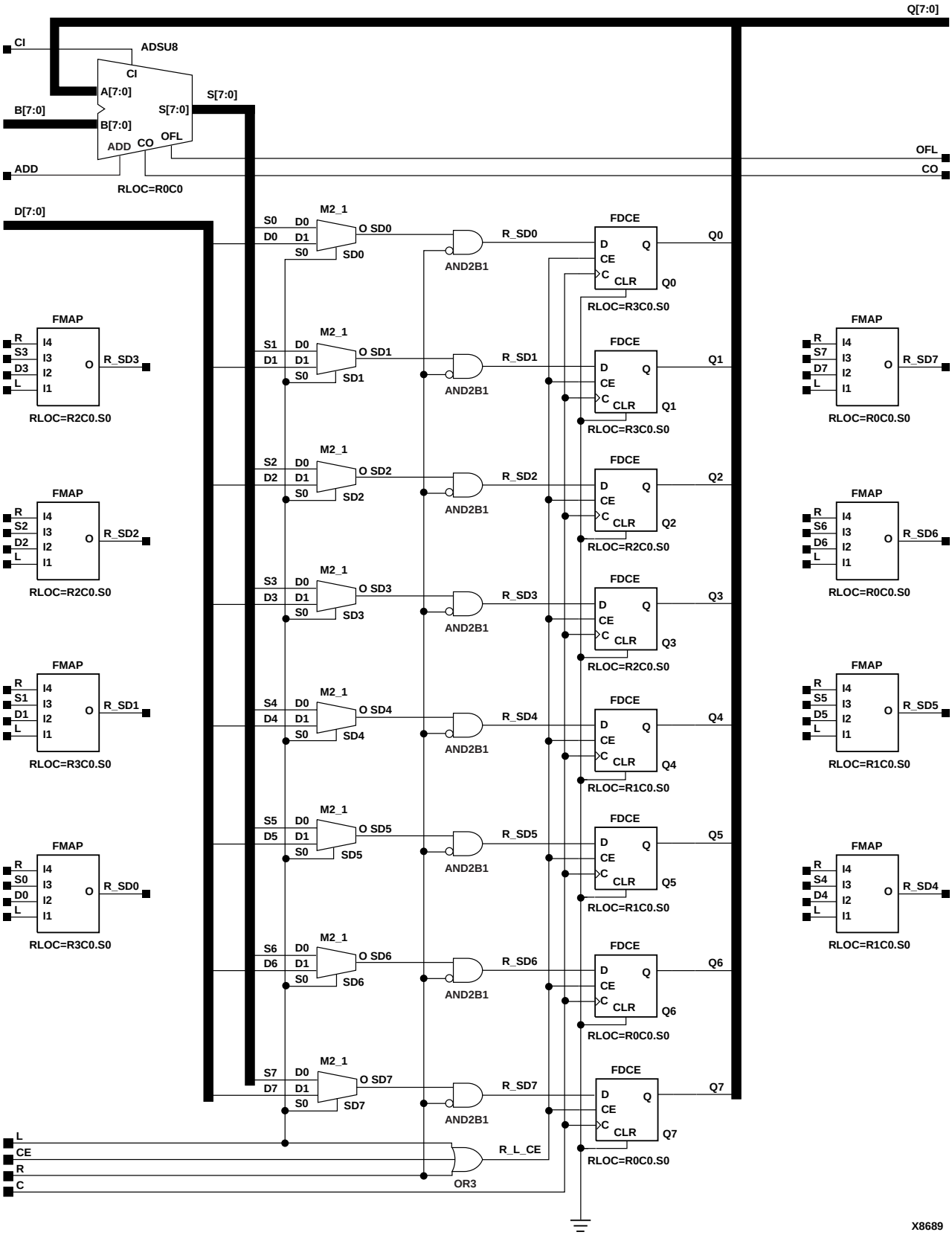


Figure 3-2 ACC8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

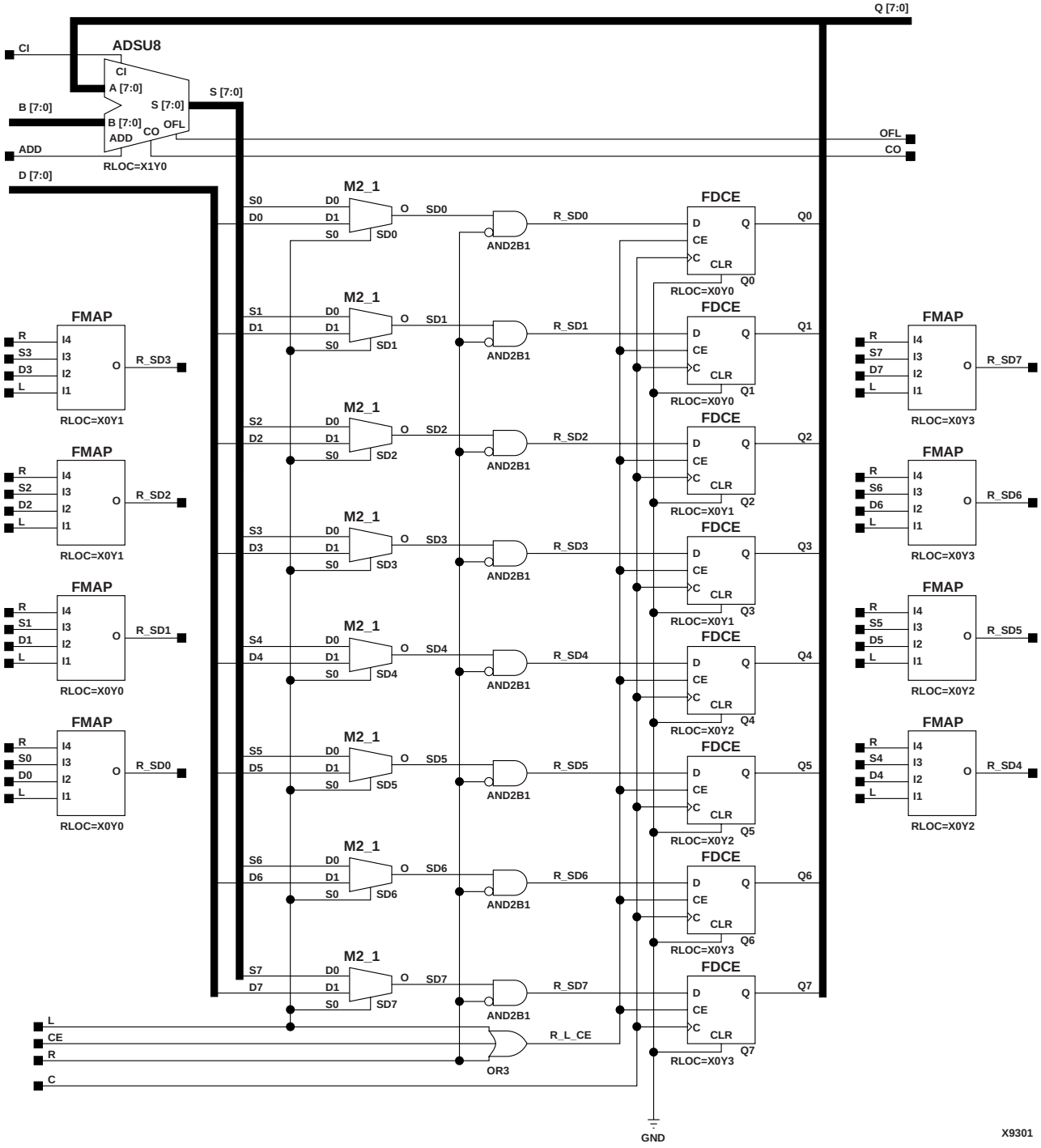


Figure 3-3 ACC8 Implementation Virtex-II, Virtex-II PRO

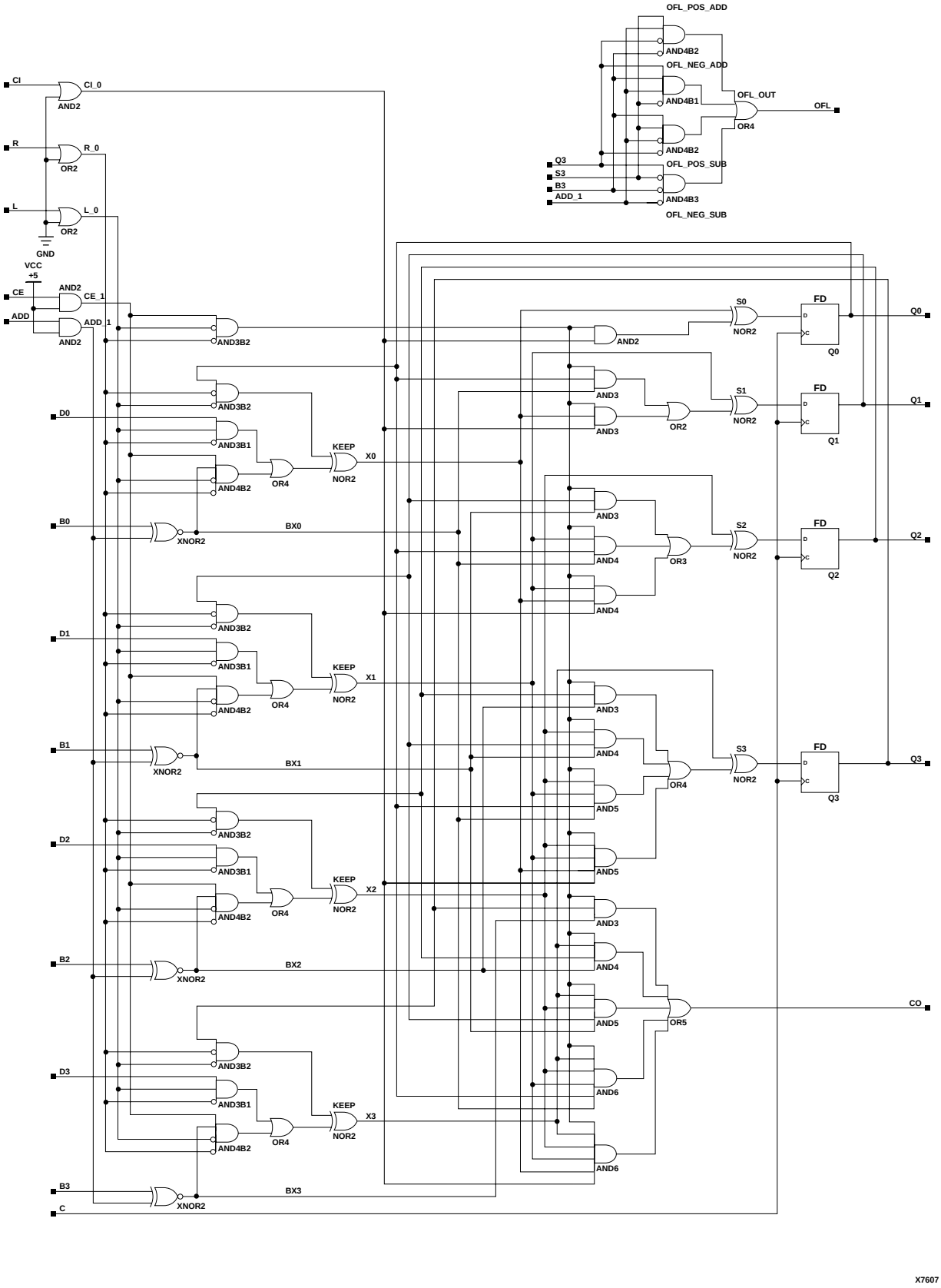


Figure 3-4 ACC4 Implementation XC9500/XV/XL, CoolRunner XPLA3, and

CoolRunner-II

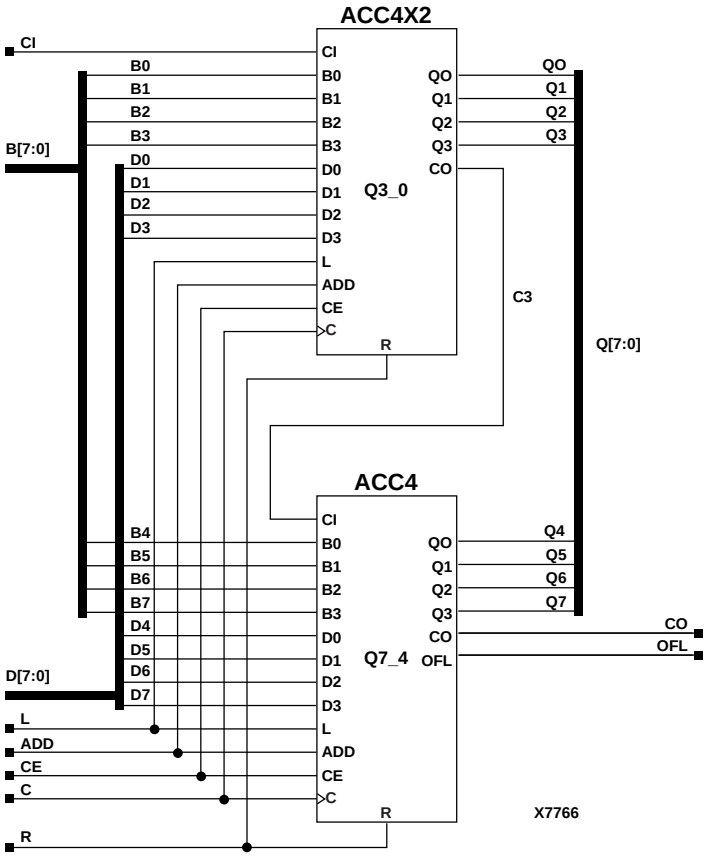
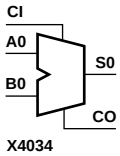


Figure 3-5 ACC8 Implementation XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II

ADD1

1-Bit Full Adder with Carry-In and Carry-Out

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



ADD1 is a cascadable 1-bit full adder with carry-in and carry-out. It adds two 1-bit words (A and B) and a carry-in (CI), producing a binary sum (S0) output and a carry-out (CO).

Inputs			Outputs	
A0	B0	CI	S0	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

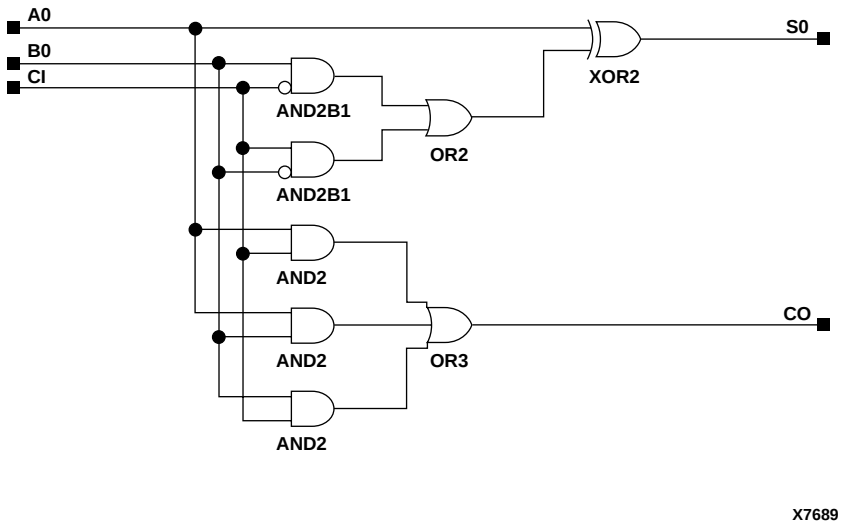
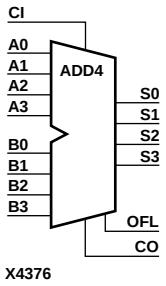


Figure 3-6 ADD1 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

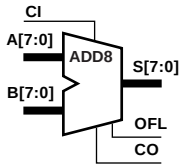
ADD4, 8, 16

4-, 8-, 16-Bit Cascadable Full Adders with Carry-In, Carry-Out, and Overflow

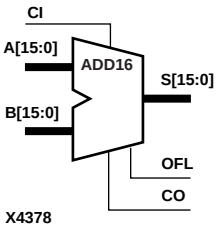
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



X4376



X4377



X4378

ADD4, ADD8, and ADD16 add two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). ADD4 adds A3 – A0, B3 – B0, and CI producing the sum output S3 – S0 and CO (or OFL). ADD8 adds A7 – A0, B7 – B0, and CI, producing the sum output S7 – S0 and CO (or OFL). ADD16 adds A15 – A0, B15 – B0 and CI, producing the sum output S15 – S0 and CO (or OFL).

Unsigned Binary Versus Twos Complement

ADD4, ADD8, ADD16 can operate on either 4-, 8-, 16-bit unsigned binary numbers or 4-, 8-, 16-bit twos-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when “overflow” occurs. Unsigned binary uses CO, while twos-complement uses OFL to determine when “overflow” occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as twos complement, follow the OFL output.

Unsigned Binary Operation

For unsigned binary operation, ADD4 can represent numbers between 0 and 15, inclusive; ADD8 between 0 and 255, inclusive; ADD16 between 0 and 65535, inclusive. CO is active (High) when the sum exceeds the bounds of the adder.

OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, ADD4 can represent numbers between -8 and +7, inclusive; ADD8 between -128 and +127, inclusive; ADD16 between -32768 and +32767, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder.

CO is ignored in twos-complement operation.

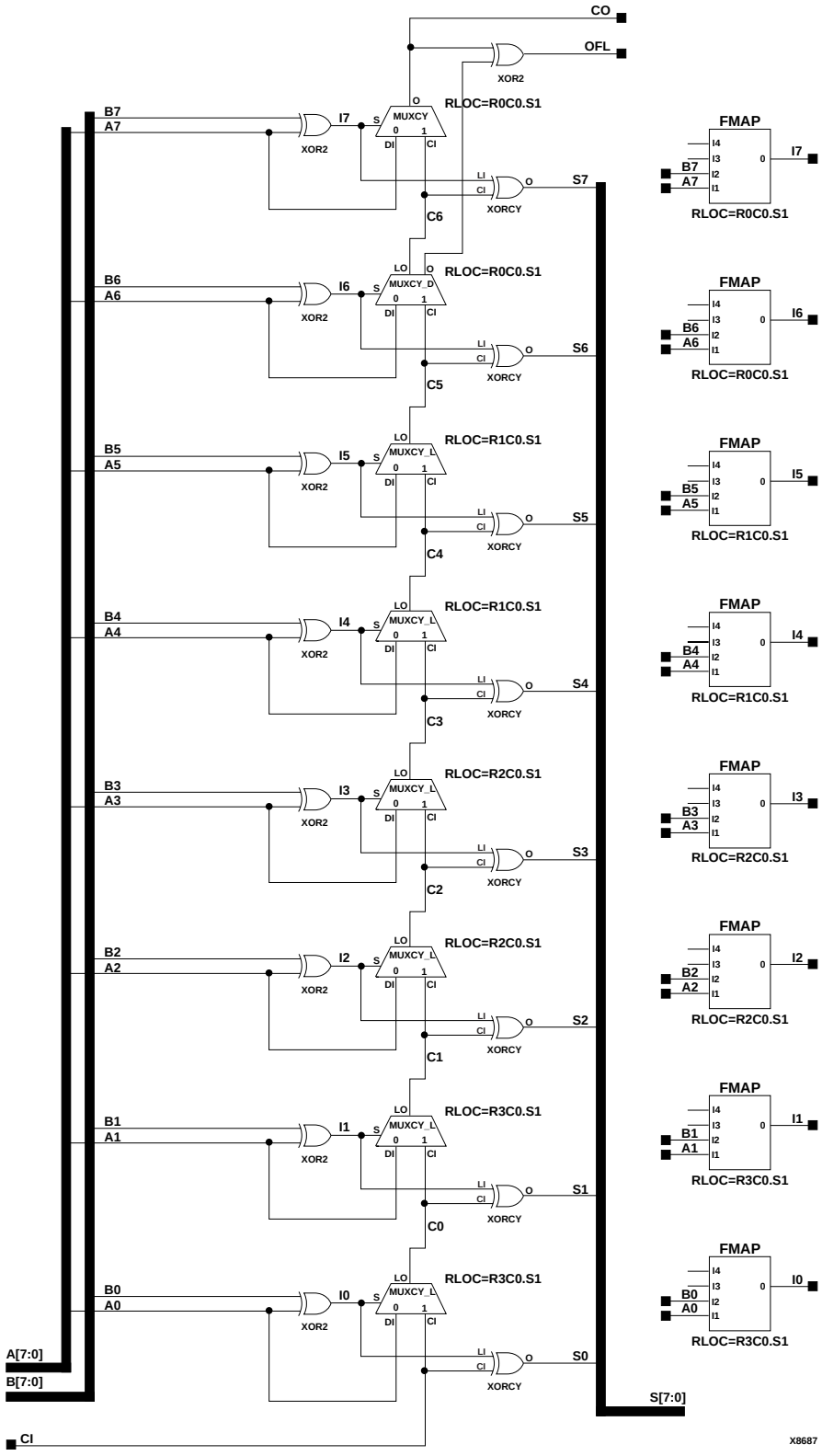


Figure 3-7 ADD8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

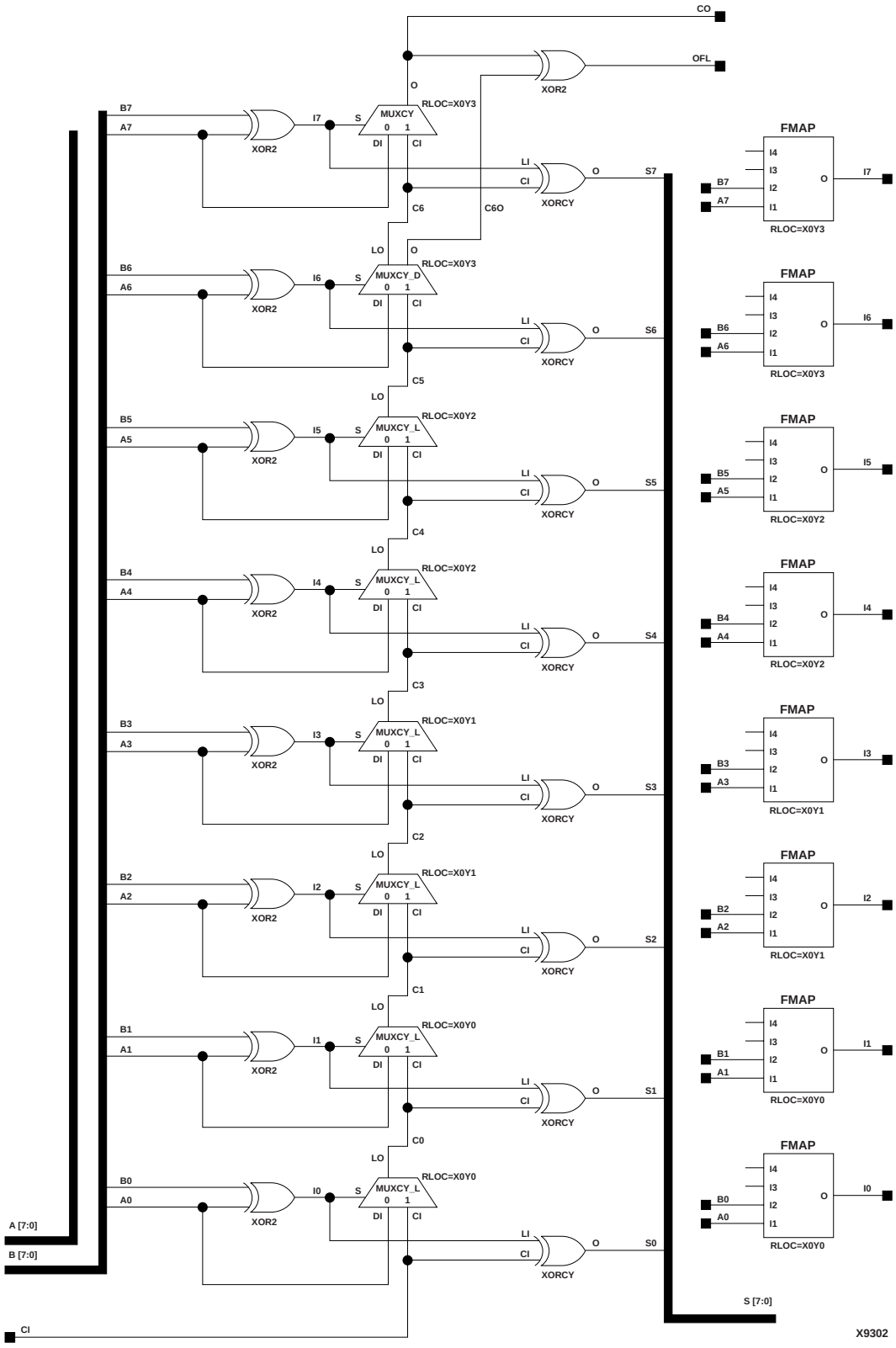


Figure 3-8 ADD8 Implementation Virtex-II, Virtex-II PRO

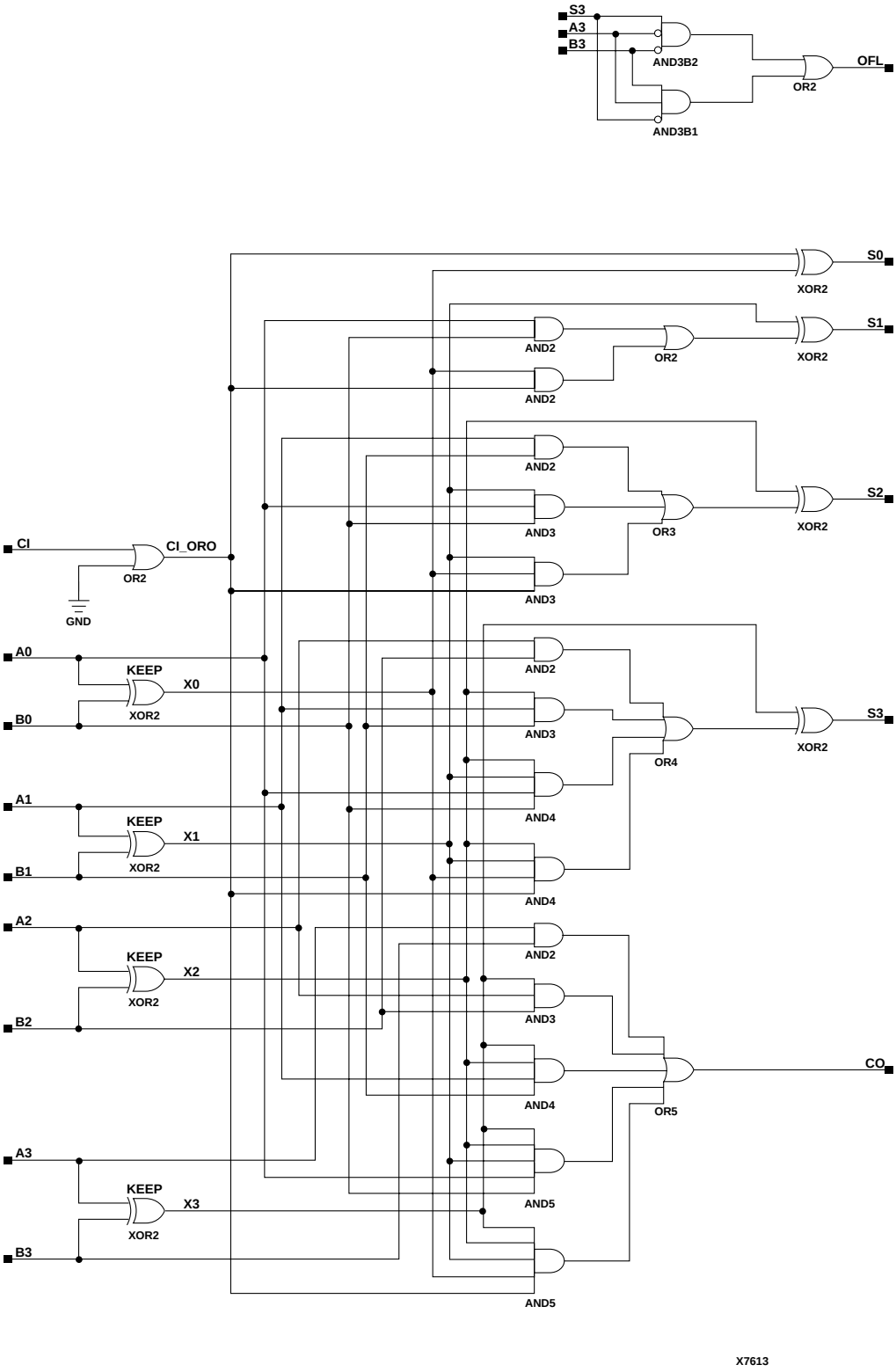


Figure 3-9 ADD4 Implementation XC9500/XV/XL, CoolRunner XPLA3,

CoolRunner-II

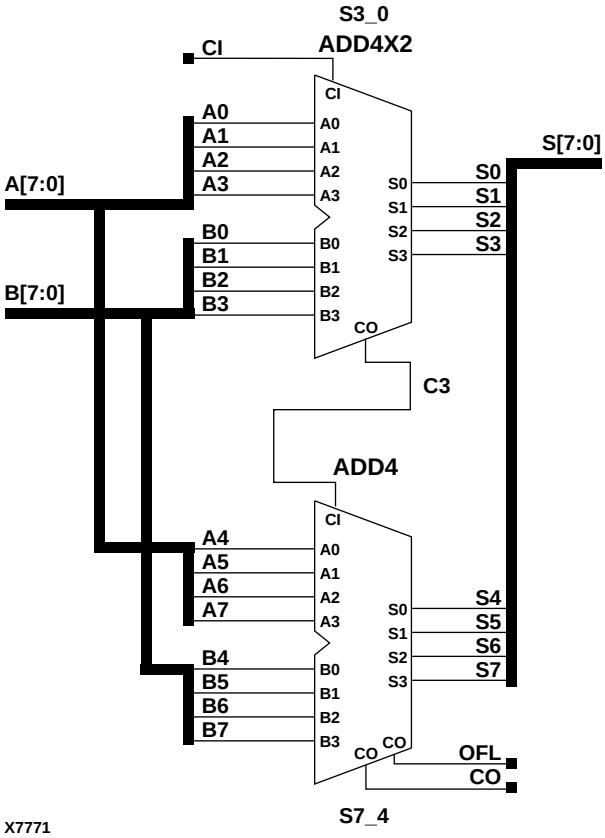
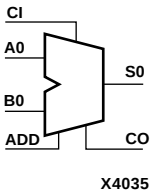


Figure 3-10 ADD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

ADSU1

1-Bit Cascadable Adder/Subtracter with Carry-In and Carry-Out

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro



When the ADD input is High, two 1-bit words (A0 and B0) are added with a carry-in (CI), producing a 1-bit output (S0) and a carry-out (CO). When the ADD input is Low, B0 is subtracted from A0, producing a result (S0) and borrow (CO). In add mode, CO represents a carry-out, and CO and CI are active-High. In subtract mode, CO represents a borrow, and CO and CI are active-Low.

Table 3-1 Add Function, ADD=1

Inputs			Outputs	
A0	B0	CI	S0	CO
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Table 3-2 Subtract Function, ADD=0

Inputs			Outputs	
A0	B0	CI	S0	CO
0	0	0	1	0
0	1	0	0	0
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	1
1	1	1	0	1

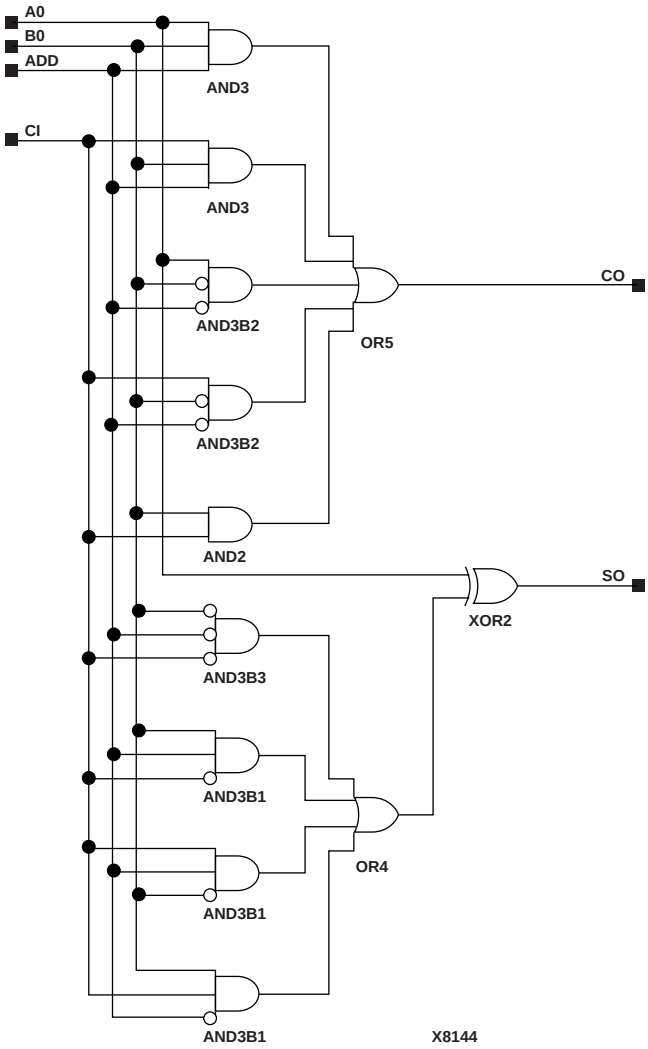
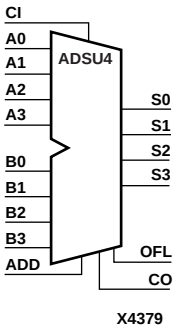


Figure 3-11 ADSU1 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

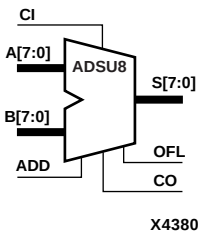
ADSU4, 8, 16

4-, 8-, 16-Bit Cascadable Adders/Subtracters with Carry-In, Carry-Out, and Overflow

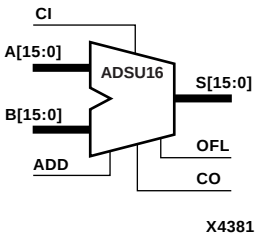
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



X4379



X4380



X4381

When the ADD input is High, ADSU4, ADSU8, and ADSU16 add two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). ADSU4 adds two 4-bit words (A3 – A0 and B3 – B0) and a CI, producing a 4-bit sum output (S3 – S0) and CO or OFL. ADSU8 adds two 8-bit words (A7 – A0 and B7 – B0) and a CI producing, an 8-bit sum output (S7 – S0) and CO or OFL. ADSU16 adds two 16-bit words (A15 – A0 and B15 – B0) and a CI, producing a 16-bit sum output (S15 – S0) and CO or OFL.

When the ADD input is Low, ADSU4, ADSU8, and ADSU16 subtract Bz – B0 from Az– A0, producing a difference output and CO or OFL. ADSU4 subtracts B3 – B0 from A3 – A0, producing a 4-bit difference (S3 – S0) and CO or OFL. ADSU8 subtracts B7 – B0 from A7 – A0, producing an 8-bit difference (S7 – S0) and CO or OFL. ADSU16 subtracts B15 – B0 from A15 – A0, producing a 16-bit difference (S15 – S0) and CO or OFL.

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

ADSU4, ADSU8, and ADSU16 CI and CO pins do not use the CPLD carry chain.

Unsigned Binary Versus Twos Complement

ADSU4, ADSU8, ADSU16 can operate, respectively, on either 4-, 8-, 16-bit unsigned binary numbers or 4-, 8-, 16-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when “overflow” occurs. Unsigned binary uses CO, while twos complement uses OFL to determine when “overflow” occurs.

With adder / subtracters, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated. The following figure shows the ADSU carry-out and overflow boundaries.

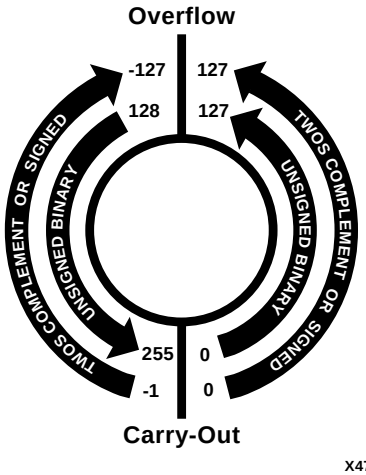


Figure 3-12 ADSU Carry-Out and Overflow Boundaries

Unsigned Binary Operation

For unsigned binary operation, ADSU4 can represent numbers between 0 and 15, inclusive; ADSU8 between 0 and 255, inclusive; ADSU16 between 0 and 65535, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows.

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, ADSU4 can represent numbers between -8 and +7, inclusive; ADSU8 between -128 and +127, inclusive; ADSU16 between -32768 and +32767, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High.

CO is ignored in twos-complement operation.

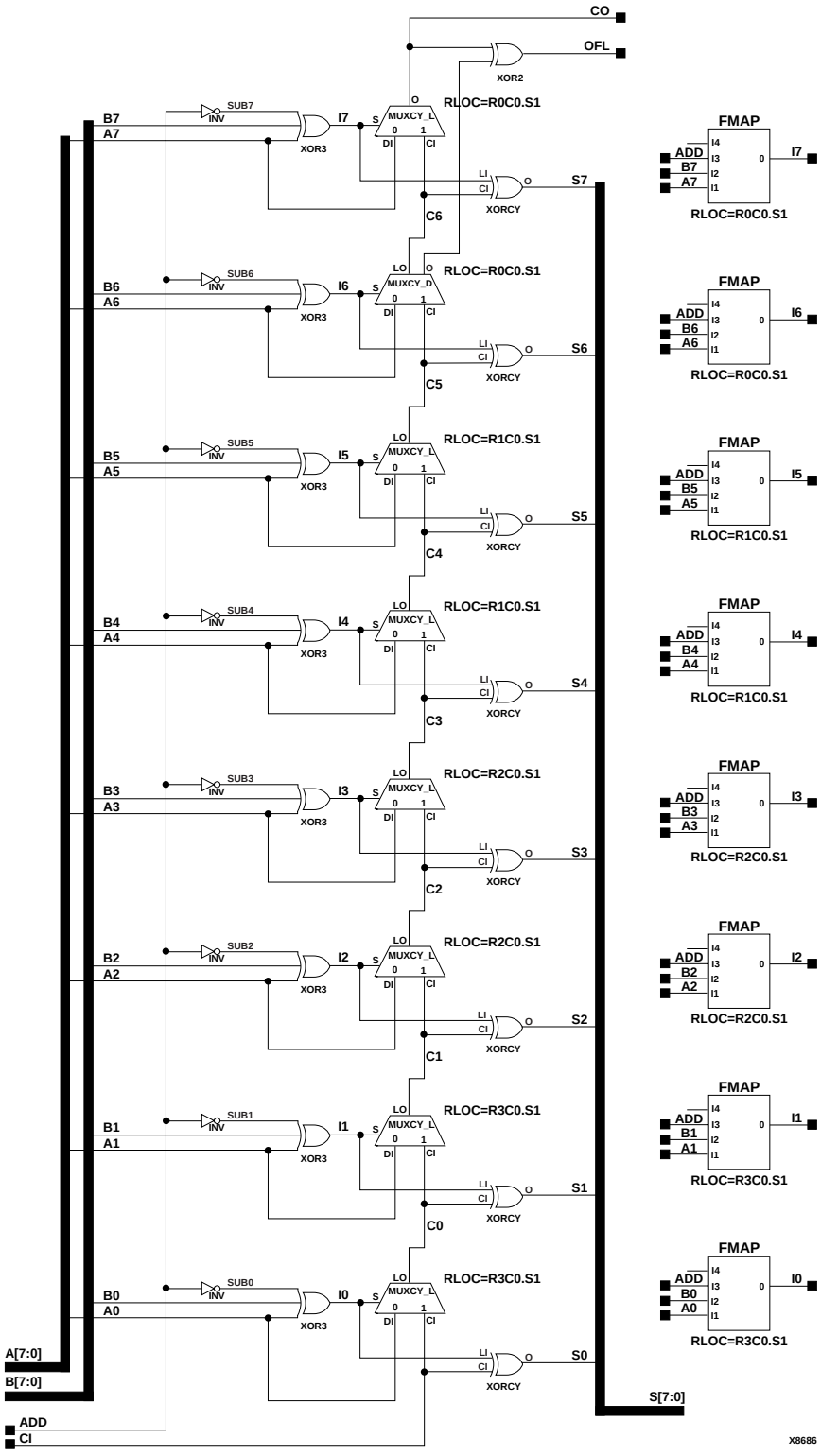


Figure 3-13 ADSU8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

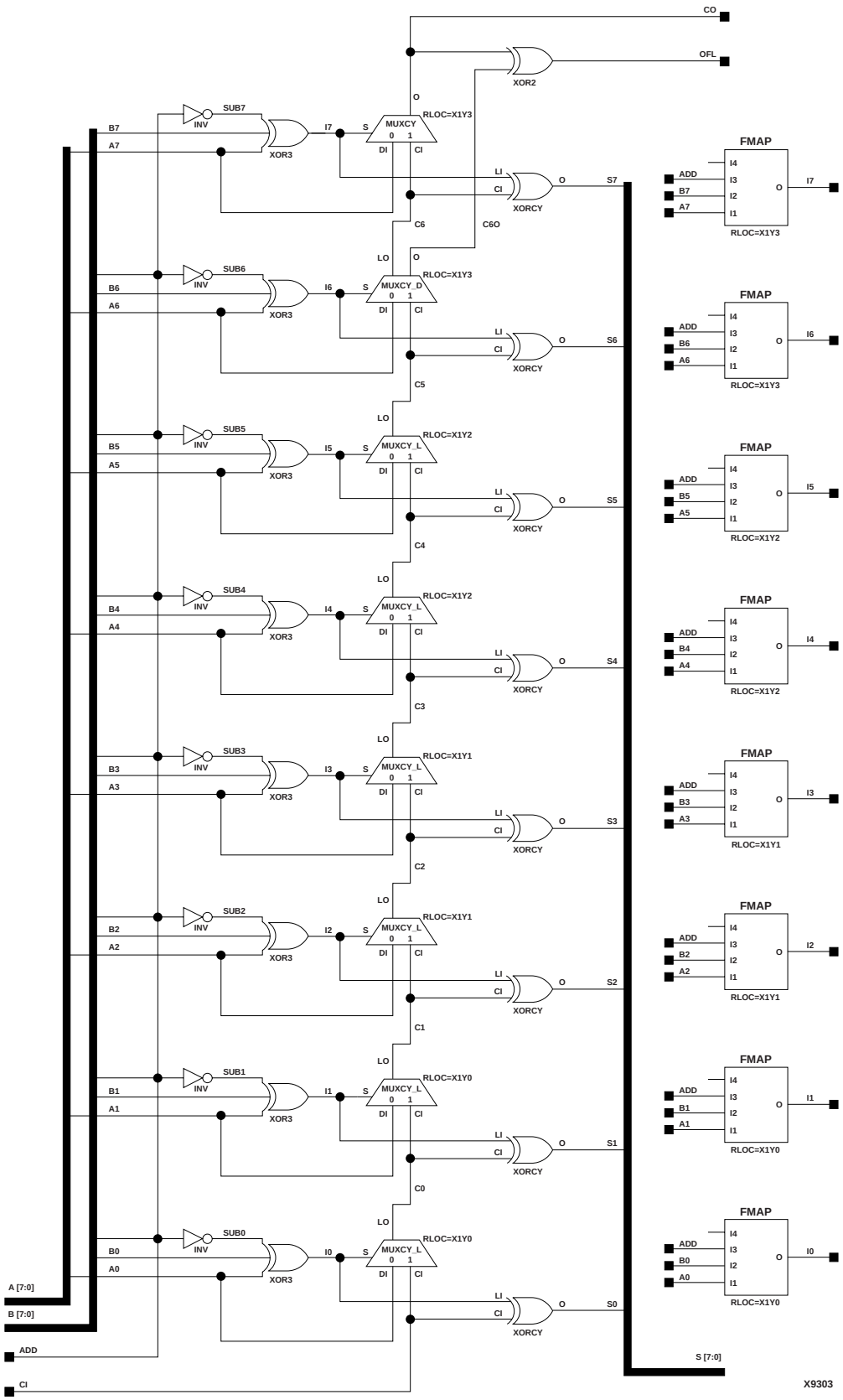


Figure 3-14 ADSU8 Implementation Virtex-II, Virtex-II PRO

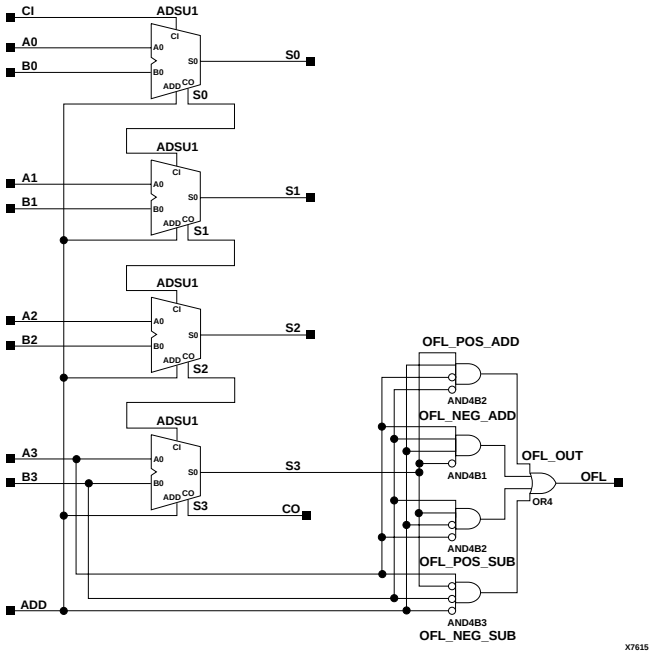


Figure 3-15 ADSU4 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

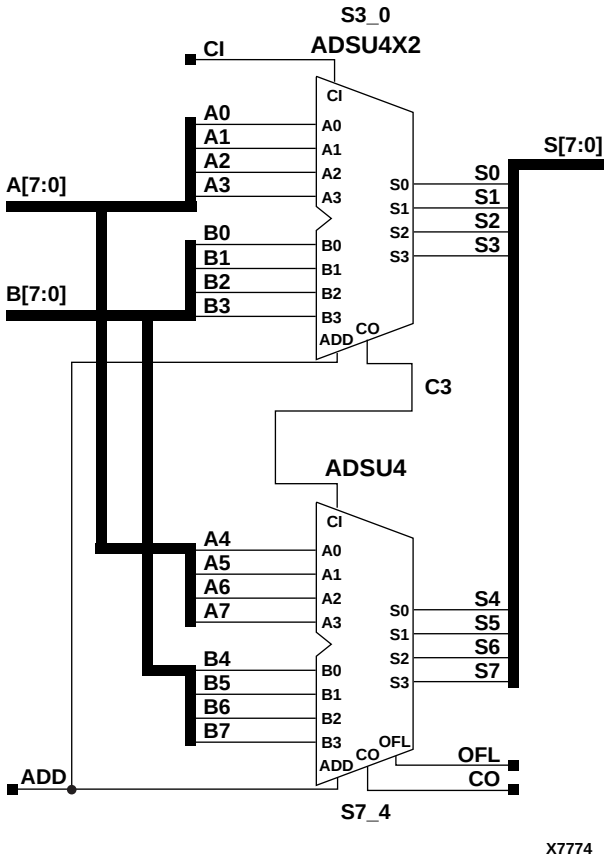


Figure 3-16 ADSU8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

AND2-9

2- to 9-Input AND Gates with Inverted and Non-Inverted Inputs

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
AND2, AND2B1, AND2B2, AND3, AND3B1, AND3B2, AND3B3, AND4, AND4B1, AND4B2, AND4B3, AND4B4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND5, AND5B1, AND5B2, AND5B3, AND5B4, AND5B5	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND6, AND7, AND8, AND9	Macro	Macro	Macro	Primitive	Primitive	Primitive

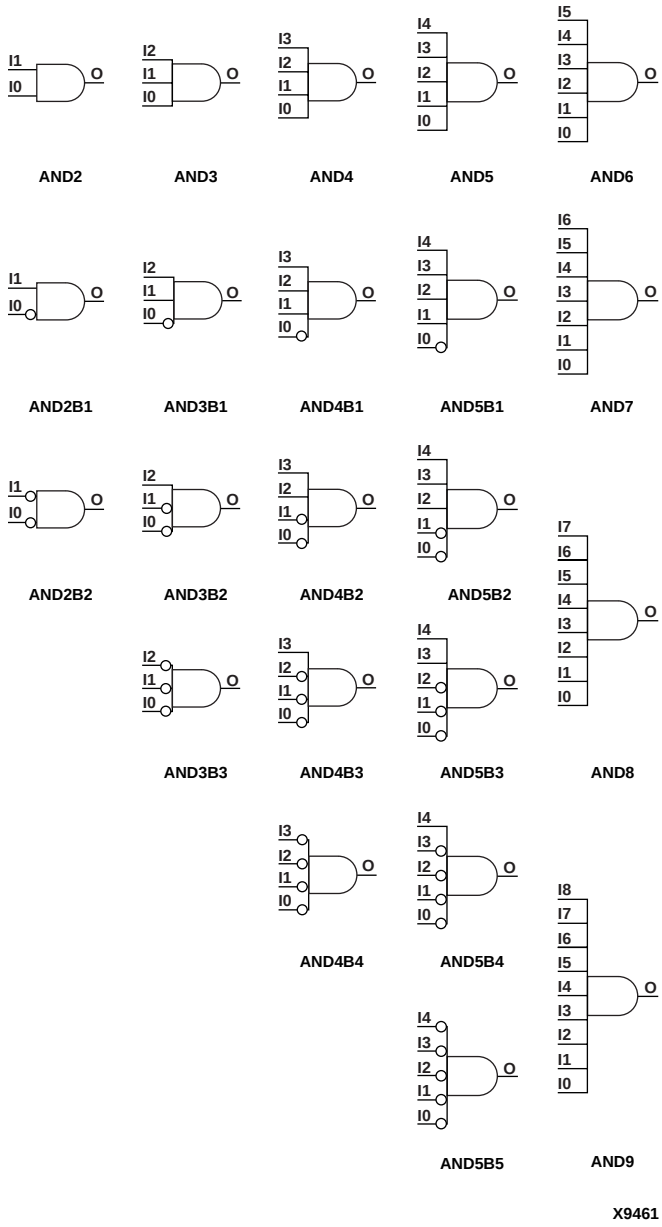


Figure 3-17 AND Gate Representations

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs are available with only non-inverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource in Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, replace functions with unused inputs with functions having the appropriate number of inputs.

See "AND12, 16" for information on additional AND functions for Virtex, Virtex-E, Virtex-II, and Virtex-II PRO.

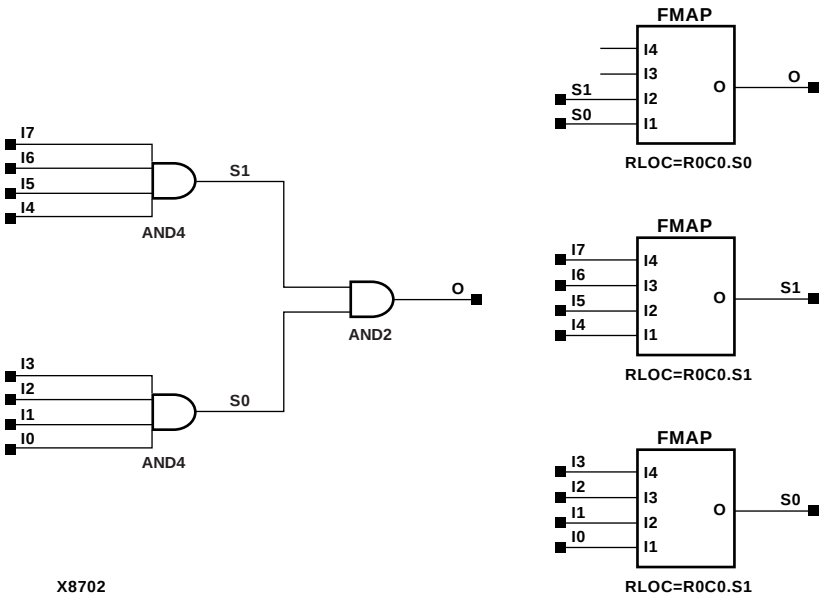


Figure 3-18 AND8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

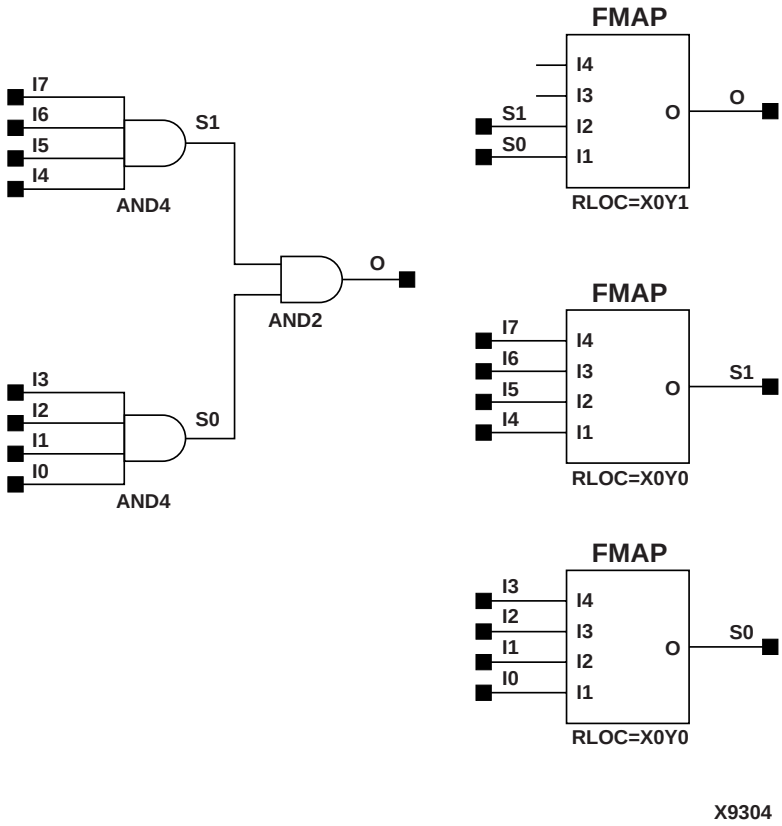
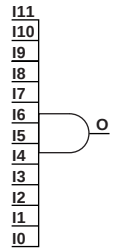


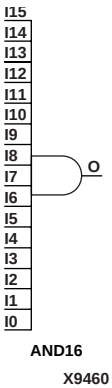
Figure 3-19 AND8 Implementation Virtex-II, Virtex-II PRO

AND12, 16

12- and 16-Input AND Gates with Non-Inverted Inputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A





AND12 and AND16 functions are performed in the Configurable Logic Block (CLB) function generator.

The 12- and 16-input AND functions are available only with non-inverting inputs. To invert all of some inputs, use external inverters.

See "AND2-9" for information on more AND functions.

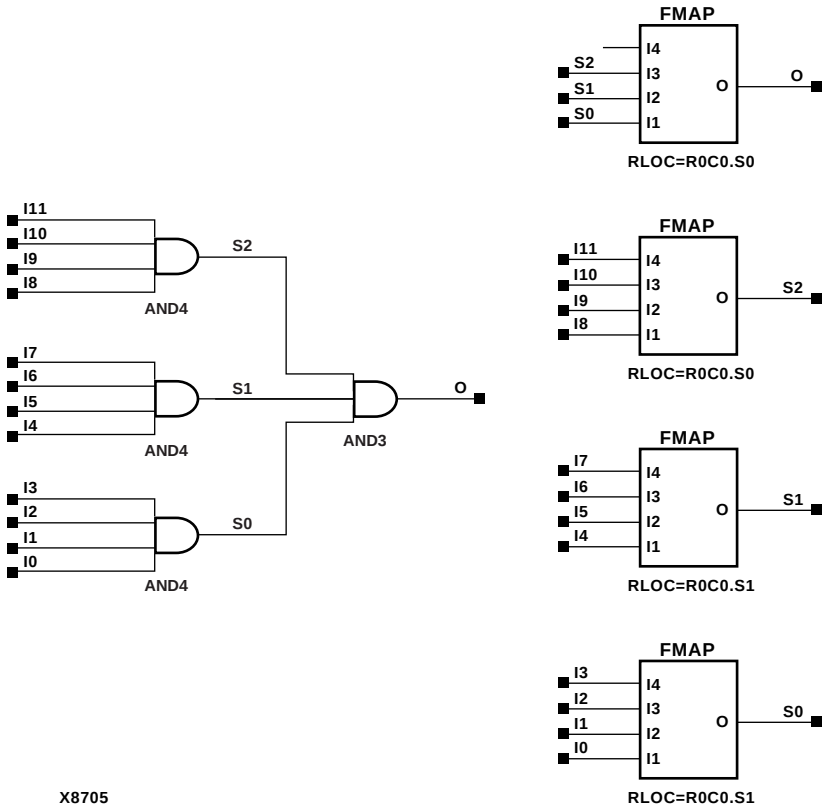


Figure 3-20 AND12 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

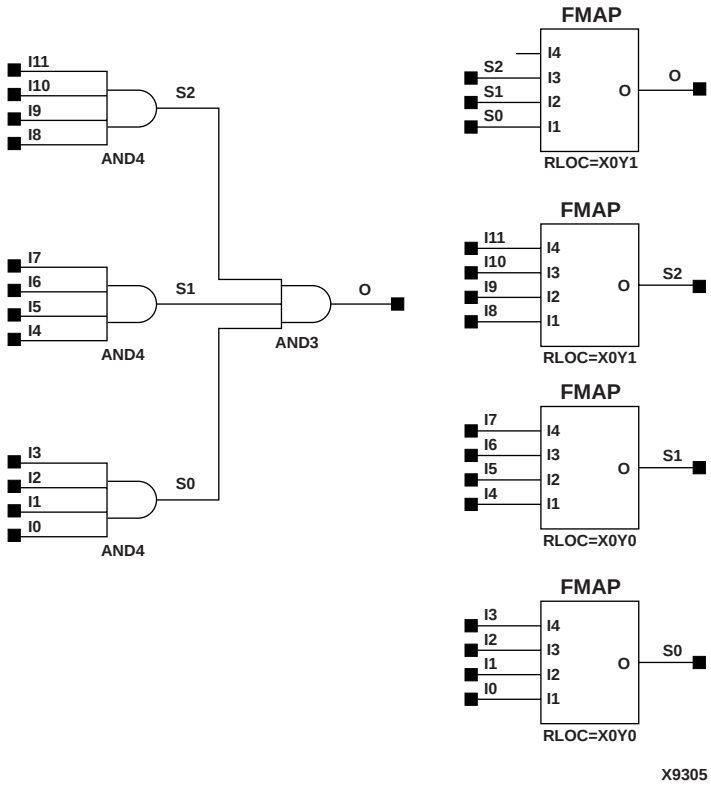


Figure 3-21 AND12 Implementation Virtex-II, Virtex-II PRO

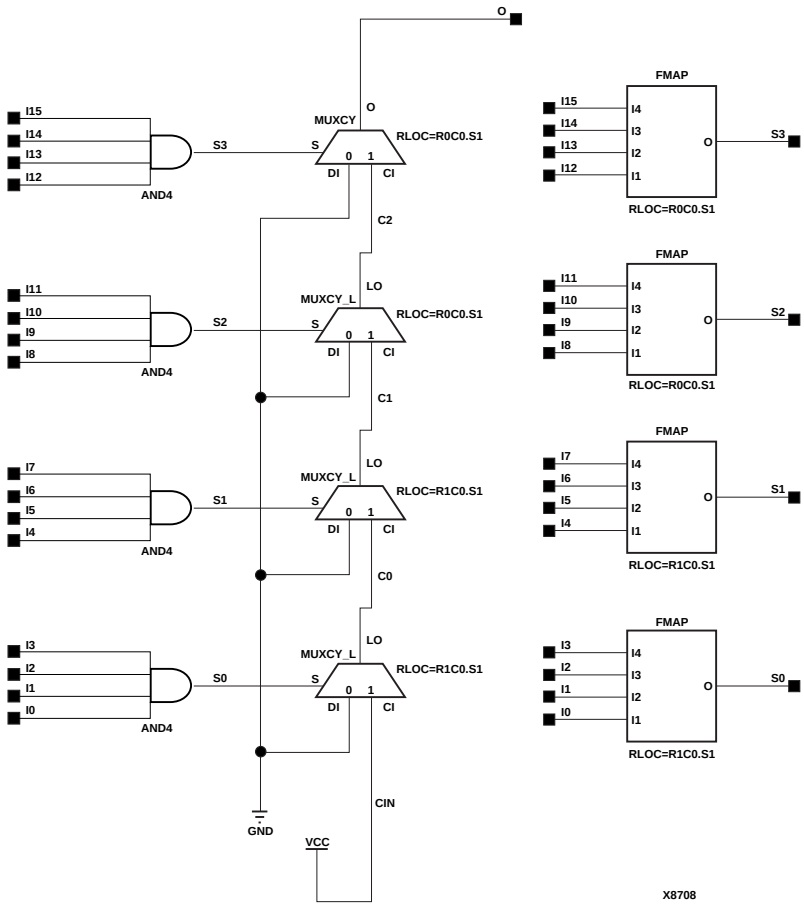


Figure 3-22 AND16 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

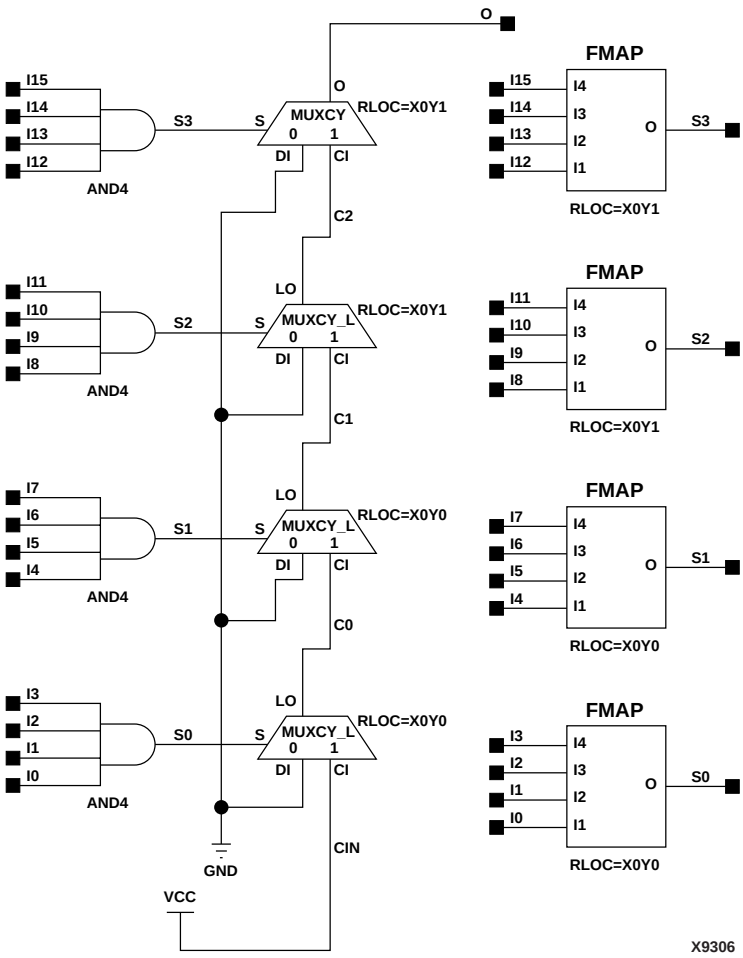
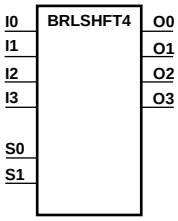


Figure 3-23 AND16 Implementation Virtex-II, Virtex-II PRO

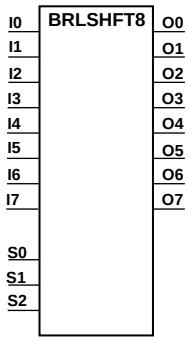
BRLSHFT4, 8

4-, 8-Bit Barrel Shifters

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



X3856



X3857

BRLSHFT4, a 4-bit barrel shifter, can rotate four inputs (I3 – I0) up to four places. The control inputs (S1 and S0) determine the number of positions, from one to four, that the data is rotated. The four outputs (O3 – O0) reflect the shifted data inputs.

BRLSHFT8, an 8-bit barrel shifter, can rotate the eight inputs (I7 – I0) up to eight places. The control inputs (S2 – S0) determine the number of positions, from one to eight, that the data is rotated. The eight outputs (O7 – O0) reflect the shifted data inputs.

Table 3-3 BRLSHFT4 Truth Table

Inputs						Outputs			
S1	S0	I0	I1	I2	I3	O0	O1	O2	O3
0	0	a	b	c	d	a	b	c	d
0	1	a	b	c	d	b	c	d	a
1	0	a	b	c	d	c	d	a	b
1	1	a	b	c	d	d	a	b	c

Table 3-4 BRLSHFT8 Truth Table

Inputs										Outputs							
S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	O0	O1	O2	O3	O4	O5	O6	O7
0	0	0	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
0	0	1	a	b	c	d	e	f	g	h	b	c	d	e	f	g	h	a
0	1	0	a	b	c	d	e	f	g	h	c	d	e	f	g	h	a	b
0	1	1	a	b	c	d	e	f	g	h	d	e	f	g	h	a	b	c
1	0	0	a	b	c	d	e	f	g	h	e	f	g	h	a	b	c	d
1	0	1	a	b	c	d	e	f	g	h	f	g	h	a	b	c	d	e
1	1	0	a	b	c	d	e	f	g	h	g	h	a	b	c	d	e	f
1	1	1	a	b	c	d	e	f	g	h	h	a	b	c	d	e	f	g

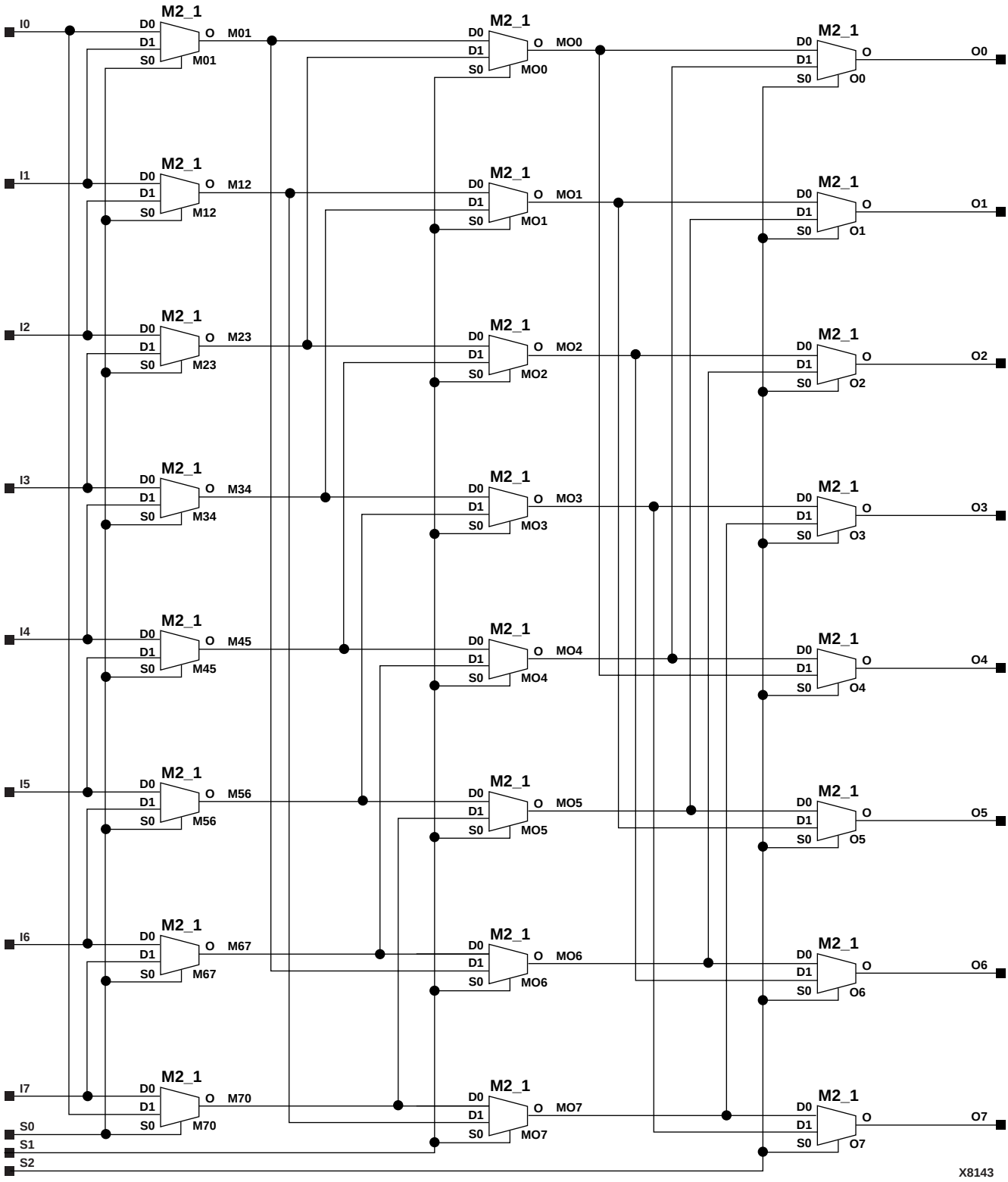
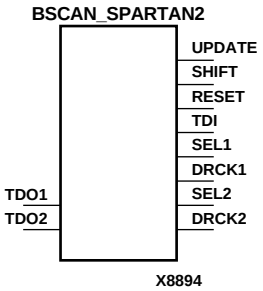


Figure 3-24 BRLSHFT8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

BSCAN_SPARTAN2

Spartan-II Boundary Scan Logic Control Circuit

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	N/A	N/A	N/A	N/A	N/A



The BSCAN_SPARTAN2 symbol creates internal boundary scan chains in a Spartan-II device. The 4-pin JTAG interface (TDI, TDO, TCK, and TMS) are dedicated pins in Spartan-II. To use normal JTAG for boundary scan purposes, just hook up the JTAG pins to the port and go. The pins on the BSCAN_SPARTAN2 symbol do not need to be connected, unless those special functions are needed to drive an internal scan chain.

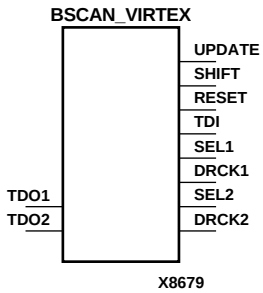
A signal on the TDO1 input is passed to the external TDO output when the USER1 instruction is executed; the SEL1 output goes High to indicate that the USER1 instruction is active.The DRCK1 output provides USER1 access to the data register clock (generated by the TAP controller). The TDO2 and SEL2 pins perform a similar function for the USER2 instruction and the DRCK2 output provides USER2 access to the data register clock (generated by the TAP controller). The RESET, UPDATE, and SHIFT pins represent the decoding of the corresponding state of the boundary scan internal state machine. The TDI pin provides access to the TDI signal of the JTAG port in order to shift data into an internal scan chain.

Note For specific information on boundary scan for an architecture, see *The Programmable Logic Data Book.*

BSCAN_VIRTEX

Virtex Boundary Scan Logic Control Circuit

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	Primitive	N/A	N/A	N/A	N/A



The BSCAN_VIRTEX symbol is used to create internal boundary scan chains in a Virtex or Virtex- E device. The 4-pin JTAG interface (TDI, TDO, TCK, and TMS) are dedicated pins in Virtex and Virtex-E. To use normal JTAG for boundary scan purposes, just hook up the JTAG pins to the port and go. The pins on the BSCAN_VIRTEX symbol do not need to be connected, unless those special functions are needed to drive an internal scan chain.

Note For Virtex-II and Virtex-II PRO, see "BSCAN_VIRTEX2".

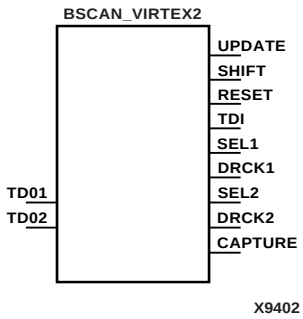
A signal on the TDO1 input is passed to the external TDO output when the USER1 instruction is executed; the SEL1 output goes High to indicate that the USER1 instruction is active.The DRCK1 output provides USER1 access to the data register clock (generated by the TAP controller). The TDO2 and SEL2 pins perform a similar function for the USER2 instruction and the DRCK2 output provides USER2 access to the data register clock (generated by the TAP controller). The RESET, UPDATE, and SHIFT pins represent the decoding of the corresponding state of the boundary scan internal state machine. The TDI pin provides access to the TDI signal of the JTAG port in order to shift data into an internal scan chain.

Note For specific information on boundary scan for an architecture, see *The Programmable Logic Data Book.*

BSCAN_VIRTEX2

Virtex-II Boundary Scan Logic Control Circuit

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



BSCAN_VIRTEX2 provides access to the BSCAN sites on a Virtex-II or Virtex-II PRO device. It is used to create internal boundary scan chains. The 4-pin JTAG interface (TDI, TDO, TCK, and TMS) are dedicated pins in Virtex-II and Virtex-II PRO. To use normal JTAG for boundary scan purposes, just hook up the JTAG pins to the port and go. The pins on the BSCAN_VIRTEX2 symbol do not need to be connected, unless those special functions are needed to drive an internal scan chain.

Note For Virtex and Virtex-E, see "BSCAN_VIRTEX".

A signal on the TDO1 input is passed to the external TDO output when the USER1 instruction is executed; the SEL1 output goes High to indicate that the USER1 instruction is active.The DRCK1 output provides USER1 access to the data register clock (generated by the TAP controller). The TDO2 and SEL2 pins perform a similar function for the USER2 instruction and the DRCK2 output provides USER2 access to the data register clock (generated by the TAP controller). The RESET, UPDATE, SHIFT, and CAPTURE pins represent the decoding of the corresponding state of the boundary scan internal state machine. The TDI pin provides access to the TDI signal of the JTAG port in order to shift data into an internal scan chain.

Note For specific information on boundary scan for an architecture, see *The Programmable Logic Data Book.*

BUF

General-Purpose Buffer

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

X9444

BUF is a general purpose, non-inverting buffer.

In Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, BUF is usually not necessary and is removed by the partitioning software (MAP). The BUF element can be preserved for reducing the delay on a high fan-out net, for example, by splitting the net and reducing capacitive loading. In this case, the buffer is preserved by attaching an X (explicit) attribute to both the input and output nets of the BUF.

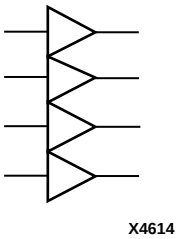
In XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, BUF is usually removed, unless you inhibit optimization by applying the OPT=OFF attribute to the BUF symbol or by using the LOGIC_OPT=OFF global attribute.

BUF4, 8, 16

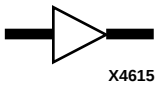
General-Purpose Buffers

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro

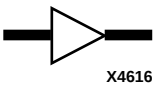
BUF4



BUF8



BUF16



BUF4, 8, 16 are general purpose, non-inverting buffers.

In XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, BUF4, BUF8, and BUF16 are usually removed, unless you inhibit optimization by applying the OPT=OFF attribute to the BUF4, BUF8, or BUF16 symbol or by using the LOGIC_OPT=OFF global attribute.

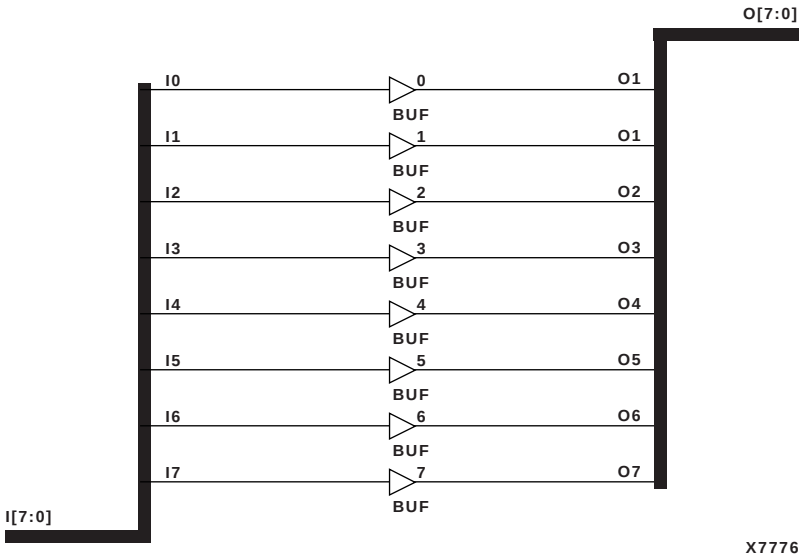
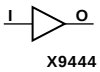


Figure 3-25 BUF8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

BUFCF

Fast Connect Buffer

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



X9444

BUFCF is a single fast connect buffer used to connect the outputs of the LUTs and some dedicated logic directly to the input of another LUT. Using this buffer implies CLB packing. No more than four LUTs may be connected together as a group.

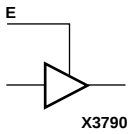
BUFE, 4, 8, 16

Internal 3-State Buffers with Active High Enable

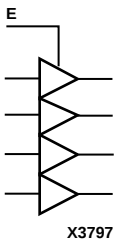
Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
BUFE	Primitive	Primitive	Primitive	Primitive*	Primitive	Primitive
BUFE4, BUFE8, BUFE16	Macro	Macro	Macro	Macro*	Macro	Macro

* not supported for XC9500XL and XC9500XV devices

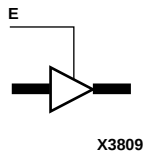
BUFE



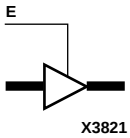
BUFE4



BUFE8



BUFE16



BUFE, BUFE4, BUFE8, and BUFE16 are single or multiple 3-state buffers with inputs I, I3 – I0, I7 – I0, and I15 – I0, respectively; outputs O, O3 – O0, O7 – O0, and O15 – O0, respectively; and active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is high impedance (Z state or Off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures.

The outputs of separate BUFE symbols can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any one time. If none of the E inputs is active-High, a “weak-keeper” circuit (Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO) keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it.

For XC9500/XVdevices, BUFE output nets assume the High logic level when all connected BUFE/BUFT buffers are disabled. On-chip 3-state multiplexing is not available in XC9500XL devices.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, BUFE elements need a PULLUP element connected to their output. NGDBuild inserts a PULLUP element if one is not connected.

Inputs		Outputs
E	I	O
0	X	Z
1	1	1
1	0	0

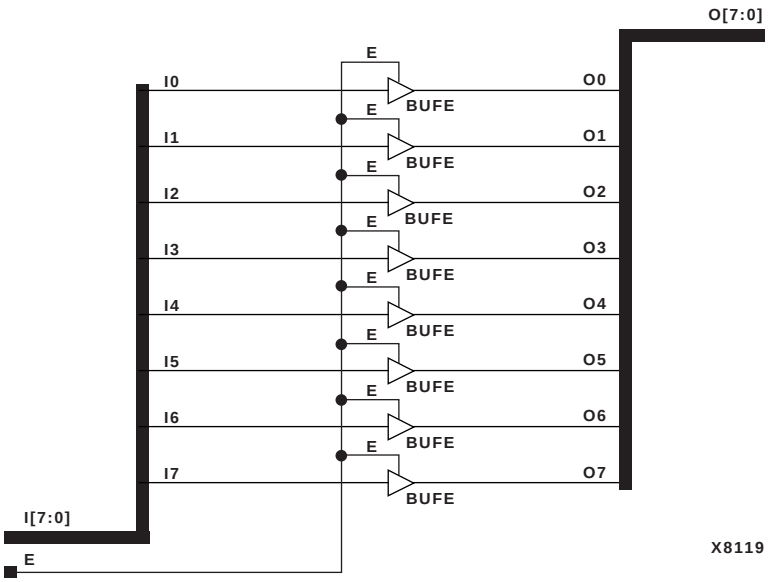
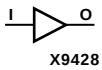


Figure 3-26 BUFE8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

BUFG

Global Clock Buffer

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive



BUFG, an architecture-independent global buffer, distributes high fan-out clock signals throughout a PLD device. The Xilinx implementation software converts each BUFG to an appropriate type of global buffer for the target PLD device. To use a specific type of buffer, instantiate it manually.

To use a BUFG in a schematic, connect the input of the BUFG symbol to the clock source. Depending on the target PLD family, the clock source can be an external PAD symbol, an IBUF symbol, or internal logic. For a negative-edge clock input, insert an INV (inverter) symbol between the BUFG output and the clock input. The inversion is implemented at the Configurable Logic Block (CLB) or Input Output Block (IOB) clock pin.

XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II

Consult the device data sheet for the number of available global pins. For these architectures BUFG is always implemented using an IOB. Connect the input of BUFG to an IPAD or an IOPAD that represents an external signal source. Each BUFG can drive any number of register clocks in a design. The output of a BUFG may also be used as an ordinary input signal to other logic elsewhere in the design.

Virtex, Virtex-E, Spartan-II, Spartan-IIE

In Virtex, Virtex-E, Spartan-II, and Spartan-IIE, the BUFG cannot be driven directly from a pad. It can be driven from an IBUFG to indicate to use the dedicated pin (GCLKIOB pin) or from an internal driver to create an internal clock. BUFG can also be driven with an IBUF to represent an externally driven clock that does not use the dedicated pin.

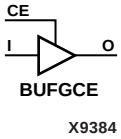
Virtex-II, Virtex-II PRO

Virtex-II and Virtex-II PRO clock buffers are multiplexed clock buffers. In Virtex-II and Virtex-II PRO, a BUFG is implemented using a BUFGMUX with the S input tied high and I0 unused.

BUFGCE

Global Clock MUX Buffer with Clock Enable and Output State 0

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



BUFGCE is a multiplexed global clock buffer with a single gated input. Its O output is "0" when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Inputs		Outputs
I	CE	O
X	0	0
I	1	I

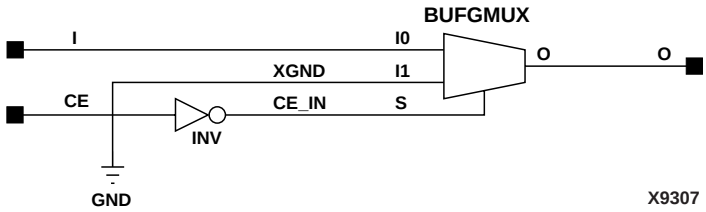
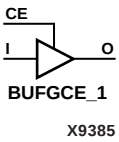


Figure 3-27 BUFGCE Implementation Virtex-II, Virtex-II PRO

BUFGCE_1

Global Clock MUX Buffer with Clock Enable and Output State 1

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



BUFGCE_1 is a multiplexed global clock buffer with a single gated input. Its O output is High (1) when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Inputs		Outputs
I	CE	O
X	0	1
I	1	I

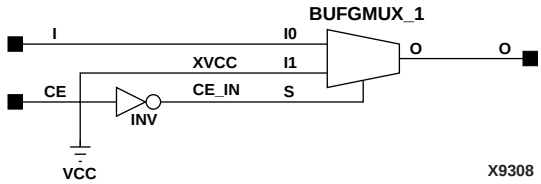
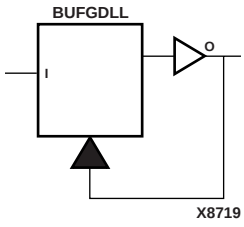


Figure 3-28 BUFGCE_1 Implementation Virtex-II, Virtex-II PRO

BUFGDLL

Clock Delay Locked Loop Buffer

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



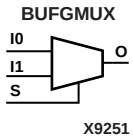
BUFGDLL is a special purpose clock delay locked loop buffer for clock skew management. It is provided as a user convenience for the most frequently used configuration of elements for clock skew management. Internally, it consists of an IBUFG driving the CLKIN pin of a CLKDLL followed by a BUFG that is driven by the CLK0 pin of the CLKDLL. Because BUFGDLL already contains an input buffer (IBUFG), it can only be driven by a top-level port (IPAD).

Any DUTY_CYCLE_CORRECTION attribute on a BUFGDLL applies to the underlying CLKDLL symbol.

BUFGMUX

Global Clock MUX Buffer with Output State 0

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



BUFGMUX is a multiplexed global clock buffer that can select between two input clocks I0 and I1. When the select input (S) is Low, the signal on I0 is selected for output (O). When the select input (S) is High, the signal on I1 is selected for output.

BUFGMUX and BUFGMUX_1 are distinguished by which state the output assumes when it switches between clocks in response to a change in its select input. BUGFMUX0 assumes output state 0 and BUFGMUX_1 assumes output state 1.

Using a BUFGMUX element in your design may cause inaccurate simulation if all the following conditions occur: both clock inputs (I0 and I1) are used, GSR is activated during simulation (after simulation time ‘0’), and the secondary clock input (I1) is selected before or while GSR is active. In this case, the primary clock input (I0) is incorrectly selected. This occurs because there is a cross-coupled register pair that ensures the BUFGMUX output does not inadvertently generate a clock edge. When GSR is asserted, these registers initialize to the default state of I0. To select the secondary clock, you must send a clock pulse to both the primary and secondary clock inputs while GSR is inactive.

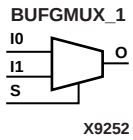
Note BUFGMUX guarantees that when S is toggled, the state of the output will remain in the inactive state until the next active clock edge (either I0 or I1) occurs.

Inputs			Outputs
I0	I1	S	O
I0	X	0	I0
X	I1	1	I1
X	X	↑	0
X	X	↓	0

BUFGMUX_1

Global Clock MUX Buffer with Output State 1

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



BUFGMUX_1 is a multiplexed global clock buffer that can select between two input clocks I0 and I1. When the select input (S) is Low, the signal on I0 is selected for output (O). When the select input (S) is High, the signal on I1 is selected for output.

BUFGMUX and BUFGMUX_1 are distinguished by which state the output assumes when it switches between clocks in response to a change in its select input. BUFGMUX assumes output state 0 and BUFGMUX_1 assumes output state 1.

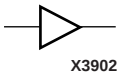
Using a BUFGMUX_1 element in your design may cause inaccurate simulation if all the following conditions occur: both clock inputs (I0 and I1) are used, GSR is activated during simulation (after simulation time ‘0’), and the secondary clock input (I1) is selected before or while GSR is active. In this case, the primary clock input (I0) is incorrectly selected. This occurs because there is a cross-coupled register pair that ensures the BUFGMUX_1 output does not inadvertently generate a clock edge. When GSR is asserted, these registers initialize to the default state of I0. To select the secondary clock, you must send a clock pulse to both the primary and secondary clock inputs while GSR is inactive.

Inputs			Outputs
I0	I1	S	O
I0	X	0	I0
X	I1	1	11
X	X	↑	1
X	X	↓	1

BUFGP

Primary Global Buffer for Driving Clocks or Longlines (Four per PLD Device)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



BUFGP, a primary global buffer, is used to distribute high fan-out clock or control signals throughout PLD devices.

In Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II and Virtex-II PRO, BUFGP is equivalent to an IBUFG driving a BUFG.

In XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, BUFGP is treated like BUFG.

A BUFGP provides direct access to Configurable Logic Block (CLB) and Input Output Block (IOB) clock pins and limited access to other CLB inputs. The input to a BUFGP comes only from a dedicated IOB.

Because of its structure, a BUFGP can always access a clock pin directly. However, it can access only one of the F3, G1, C3, or C1 pins, depending on the corner in which the BUFGP is placed. When the required pin cannot be accessed directly from the vertical line, PAR feeds the signal through another CLB and uses general purpose routing to access the load pin.

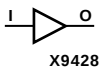
To use a BUFGP in a schematic, connect the input of the BUFGP element directly to the PAD symbol. Do not use any IBUFs, because the signal comes directly from a dedicated IOB. The output of the BUFGP is then used throughout the schematic. For a negative-edge clock, insert an INV (inverter) element between the output of the BUFGP and the clock input. This inversion is performed inside each CLB or IOB.

A Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II or Virtex-II PRO BUFGP must be sourced by an external signal. Other BUFGPs can be sourced by an internal signal, but PAR must use the dedicated IOB to drive the BUFGP, which means that the IOB is not available for use by other signals. If possible, use a BUFGS instead, because it can be sourced internally without using an IOB.

BUFGSR

Global Set/Reset Input Buffer

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Primitive	Primitive	Primitive



BUFGSR distributes global set/reset signals throughout selected flip-flops of an XC9500/XV/XL, CoolRunner XPLA3, or CoolRunner-II device. Global Set/Reset (GSR) control pins are available on these CPLD devices. Consult device data sheets for availability.

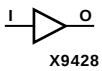
BUFGSR always acts as an input buffer. To use it in a schematic, connect the input of the BUFGSR symbol to an IPAD or an IOPAD representing the GSR signal source. GSR signals generated on-chip must be passed through an OBUF-type buffer before they are connected to BUFGSR.

For global set/reset control, the output of BUFGSR normally connects to the CLR or PRE input of a flip-flop symbol, like FDCP, or any registered symbol with asynchronous clear or preset. The global set/reset control signal may pass through an inverter to perform an active-low set/reset. The output of BUFGSR may also be used as an ordinary input signal to other logic elsewhere in the design. Each BUFGSR can control any number of flip-flops in a design.

BUFGTS

Global 3-State Input Buffer

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Primitive	Primitive	Primitive



BUFGTS distributes global output-enable signals throughout the output pad drivers of an XC9500/XV/XL, CoolRunner XPLA3, or CoolRunner-II device. Global Three-State (GTS) control pins are available on these CPLD devices. Consult device data sheets for availability.

BUFGTS always acts as an input buffer. To use it in a schematic, connect the input of the BUFGTS symbol to an IPAD or an IOPAD representing the GTS signal source. GTS signals generated on-chip must be passed through an OBUF-type buffer before they are connected to BUFGTS.

For global 3-state control, the output of BUFGTS normally connects to the E input of a 3-state output buffer symbol, OBUFE. The global 3-state control signal may pass through an inverter or control an OBUFT symbol to perform an active-low output-enable. The same 3-state control signal may even be used both inverted and non-inverted to enable alternate groups of device outputs. The output of BUFGTS may also be used as an ordinary input signal to other logic elsewhere in the design. Each BUFGTS can control any number of output buffers in a design.

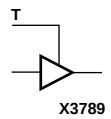
BUFT, 4, 8, 16

Internal 3-State Buffers with Active-Low Enable

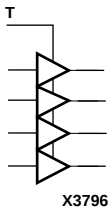
Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
BUFT	Primitive	Primitive	Primitive	Primitive*	Primitive	Primitive
BUFT4, BUFT8, BUFT16	Macro	Macro	Macro	Macro*	Macro	Macro

* not supported for XC9500XL and XC9500XV devices

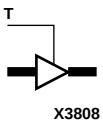
BUFT



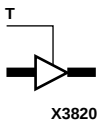
BUFT4



BUFT8



BUFT16



BUFT, BUFT4, BUFT8, and BUFT16 are single or multiple 3-state buffers with inputs I, I3 – I0, I7 – I0, and I15 – 10, respectively; outputs O, O3 – O0, O7 – O0, and O15 – O0, respectively; and active-Low output enable (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (Z state or off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures.

The outputs of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at one time. If none of the T inputs is active (Low), a "weak-keeper" circuit (Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO) prevents the output bus from floating but does not guarantee that the bus remains at the last value driven onto it.

For XC9500/XV/XL devices, BUFT output nets assume the High logic level when all connected BUFE/BUFT buffers are disabled. On-chip 3-state multiplexing is not available in XC9500XL devices.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, when all BUFTs on a net are disabled, the net is High. For correct simulation of this effect, a PULLUP element must be connected to the net. NGDBuild inserts a PULLUP element if one is not connected so that back-annotation simulation reflects the true state of the device.

Inputs		Outputs
T	I	O
1	X	Z
0	1	1
0	0	0

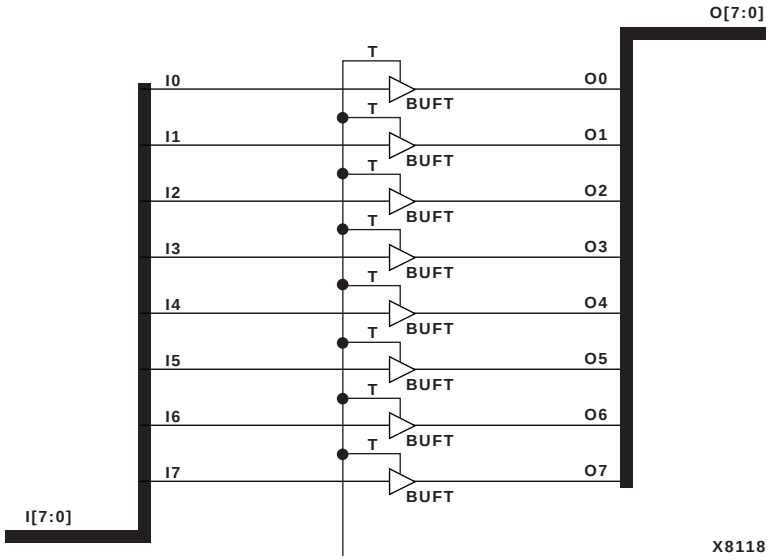


Figure 3-29 BUFT8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

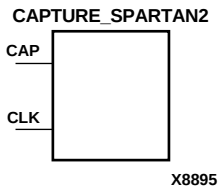
Chapter 4

CAPTURE_SPARTAN2 to DECODE32, 64

CAPTURE_SPARTAN2

Spartan-II Register State Capture for Bitstream Readback

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	N/A	N/A	N/A	N/A	N/A



CAPTURE_SPARTAN2 provides user control over when to capture register (flip-flop and latch) information for readback. Spartan-II and Spartan-II E devices provide the readback function through dedicated configuration port instructions, instead of with a READBACK component as in other FPGA architectures. The CAPTURE_SPARTAN2 symbol is optional. Without it readback is still performed, but the asynchronous capture function it provides for register states is not available.

Note Spartan-II and Spartan-II E devices only allow for capturing register (flip-flop and latch) states. Although LUT RAM, SRL, and block RAM states are read back, they cannot be captured.

An asserted High CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. The Low-to-High clock transition triggers the capture clock (CLK) which clocks out the readback data.

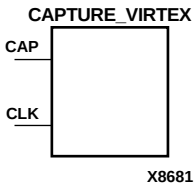
By default, data is captured after every trigger (transition on CLK while CAP is asserted). To limit the readback operation to a single data capture, add the ONESHOT attribute to CAPTURE_SPARTAN2. See the *Constraints Guide* for information on the ONESHOT attribute.

Note For details on the Spartan-II and Spartan-II E readback functions, see *The Programmable Logic Data Book*.

CAPTURE_VIRTEX

Virtex Register State Capture for Bitstream Readback

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	Primitive	N/A	N/A	N/A	N/A



CAPTURE_VIRTEX provides user control over when to capture register (flip-flop and latch) information for readback. Virtex and Virtex-E devices provide the readback function through dedicated configuration port instructions, instead of with a READBACK component as in other FPGA architectures.

Note For Virtex-II and Virtex-II PRO, see "CAPTURE_VIRTEX2".

The CAPTURE_VIRTEX symbol is optional. Without it readback is still performed, but the asynchronous capture function it provides for register states is not available.

Note Virtex and Virtex-E allow for capturing register (flip-flop and latch) states only. Although LUT RAM, SRL, and block RAM states are read back, they cannot be captured.

An asserted High CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. The Low-to-High clock transition triggers the capture clock (CLK) which clocks out the readback data.

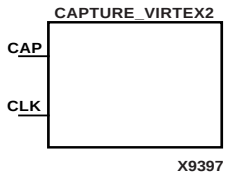
By default, data is captured after every trigger (transition on CLK while CAP is asserted). To limit the readback operation to a single data capture, add the ONESHOT attribute to CAPTURE_VIRTEX. See the *Constraints Guide* for information on the ONESHOT attribute.

For details on the Virtex and Virtex-E readback functions, see the Virtex datasheets on the Xilinx web site, http://support.xilinx.com.

CAPTURE_VIRTEX2

Virtex-II Register State Capture for Bitstream Readback

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



CAPTURE_VIRTEX2 provides user control over when to capture register (flip-flop and latch) information for readback. Virtex-II and Virtex-II PRO devices provide the readback function through dedicated configuration port instructions, instead of with a READBACK component as in other FPGA architectures.

Note For Virtex and Virtex-E, see "CAPTURE_VIRTEX".

The CAPTURE_VIRTEX2 symbol is optional. Without it readback is still performed, but the asynchronous capture function it provides for register states is not available.

Virtex-II and Virtex-II PRO allow for capturing register (flip-flop and latch) states only. Although LUT RAM, SRL, and block RAM states are read back, they cannot be captured.

An asserted high CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. The Low-to-High clock transition triggers the capture clock (CLK) which clocks out the readback data.

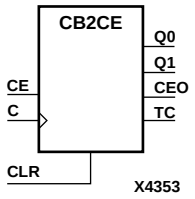
By default, data is captured after every trigger (transition on CLK while CAP is asserted). To limit the readback operation to a single data capture, add the ONESHOT attribute to CAPTURE_VIRTEX2. See the *Constraints Guide* for information on the ONESHOT attribute.

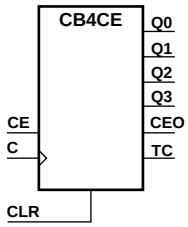
For details on the Virtex-II and Virtex-II PRO readback functions, see *The Programmable Logic Data Book*.

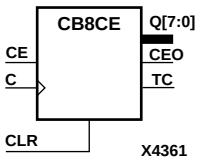
CB2CE, CB4CE, CB8CE, CB16CE

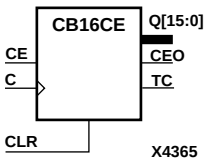
2-, 4-, 8-,16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro









CB2CE, CB4CE, CB8CE, and CB16CE are, respectively, 2-, 4-, 8-, and 16-bit (stage), asynchronous, clearable, cascadable binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, outputs Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

z= 1 for CB2CE; z = 3 for CB4CE; z = 7 for CB8CE; z = 15 for CB16CE

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEO = TC • CE

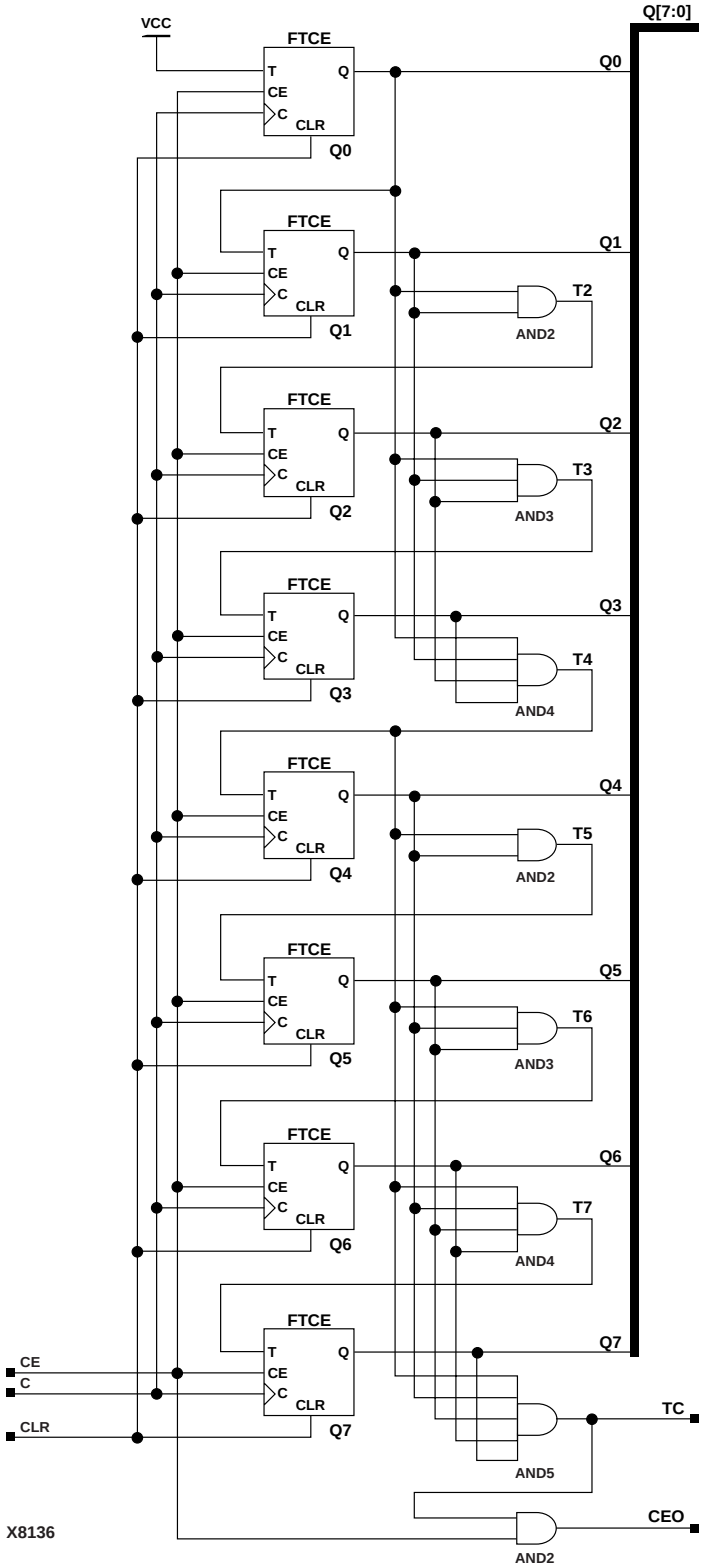


Figure 4-1 CB8CE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

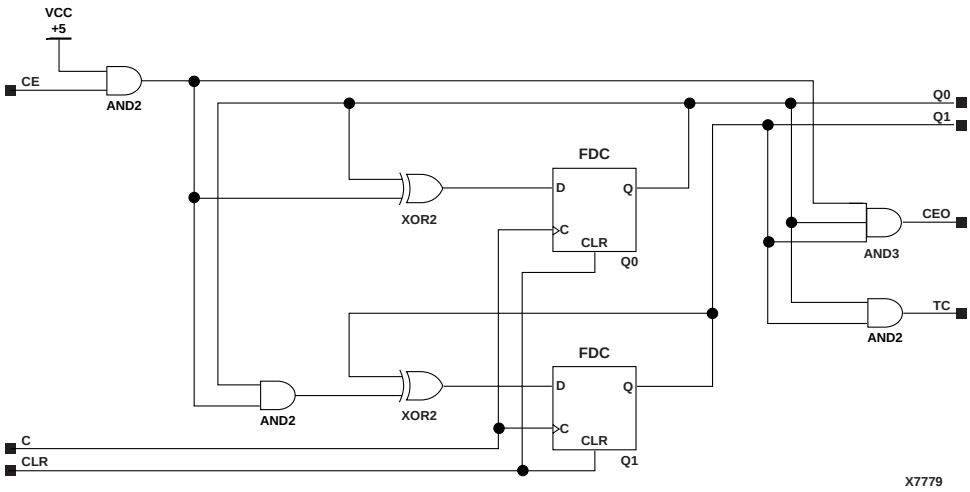


Figure 4-2 CB2CE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

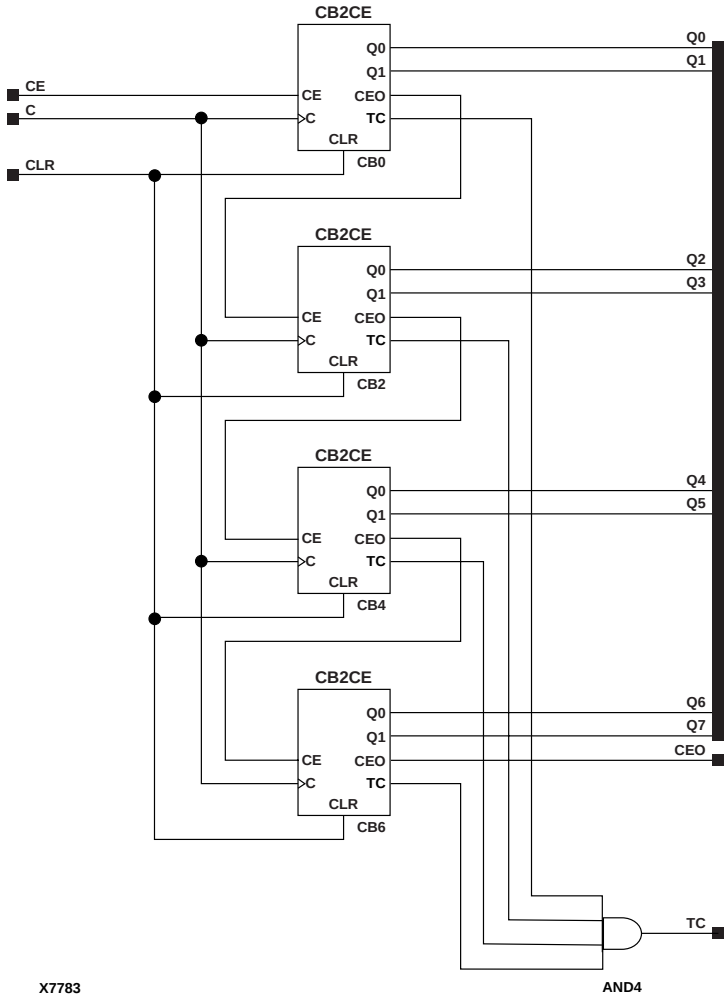
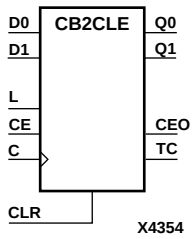


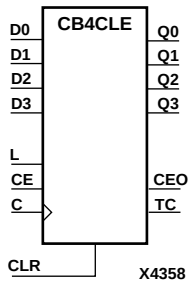
Figure 4-3 CB8CE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

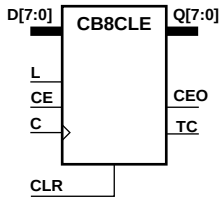
CB2CLE, CB4CLE, CB8CLE, CB16CLE

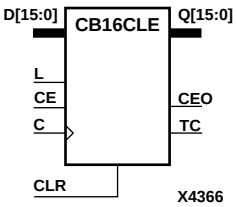
2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro









CB2CLE, CB4CLE, CB8CLE, and CB16CLE are, respectively, 2-, 4-, 8-, and 16-bit (stage) synchronously loadable, asynchronously clearable, cascadable binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	dn	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

z= 1 for CB2CLE; z = 3 for CB4CLE; z = 7 for CB8CLE; z = 15 for CB16CLE

dn = state of referenced input (Dn) one setup time prior to active clock transition.

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEO = TC • CE

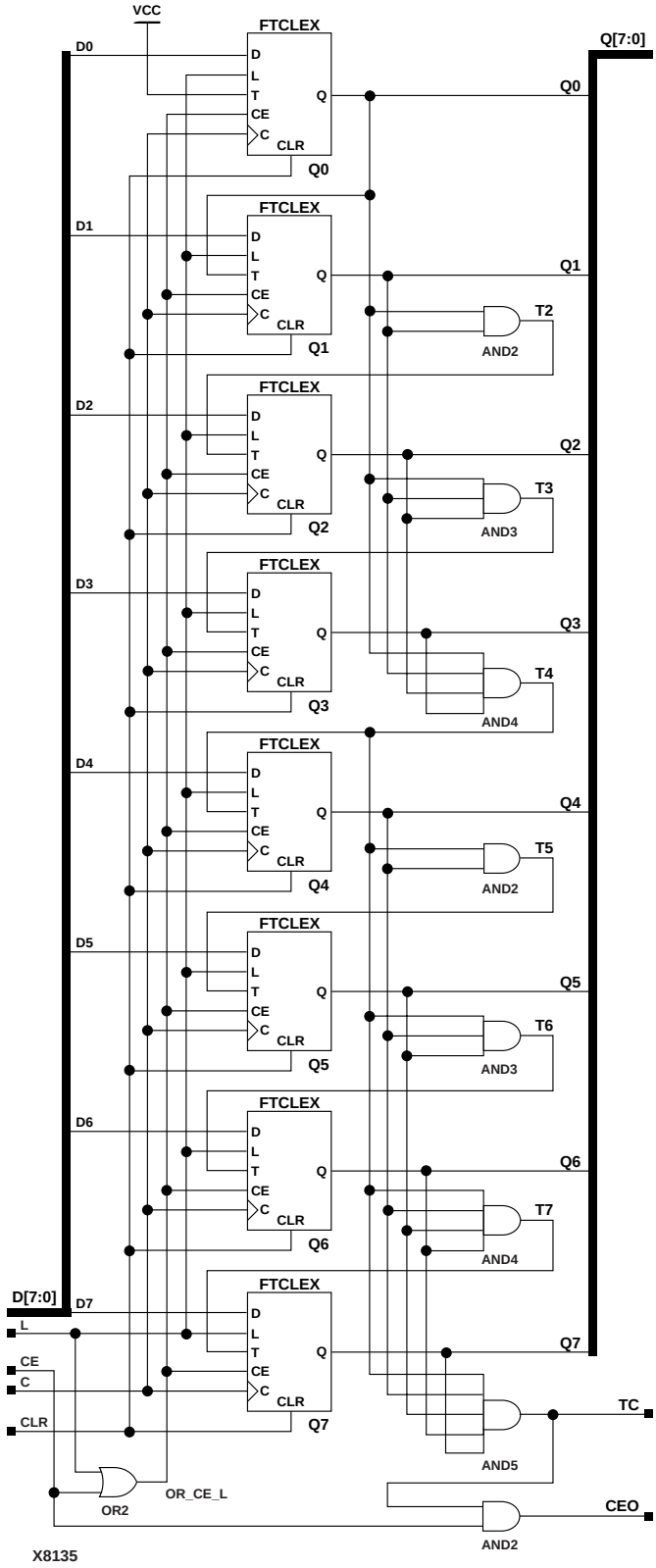


Figure 4-4 CB8CLE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

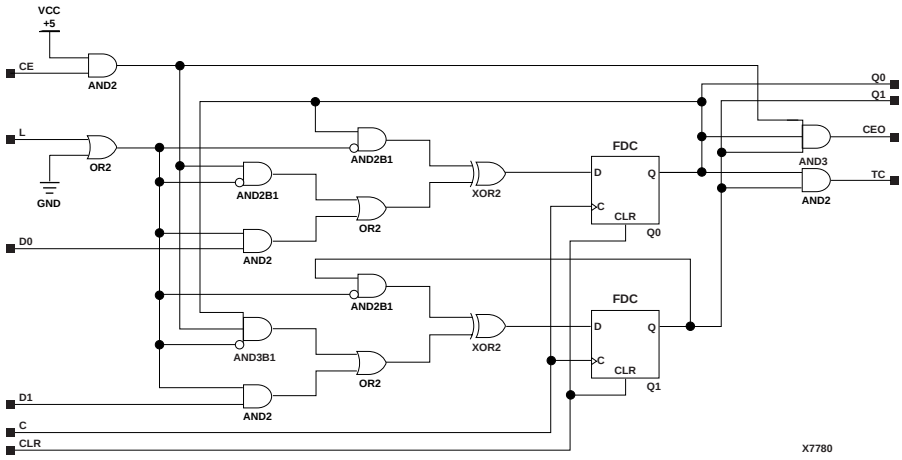


Figure 4-5 CB2CLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

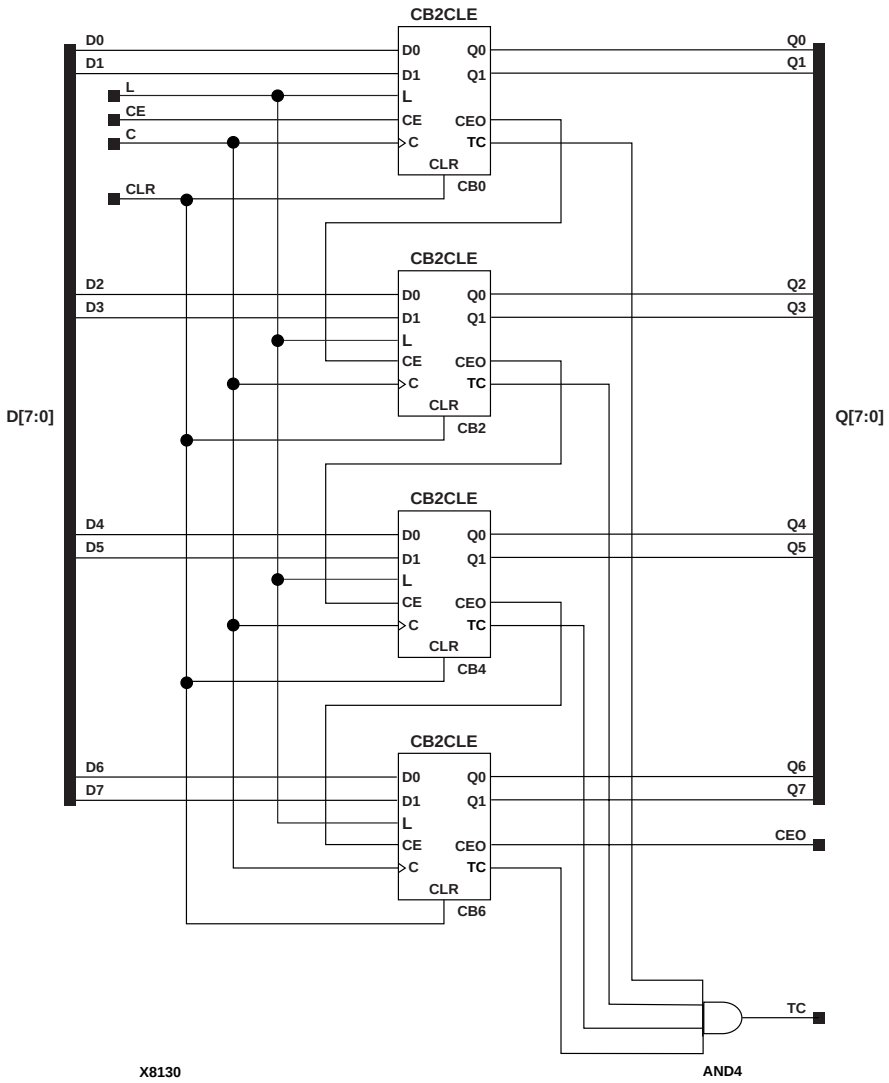
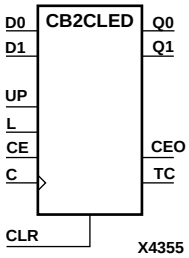


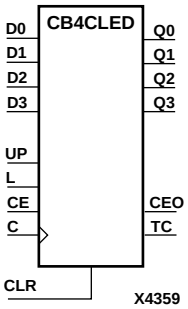
Figure 4-6 CB8CLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

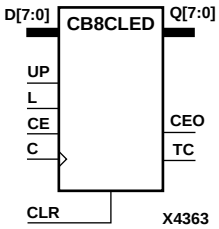
CB2CLED, CB4CLED, CB8CLED, CB16CLED

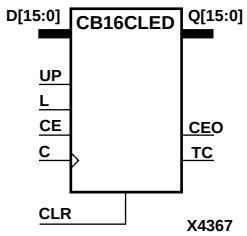
2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro









CB2CLED, CB4CLED, CB8CLED, and CB16CLED are, respectively, 2-, 4-, 8- and 16-bit (stage), synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low. To cascade counters, the CEO output of each counter is connected to the CE pin of the next stage. The clock, UP, L, and CLR inputs are connected in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage.

When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not. For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, see the "CB2X1, CB4X1, CB8X1, CB16X1" section for high-performance cascadable, bidirectional counters.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted with an inverter in front of the GSR input of STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2.

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	dn	TC	CEO
0	0	0	X	X	X	No Chg	No Chg	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

z = 1 for CB2CLED; z = 3 for CB4CLED; z = 7 for CB8CLED; z = 15 for CB16CLED

dn = state of referenced input (Dn), one setup time prior to active clock transition

TC = (Qz • Q(z-1) • Q(z-2) • ... • Q0 • UP) + (Qz • Q(z-1) • Q(z-2) • ... • Q0 • UP)

CEO = TC • CE

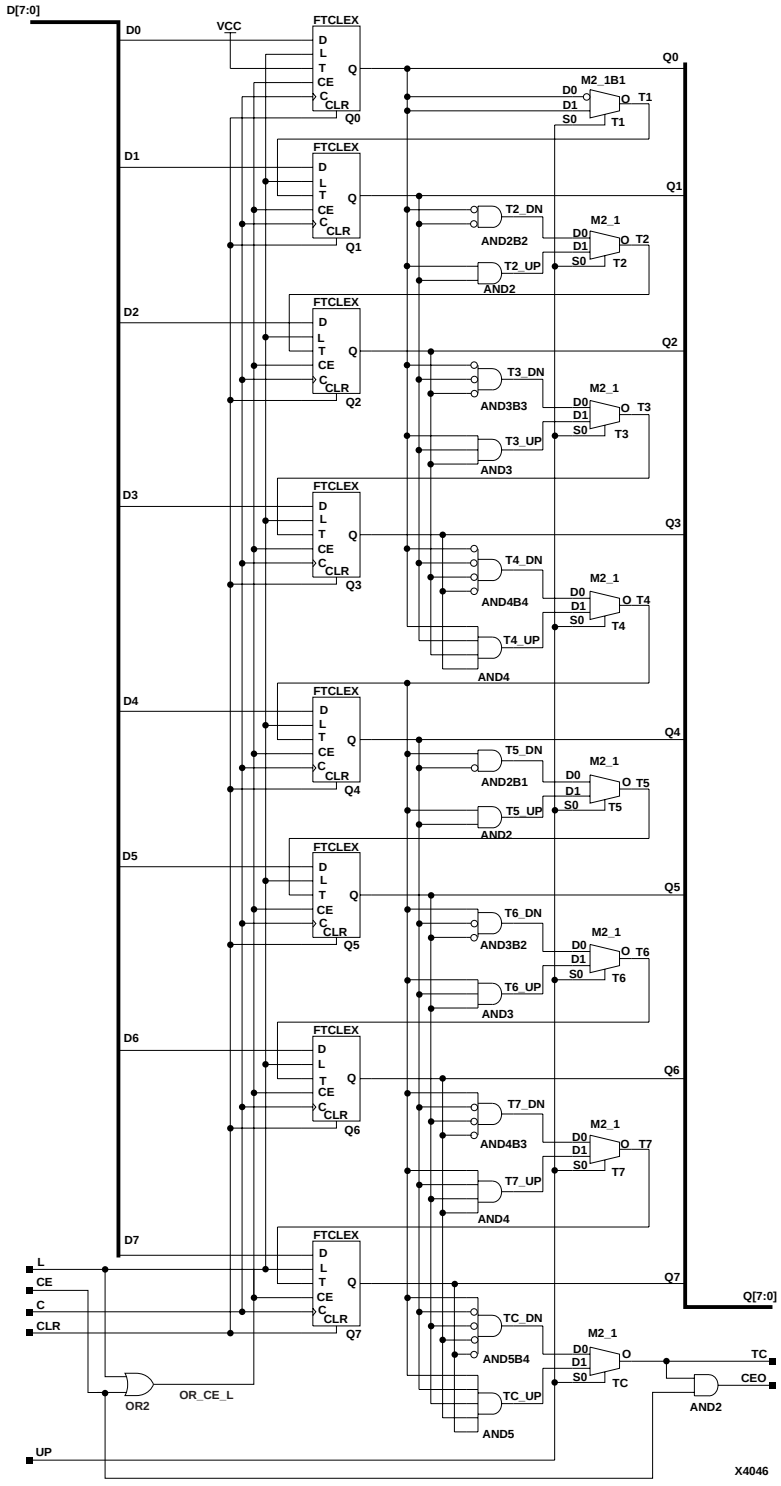


Figure 4-7 CB8CLED Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

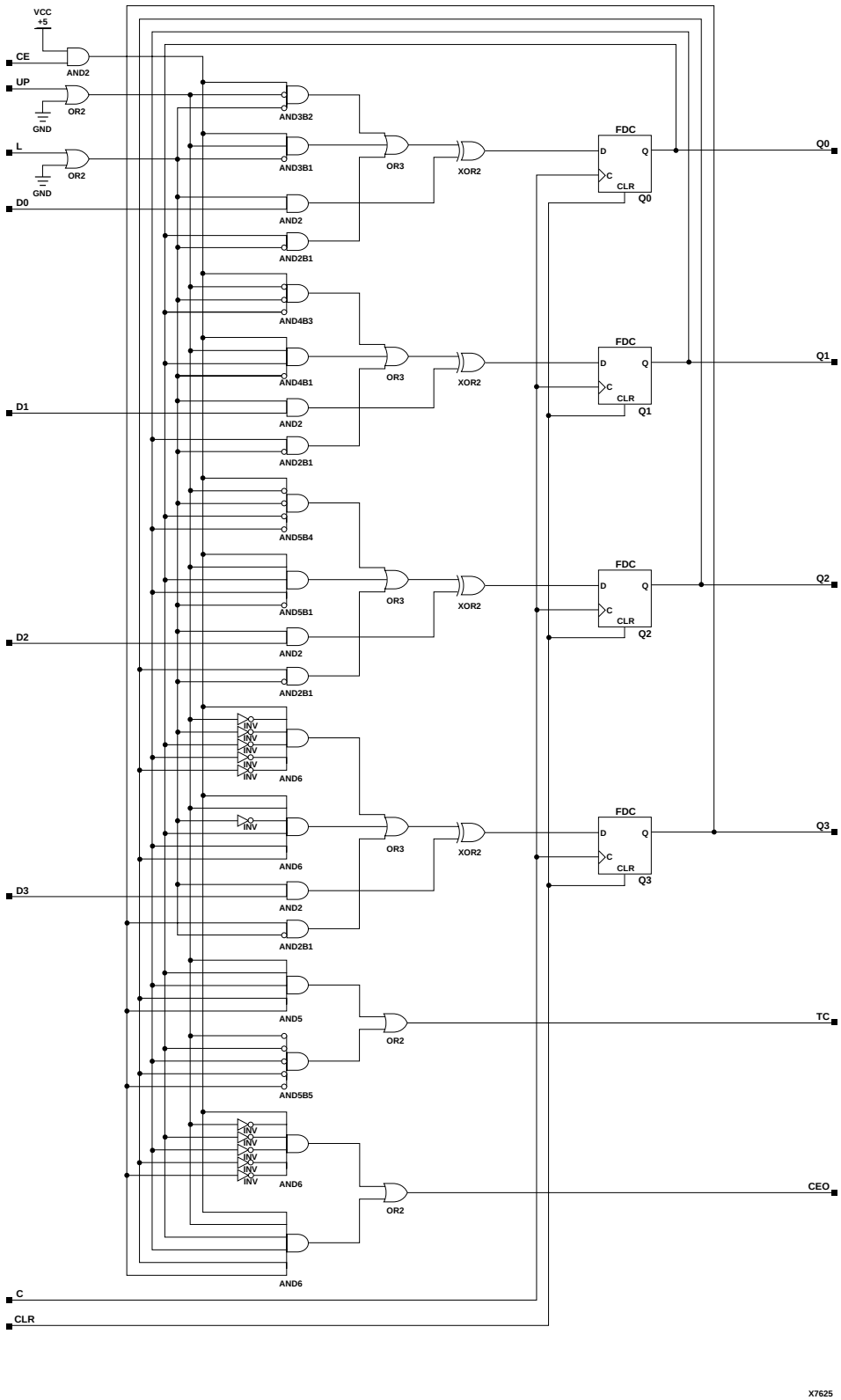
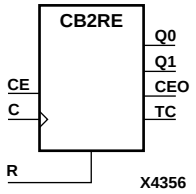


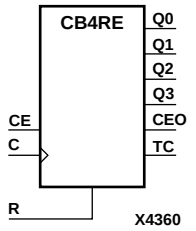
Figure 4-8 CB4CLED Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

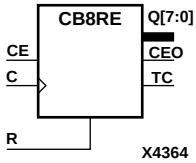
CB2RE, CB4RE, CB8RE, CB16RE

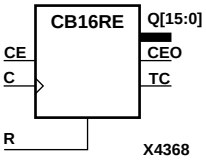
2-, 4-, 8-, 16-Bit Cascadable Binary Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro









CB2RE, CB4RE, CB8RE, and CB16RE are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, resettable, cascadable binary counters. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero during the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs		
R	CE	C	Qz – Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

z = 1 for CB2RE; z = 3 for CB4RE; z = 7 for CB8RE; z = 15 for CB16RE

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0)

CEO = TC • CE

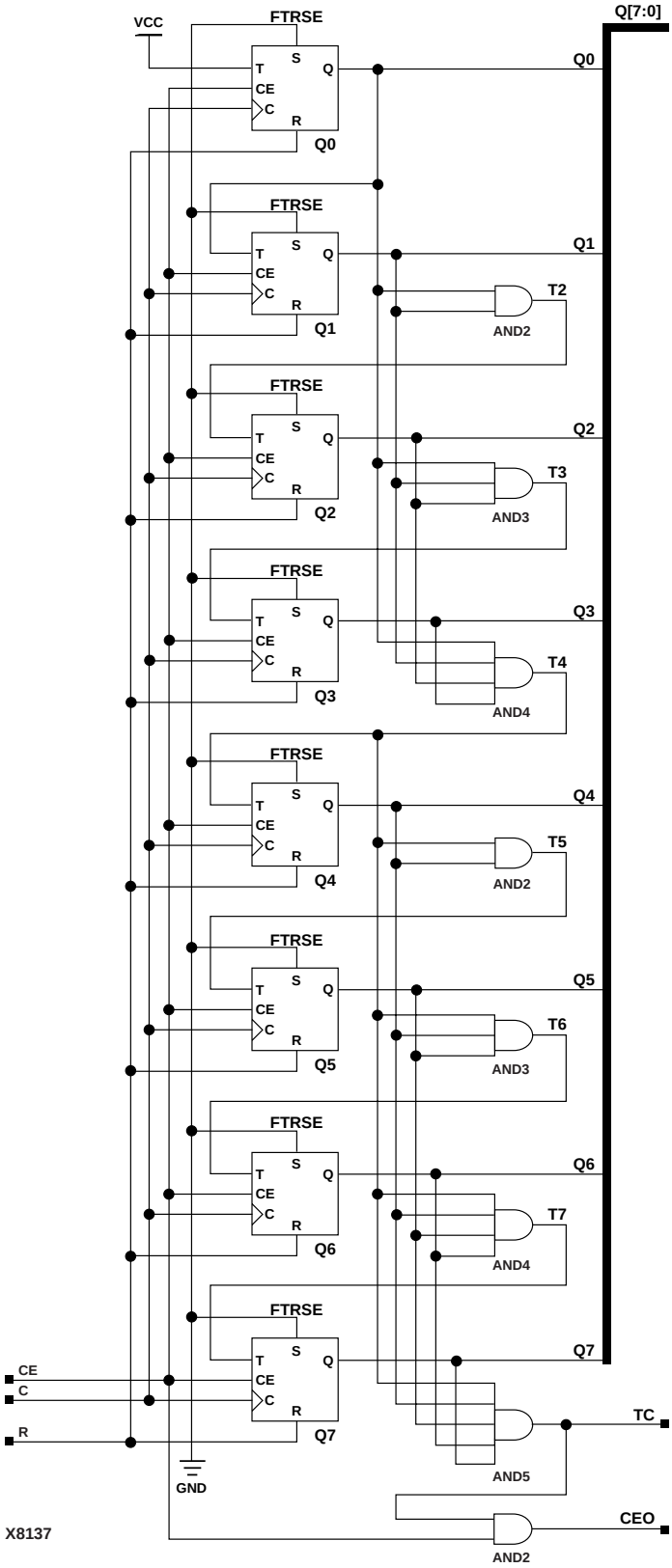


Figure 4-9 CB8RE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

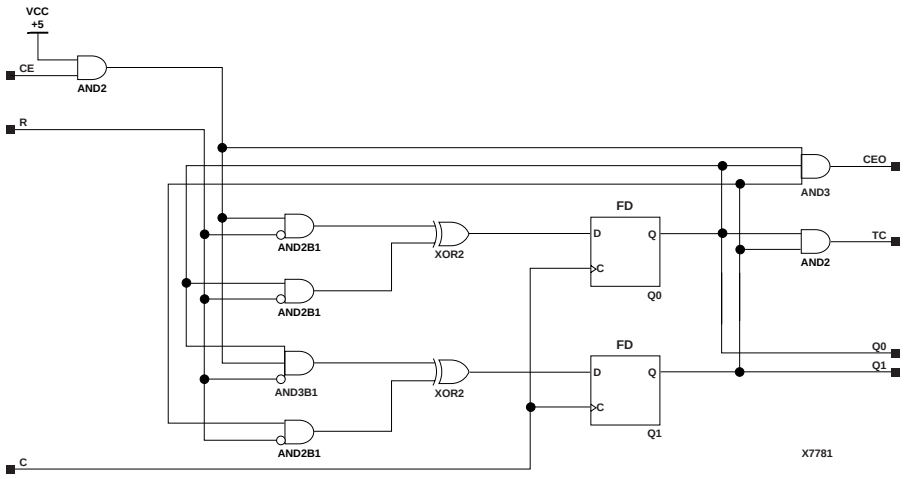


Figure 4-10 CB2RE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

I

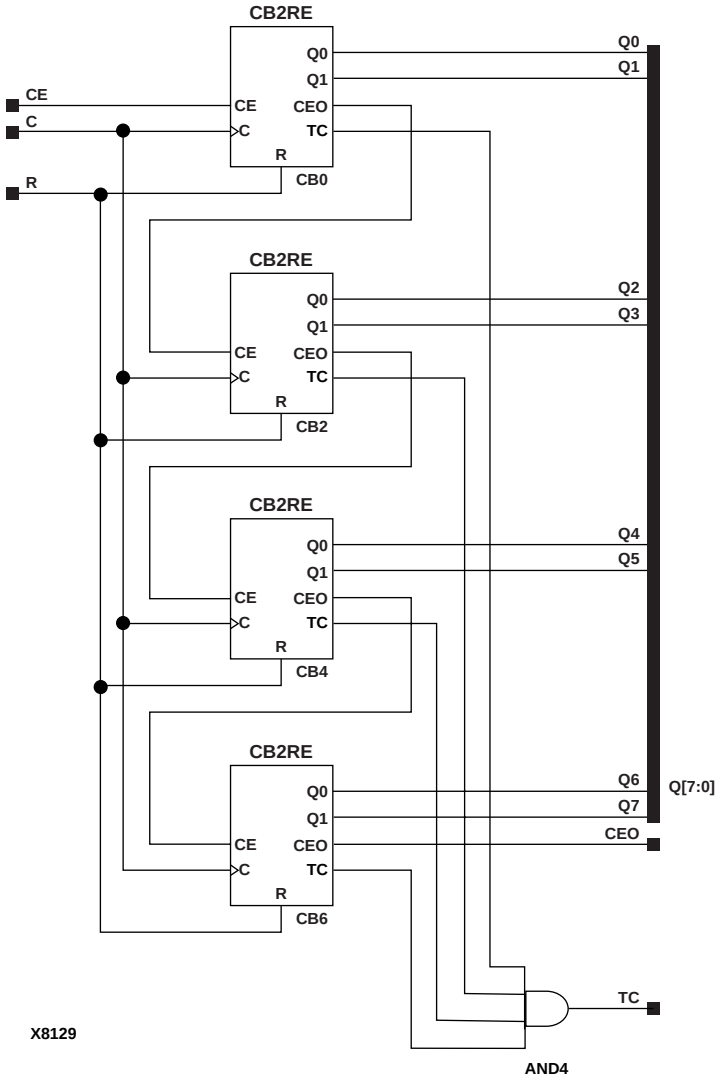
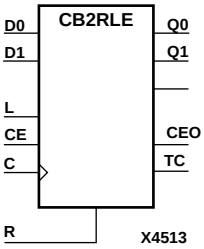


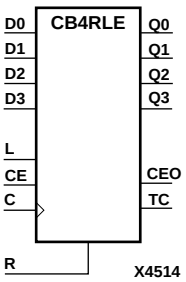
Figure 4-11 CB8RE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

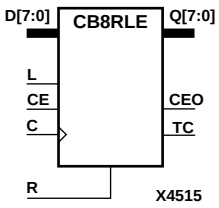
CB2RLE, CB4RLE, CB8RLE, CB16RLE

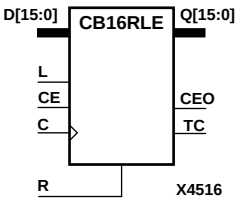
2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro









CB2RLE, CB4RLE, CB8RLE, and CB16RLE are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R) is the highest priority input. The synchronous R, when High, overrides all other inputs and resets the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and by connecting the C, L, and R inputs in parallel. The maximum length of the counter is determined by the accumulated CE-to-CEO propagation delays versus the clock period. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs		
R	L	CE	C	Dz – D0	Qz – Q0	TC	CEO
1	X	X	↑	X	0	0	0
0	1	X	↑	Dn	dn	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

z = 1 for CB2RLE; z = 3 for CB4RLE; z = 7 for CB8RLE; z = 15 for CB16RLE

dn = state of referenced input (Dn) one setup time prior to active clock transition

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEO = TC • CE

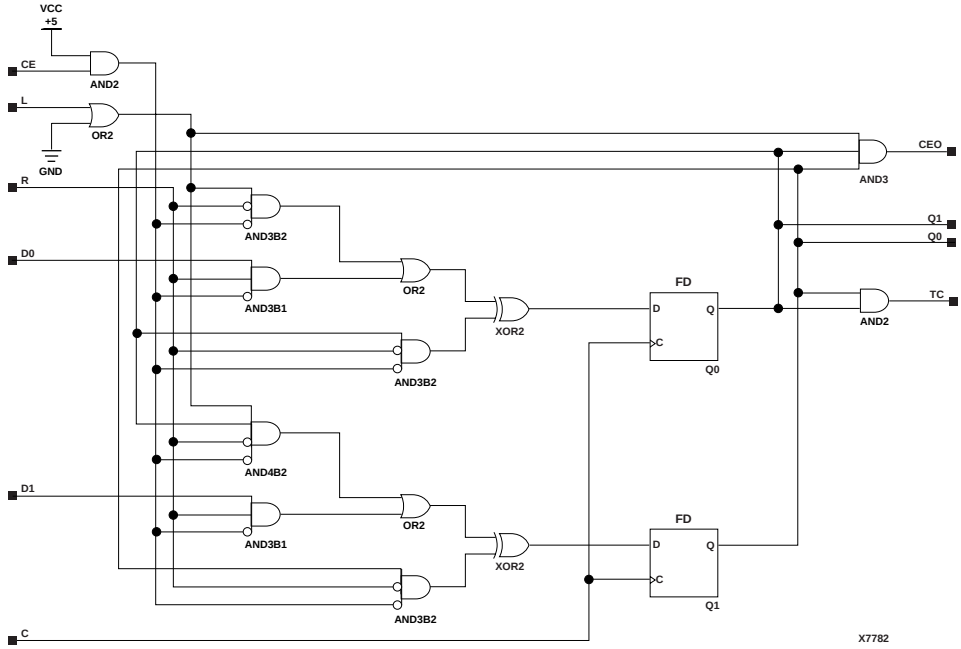


Figure 4-12 CB2RLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

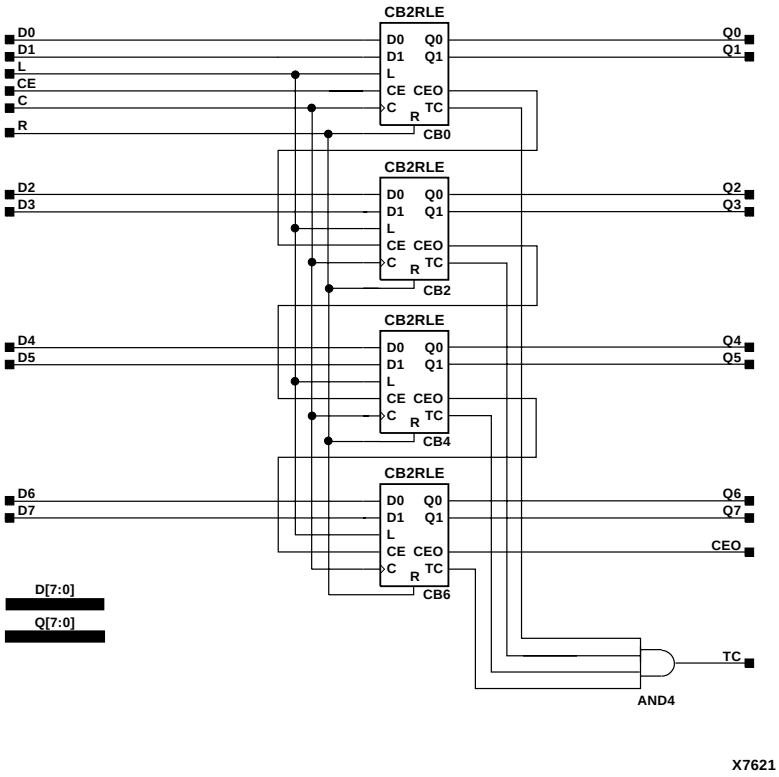
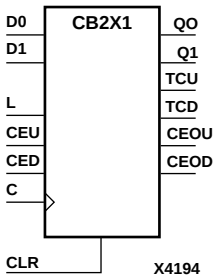


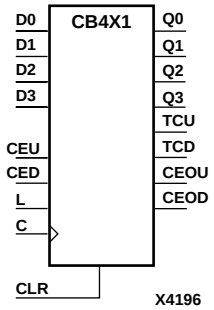
Figure 4-13 CB8RLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

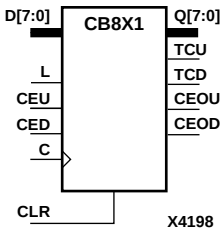
CB2X1, CB4X1, CB8X1, CB16X1

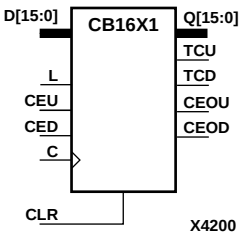
2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro









CB2X1, CB4X1, CB8X1, and CB16X1 are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronously loadable, asynchronously clearable, bidirectional binary counters. These counters have separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs				
CLR	**L**	**CEU**	**CED**	**C**	**Dz–D0**	**Qz–Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid

z = 1 for CB2X1; z = 3 for CB4X1; z = 7 for CB8X1; z = 15 for CB16X1

dn = state of referenced input (Dn) one setup time prior to active clock transition

TCU = Qz • Q(z-1) • Q(z-2) • ... • Q0

TCD = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEOU = TCU • CEU

CEOD = TCD • CED

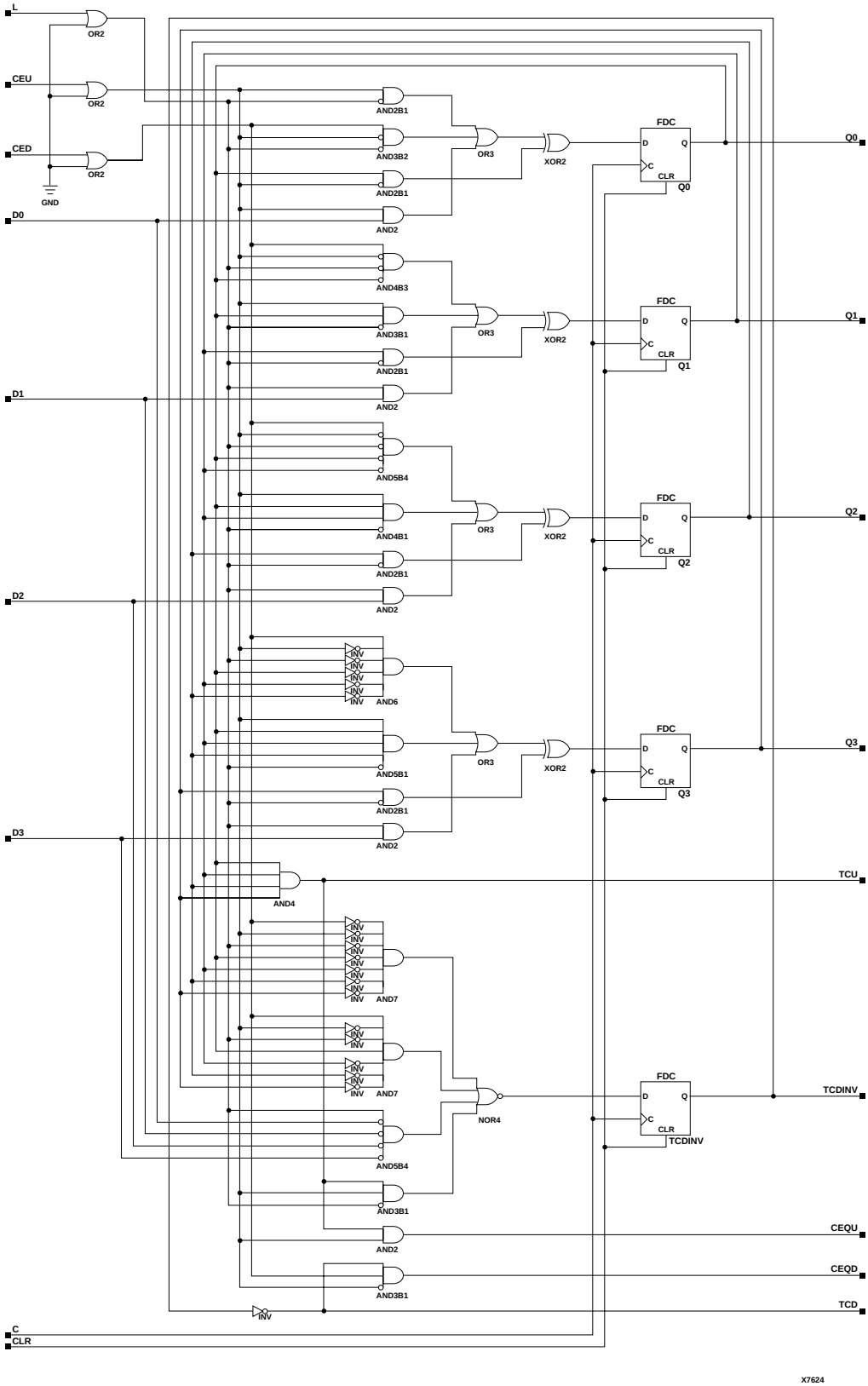
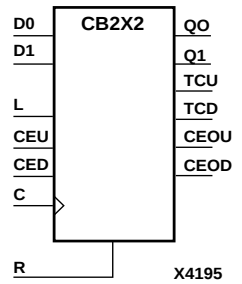


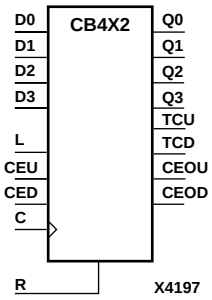
Figure 4-14 CB4X1 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

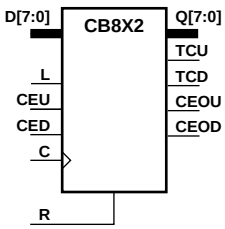
CB2X2, CB4X2, CB8X2, CB16X2

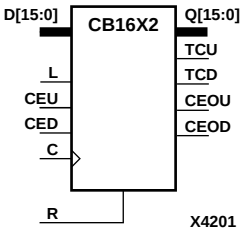
2-, 4-, 8-, and 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro









CB2X2, CB4X2, CB8X2, and CB16X2 are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, loadable, resettable, bidirectional binary counters. These counters have separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs				
R	**L**	**CEU**	**CED**	**C**	**Dz – D0**	**Qz – Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	↑	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid

z = 1 for CB2X2; z = 3 for CB4X2; z = 7 for CB8X2; z = 15 for CB16X2

d = state of referenced input (Dn) one setup time prior to active clock transition

TCU = Qz • Q(z-1) • Q(z-2) • ... • Q0

TCD = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEOU = TCU • CEU

CEOD = TCD • CED

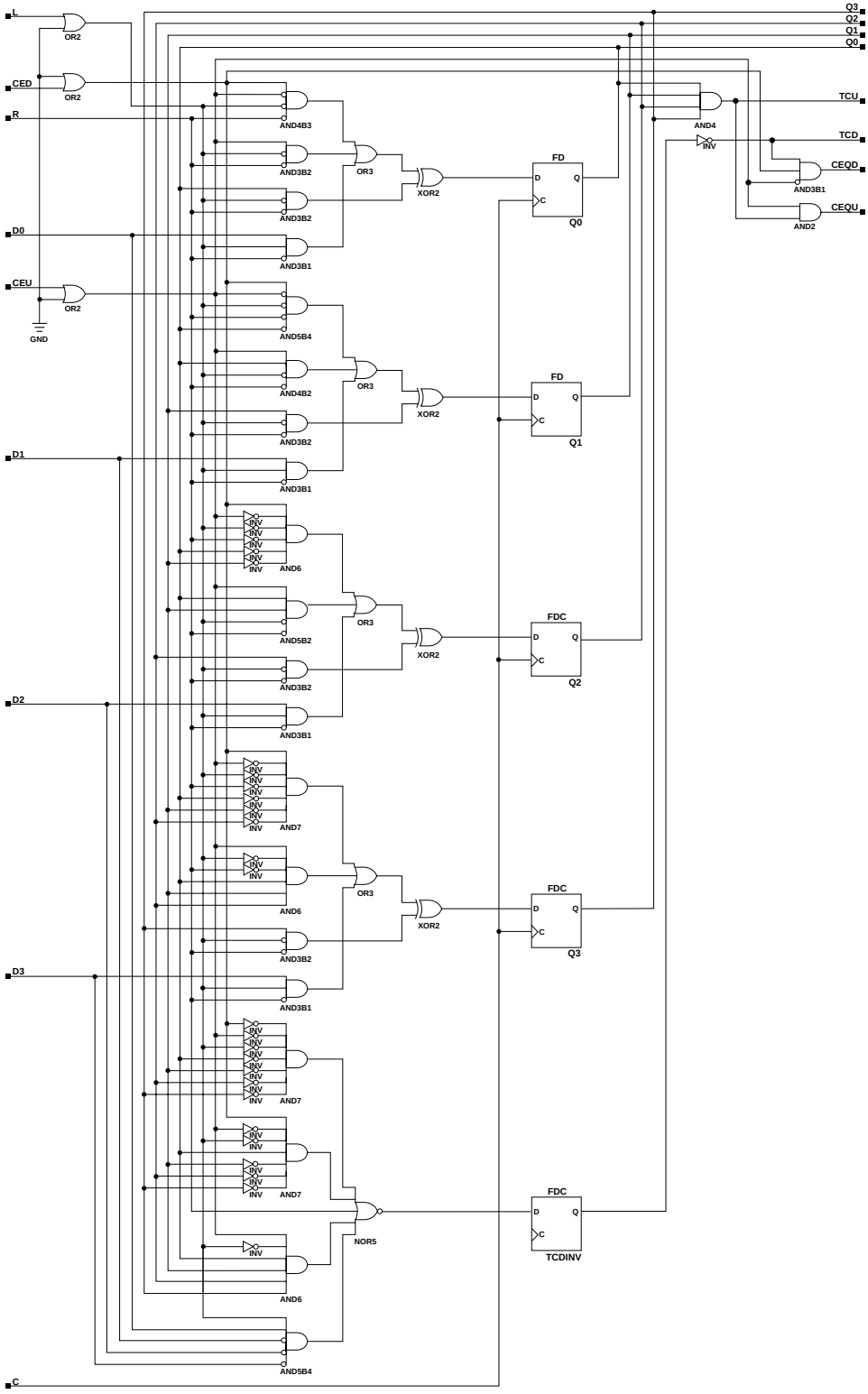
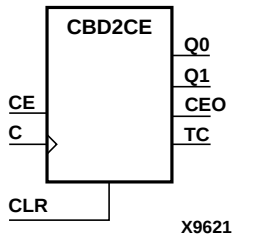


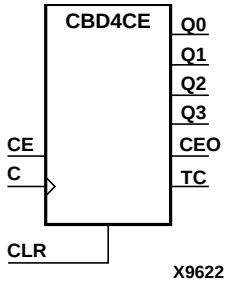
Figure 4-15 CB4X2 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

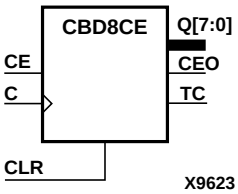
CBD2CE, CBD4CE, CBD8CE, CBD16CE

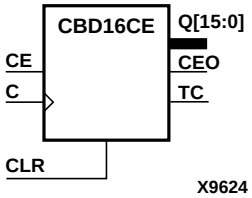
2-, 4-, 8-,16-Bit Cascadable Dual Edge Triggered Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro









CBD2CE, CBD4CE, CBD8CE, and CBD16CE are, respectively, 2-, 4-, 8-, and 16-bit (stage), asynchronous, clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs	
TC	TC	TC	TC	TC
1	X	X	0	0
0	0	X	No Chg	No Chg
0	1	↑	Inc	TC
0	1	↓	Inc	TC

z= 1 for CBD2CE; z = 3 for CBD4CE; z = 7 for CBD8CE; z = 15 for CBD16CE

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEO = TC • CE

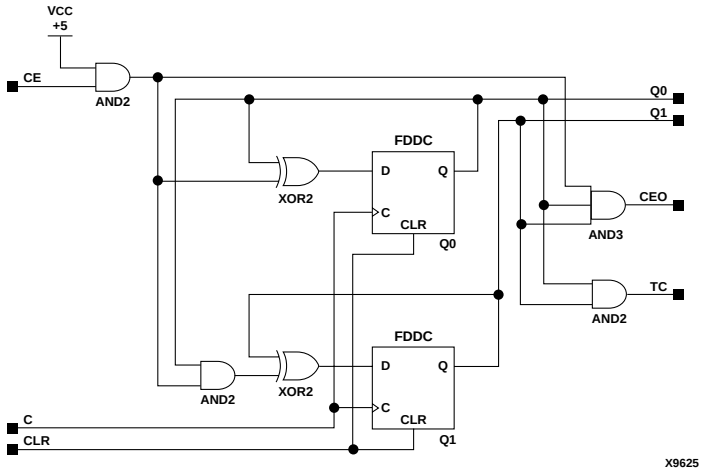


Figure 4-16 CBD2CE Implementation CoolRunner-II

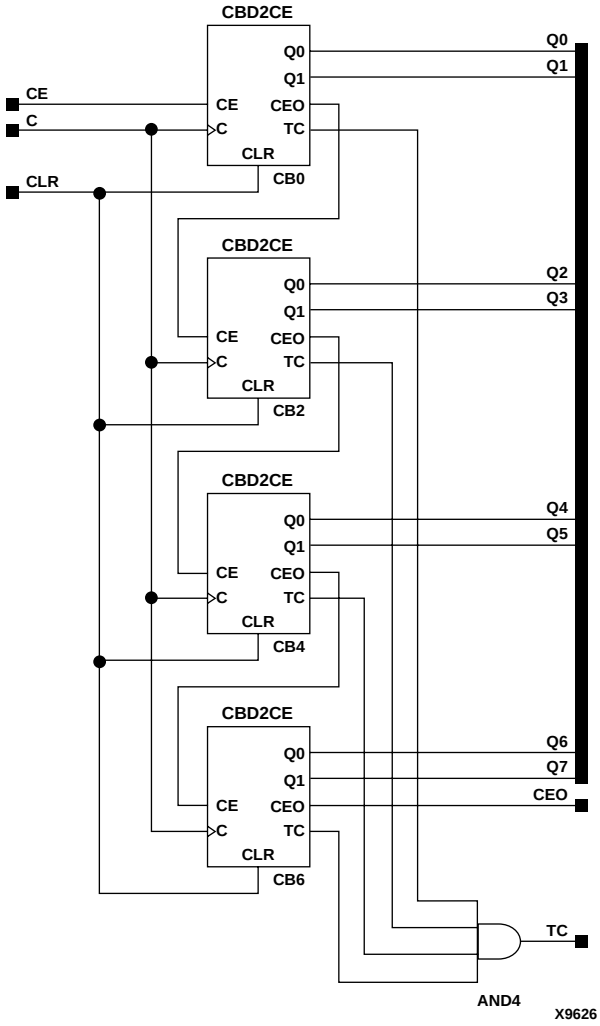
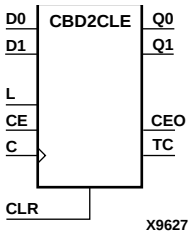


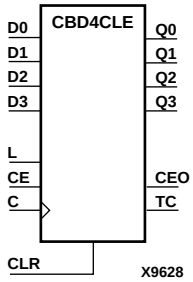
Figure 4-17 CBD8CE Implementation CoolRunner-II

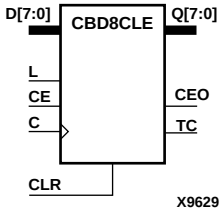
CBD2CLE, CBD4CLE, CBD8CLE, CBD16CLE

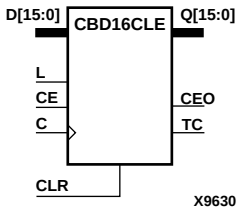
2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro









CBD2CLE, CBD4CLE, CBD8CLE, and CBD16CLE are, respectively, 2-, 4-, 8-, and 16-bit (stage) synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs		
CLR	L	CE	C	Dz – D0	Qz – Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	dn	TC	CEO
0	1	X	↓	Dn	dn	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

Inputs					Outputs		
CLR	L	CE	C	Dz – D0	Qz – Q0	TC	CEO
0	0	1	↓	X	Inc	TC	CEO

z= 1 for CBD2CLE; z = 3 for CBD4CLE; z = 7 for CBD8CLE; z = 15 for CBD16CLE

dn = state of referenced input (Dn) one setup time prior to active clock transition.

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEO = TC • CE

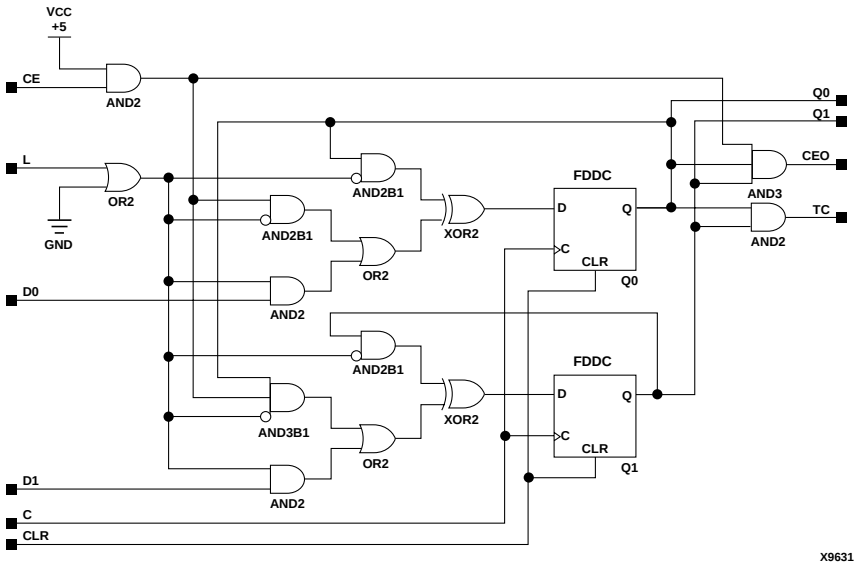


Figure 4-18 CBD2CLE Implementation CoolRunner-II

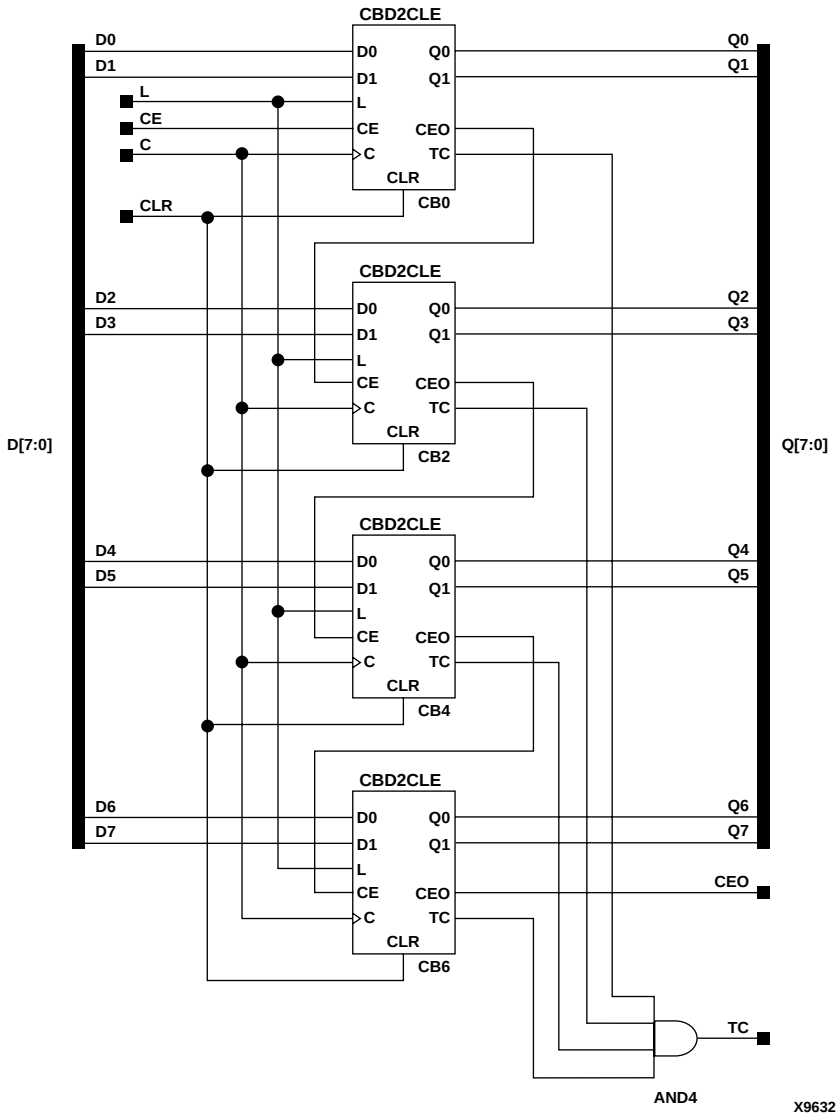
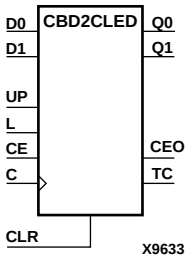


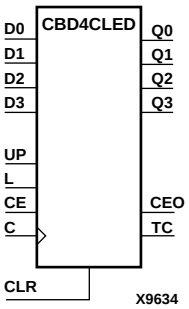
Figure 4-19 CBD8CLE Implementation CoolRunner-II

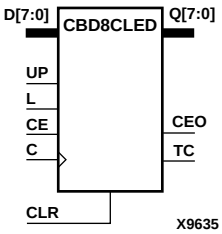
CBD2CLED, CBD4CLED, CBD8CLED, CBD16CLED

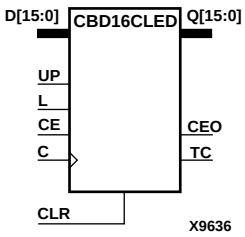
2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro









CBD2CLED, CBD4CLED, CBD8CLED, and CBD16CLED are, respectively, 2-, 4-, 8- and 16-bit (stage), synchronously loadable, asynchronously clearable, cascadable, bidirectional dual edge triggered binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low. To cascade counters, the CEO output of each counter is connected to the CE pin of the next stage. The clock, UP, L, and CLR inputs are connected in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage.

When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not. For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, see the "CB2X1, CB4X1, CB8X1, CB16X1" section for high-performance cascadable, bidirectional counters.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	dn	TC	CEO
0	1	X	↓	X	Dn	dn	TC	CEO
0	0	0	X	X	X	No Chg	No Chg	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↓	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
0	0	1	↓	0	X	Dec	TC	CEO

z = 1 for CBD2CLED; z = 3 for CBD4CLED; z = 7 for CBD8CLED; z = 15 for CBD16CLED

dn = state of referenced input (Dn), one setup time prior to active clock transition

TC = (Qz • Q(z-1) • Q(z-2) • ... • Q0 • UP) + (Qz • Q(z-1) • Q(z-2) • ... • Q0 • UP)

CEO = TC • CE

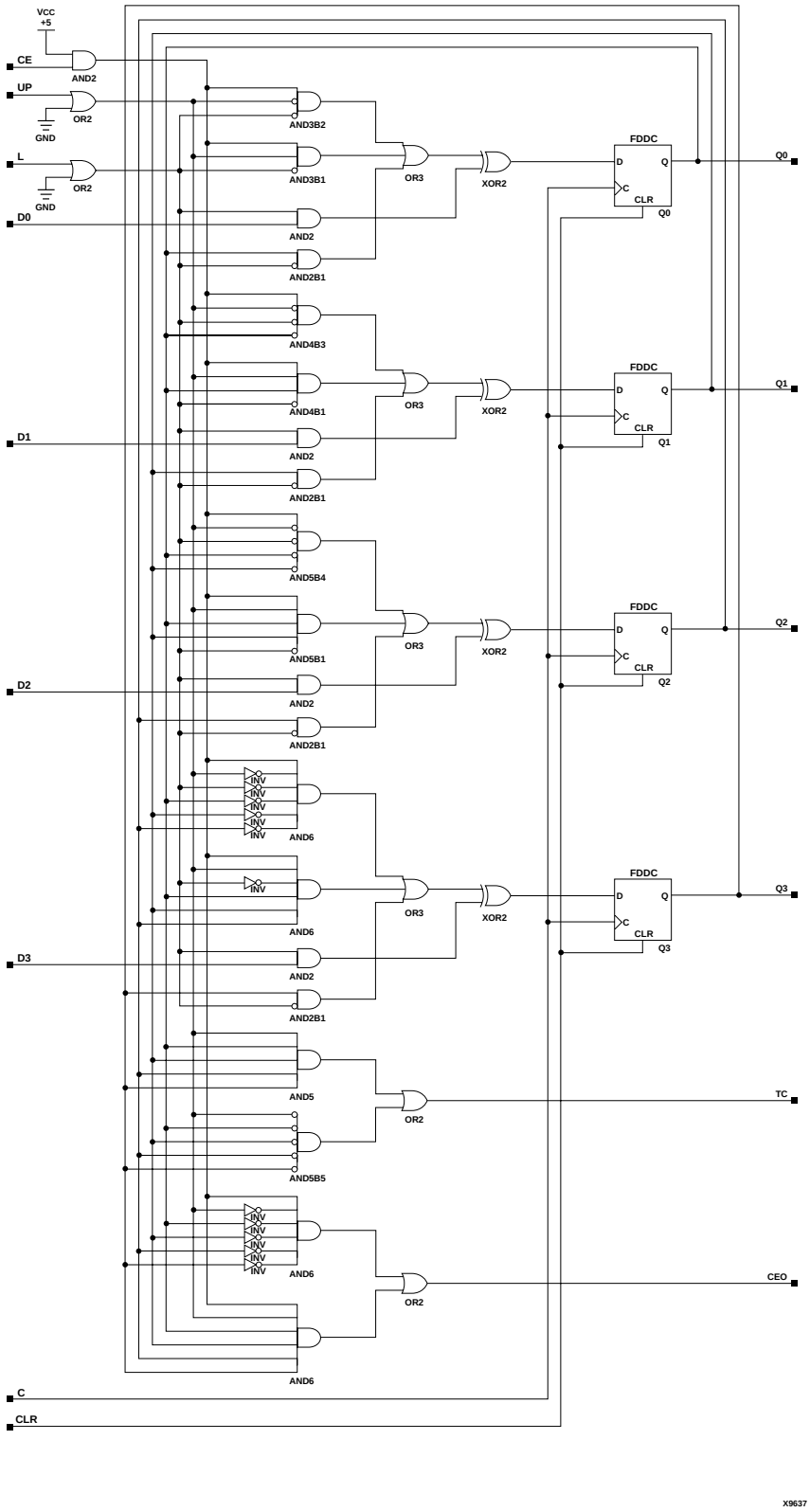
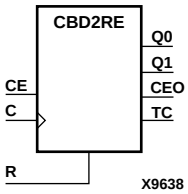


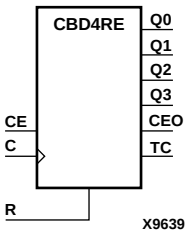
Figure 4-20 CBD4CLED Implementation CoolRunner-II

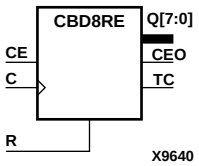
CBD2RE, CBD4RE, CBD8RE, CBD16RE

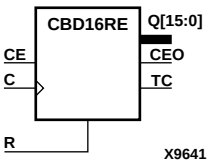
2-, 4-, 8-, 16-Bit Cascadable Dual Edge Triggered Binary Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro









CBD2RE, CBD4RE, CBD8RE, and CBD16RE are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, resettable, cascadable dual edge triggered binary counters. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs	
R	CE	C	Qz – Q0	TC	CEO
1	X	↑	0	0	0
1	X	↓	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO

z = 1 for CBD2RE; z = 3 for CBD4RE; z = 7 for CBD8RE; z = 15 for CBD16RE

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0)

CEO = TC • CE

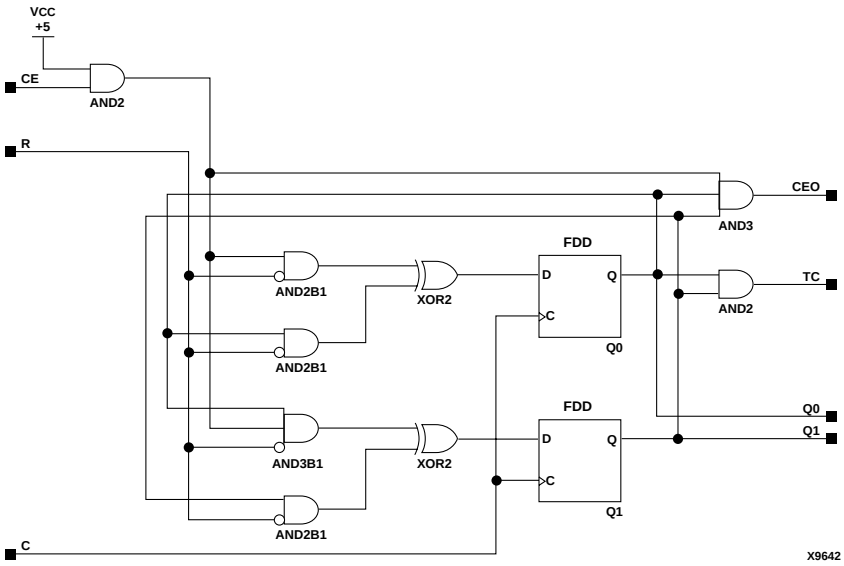


Figure 4-21 CBD2RE Implementation CoolRunner-II

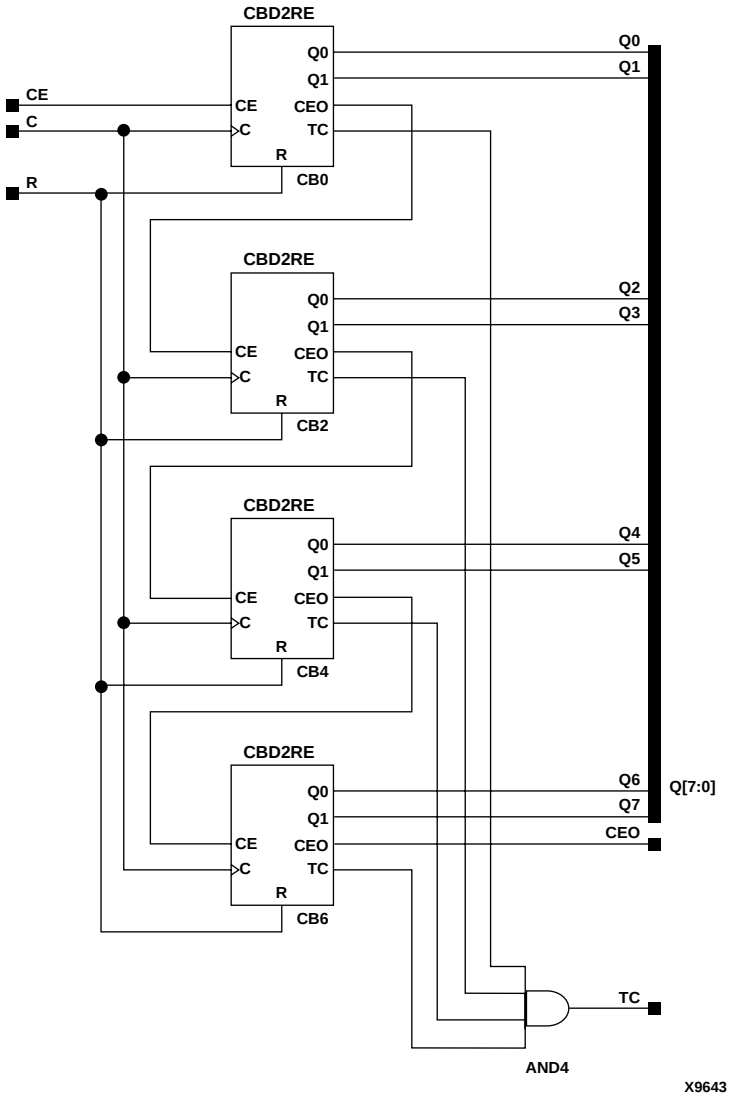
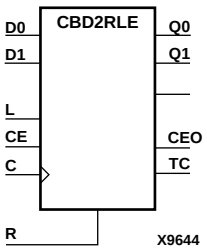


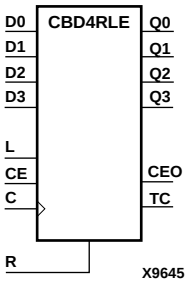
Figure 4-22 CBD8RE Implementation CoolRunner-II

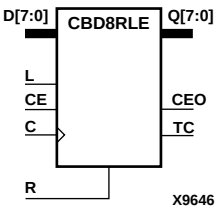
CBD2RLE, CBD4RLE, CBD8RLE, CBD16RLE

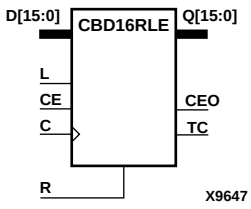
2-, 4-, 8-, 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro









CBD2RLE, CBD4RLE, CBD8RLE, and CBD16RLE are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R) is the highest priority input. The synchronous R, when High, overrides all other inputs and resets the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and by connecting the C, L, and R inputs in parallel. The maximum length of the counter is determined by the accumulated CE-to-CEO propagation delays versus the clock period. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs		
R	L	CE	C	Dz – D0	Qz – Q0	TC	CEO
1	X	X	↑	X	0	0	0
1	X	X	↓	X	0	0	0
0	1	X	↑	Dn	dn	TC	CEO
0	1	X	↓	Dn	dn	TC	CEO
1	X	X	↓	X	0	0	0
0	1	X	↓	Dn	dn	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

Inputs					Outputs		
R	**L**	**CE**	**C**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
0	0	1	↓	X	Inc	TC	CEO

z = 1 for CBD2RLE; z = 3 for CBD4RLE; z = 7 for CBD8RLE; z = 15 for CBD16RLE

dn = state of referenced input (Dn) one setup time prior to active clock transition

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEO = TC • CE

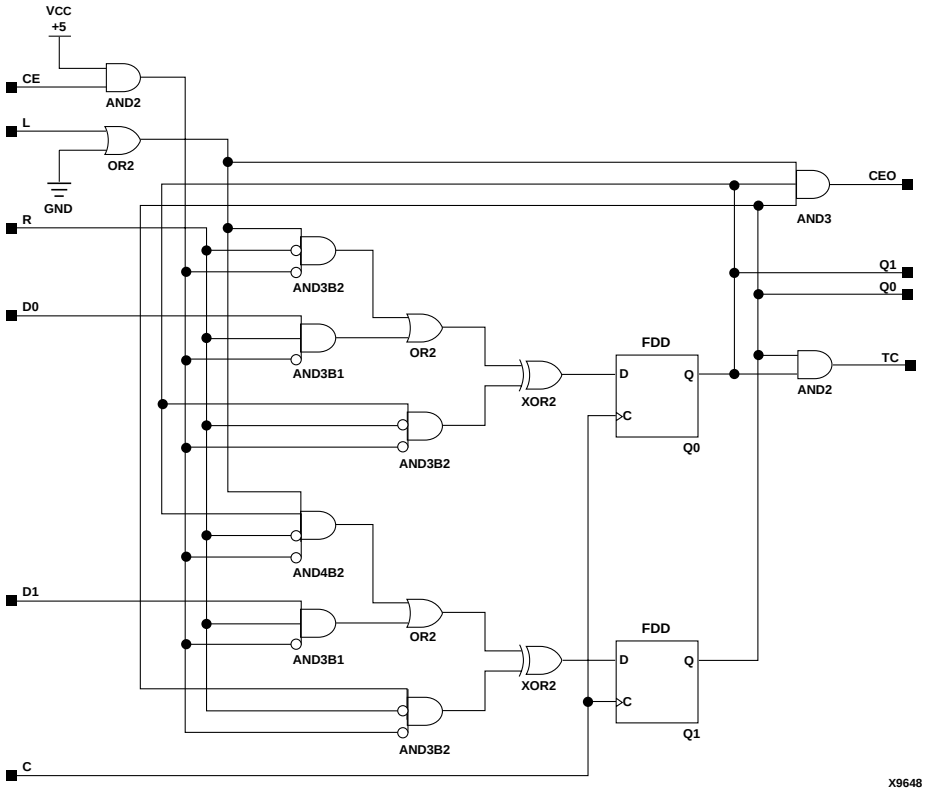


Figure 4-23 CBD2RLE Implementation CoolRunner-II

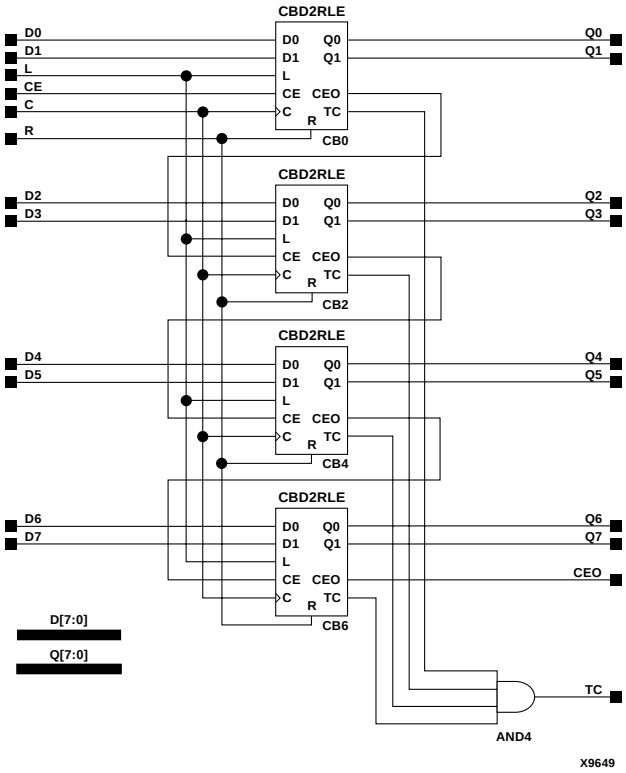
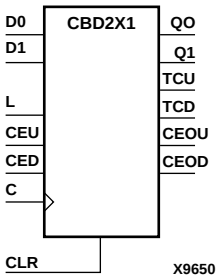


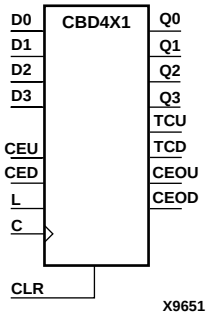
Figure 4-24 CBD8RLE Implementation CoolRunner-II

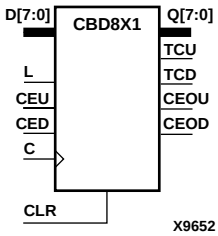
CBD2X1, CBD4X1, CBD8X1, CBD16X1

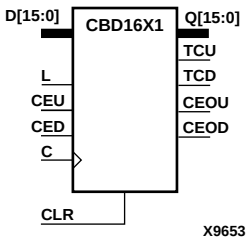
2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro









CBD2X1, CBD4X1, CBD8X1, and CBD16X1 are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. These counters have separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in the CoolRunner-II architecture.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

In CoolRunner-II, the maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs				
CLR	**L**	**CEU**	**CED**	**C**	**Dz–D0**	**Qz–Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid

z = 1 for CBD2X1; z = 3 for CBD4X1; z = 7 for CBD8X1; z = 15 for CBD16X1

dn = state of referenced input (Dn) one setup time prior to active clock transition

TCU = Qz • Q(z-1) • Q(z-2) • ... • Q0

TCD = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEOU = TCU • CEU

CEOD = TCD • CED

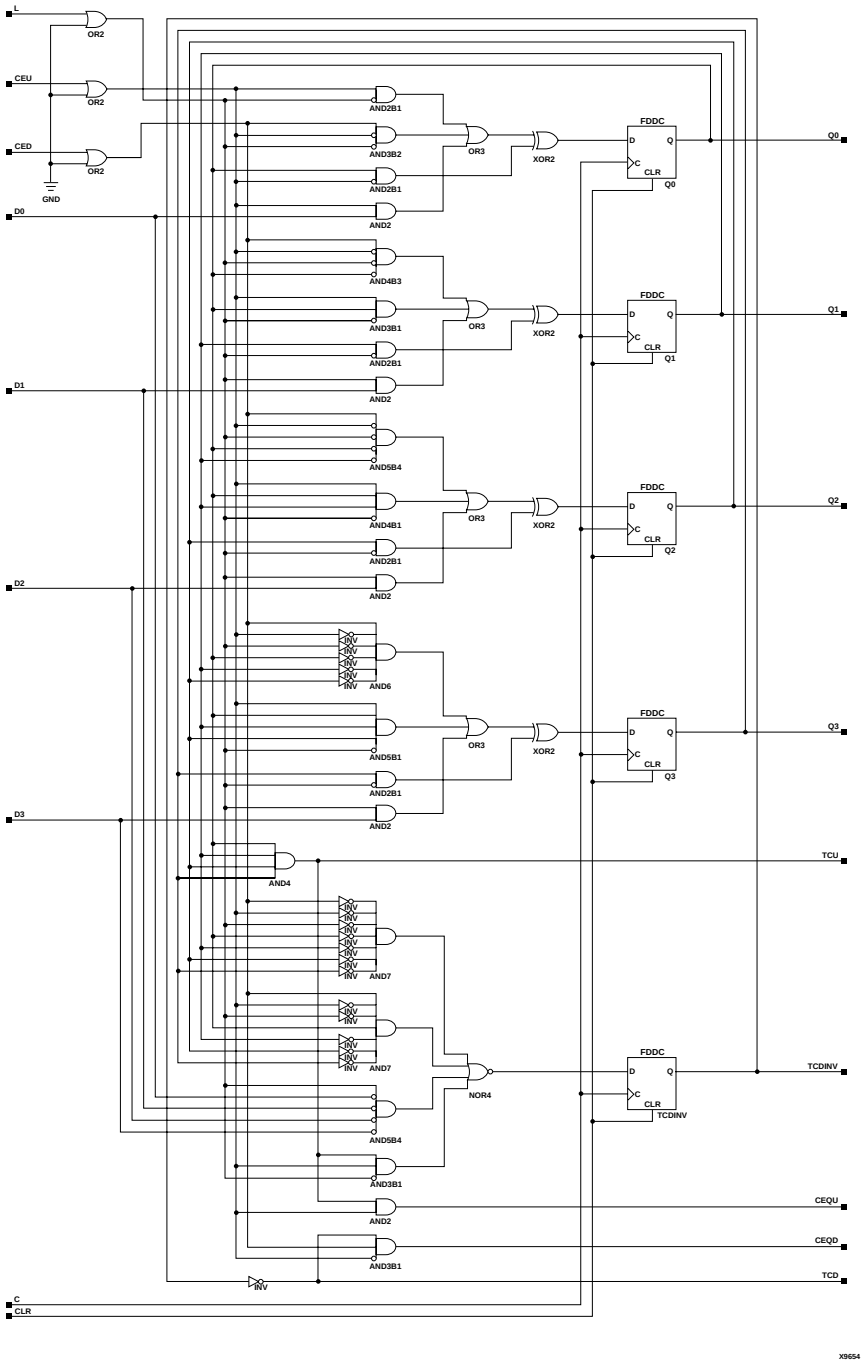
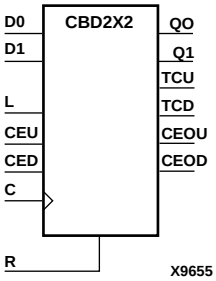


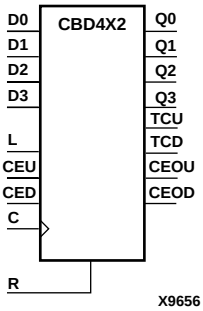
Figure 4-25 CBD4X1 Implementation CoolRunner-II

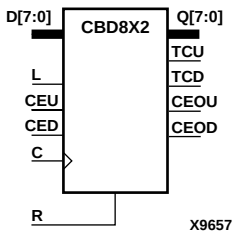
CBD2X2, CBD4X2, CBD8X2, CBD16X2

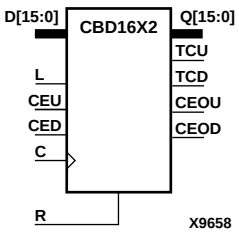
2-, 4-, 8-, and 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro









CBD2X2, CBD4X2, CBD8X2, and CBD16X2 are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, loadable, resettable, bidirectional dual edge triggered binary counters. These counters have separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in the CoolRunner-II architecture.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

In CoolRunner-II, the maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs				
R	**L**	**CEU**	**CED**	**C**	**Dz – D0**	**Qz – Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	↑	X	0	0	1	0	CEOD
1	X	X	X	↓	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid

z = 1 for CBD2X2; z = 3 for CBD4X2; z = 7 for CBD8X2; z = 15 for CBD16X2

d = state of referenced input (Dn) one setup time prior to active clock transition

TCU = Qz • Q(z-1) • Q(z-2) • ... • Q0

TCD = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEOU = TCU • CEU

CEOD = TCD • CED

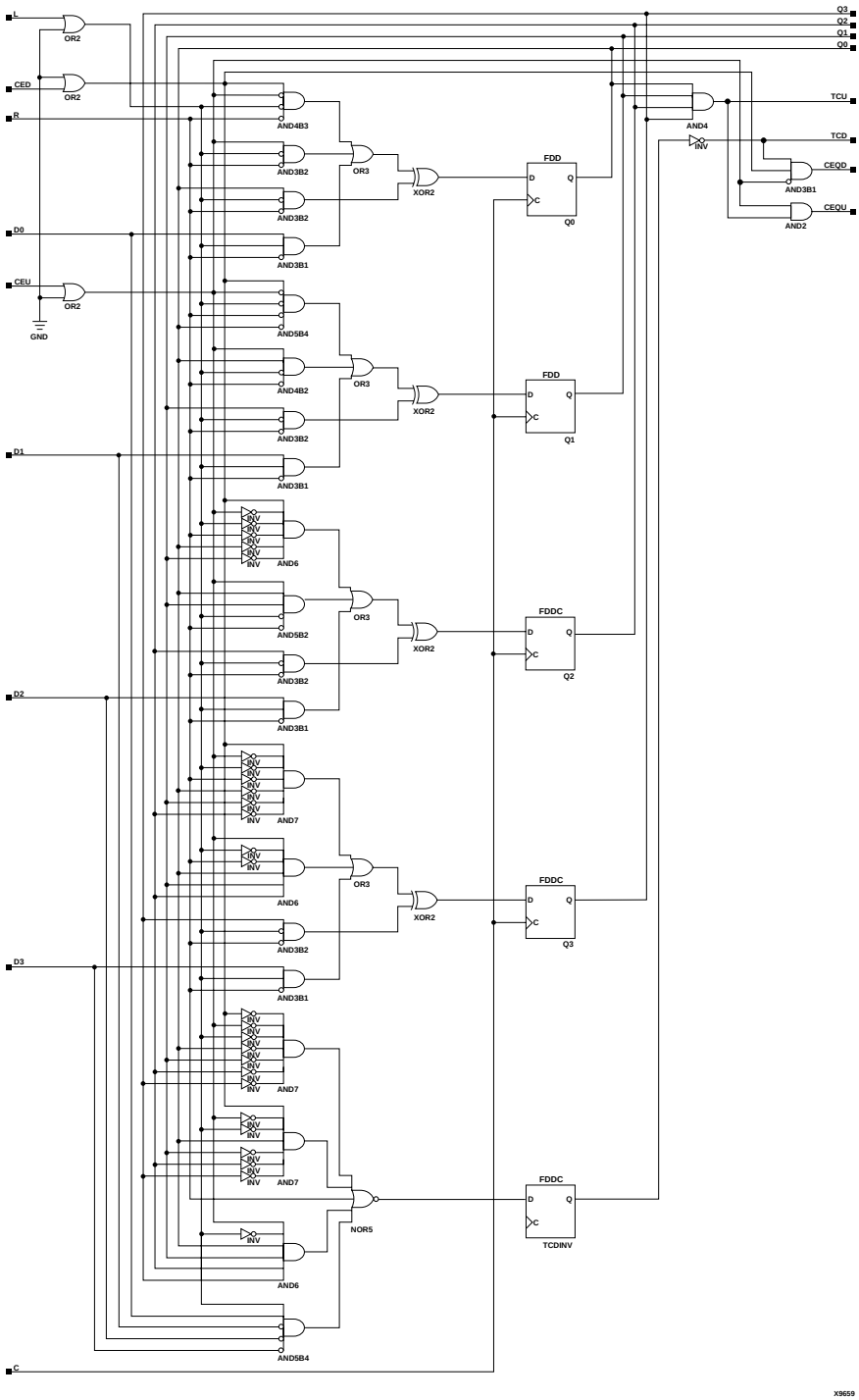
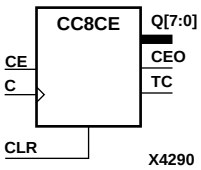


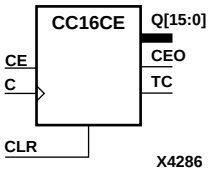
Figure 4-26 CBD4X2 Implementation CoolRunner-II

CC8CE, CC16CE

8-, 16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A





CC8CE and CC16CE are, respectively, 8- and 16-bit (stage), asynchronous, clearable, cascadable binary counters. These counters are implemented using carry logic with relative location constraints to ensure efficient placement of logic. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, with Low outputs, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs		
CLR	CE	C	Qz – Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

z = 7 for CC8CE; z = 15 for CC16CE

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEO = TC • CE

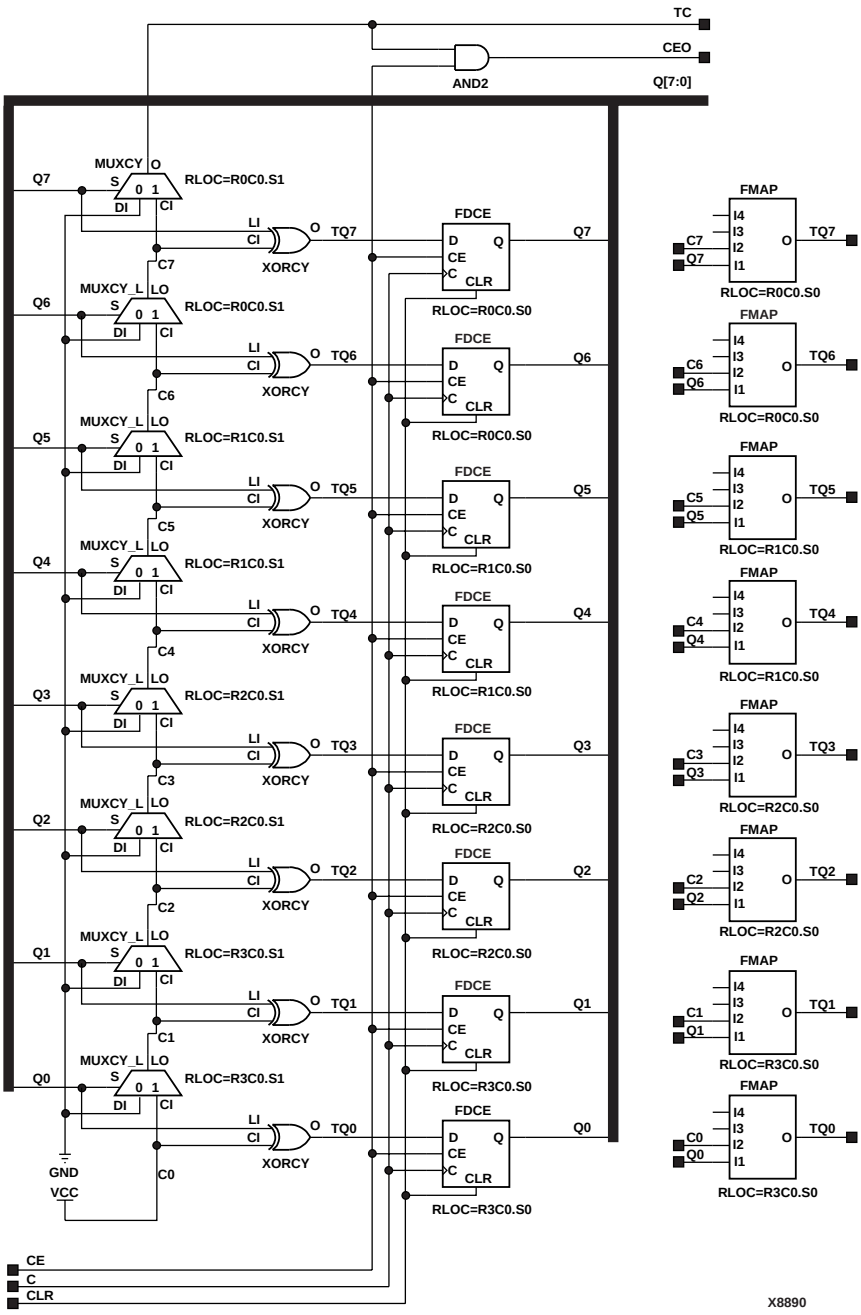


Figure 4-27 CC8CE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

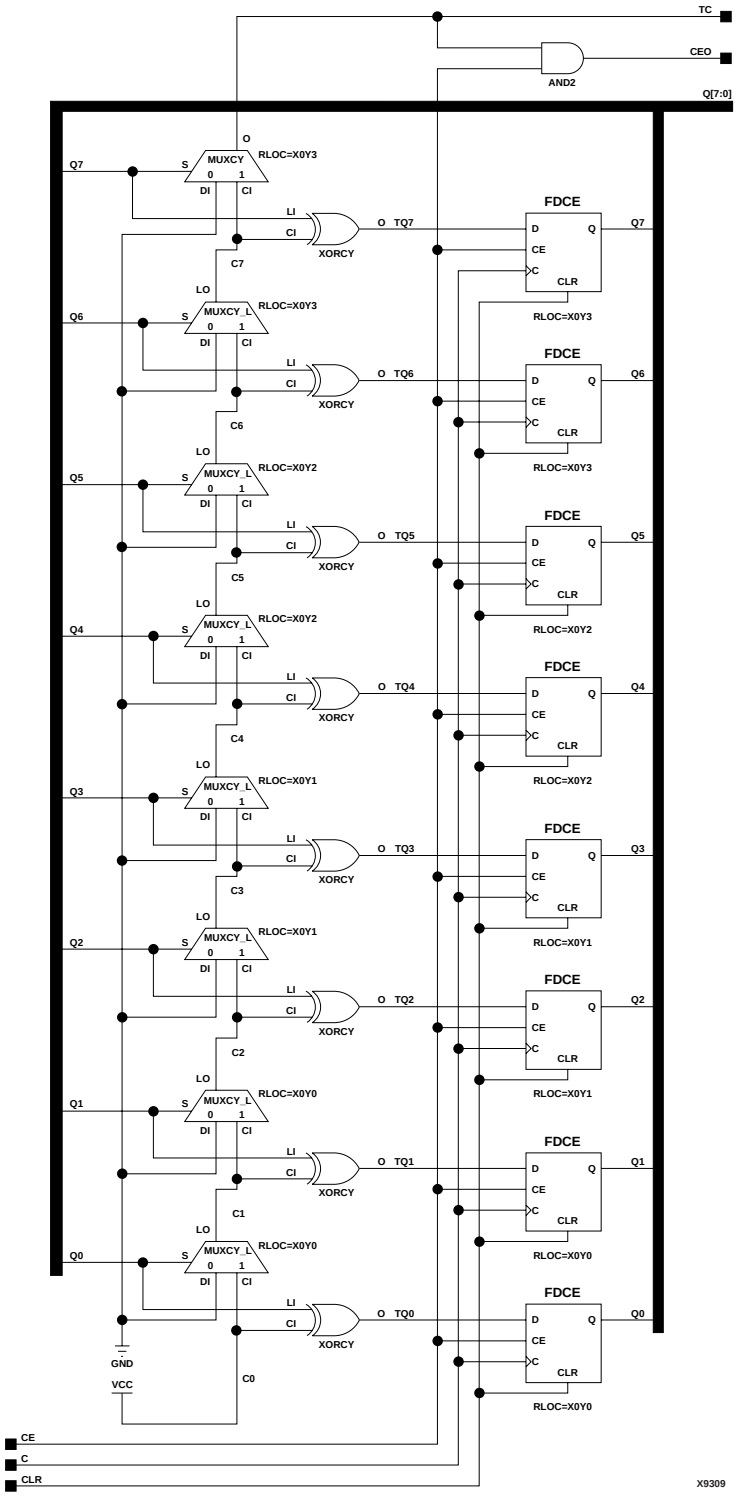
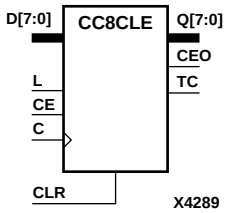


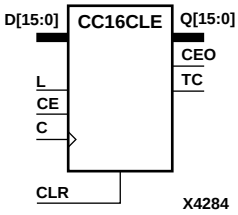
Figure 4-28 CC8CE Implementation Virtex-II, Virtex-II PRO

CC8CLE, CC16CLE

8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A





CC8CLE and CC16CLE are, respectively, 8- and 16-bit (stage), synchronously loadable, asynchronously clearable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient placement of logic.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, with Low output, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs		
CLR	L	CE	C	Dz – D0	Qz – Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	dn	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

z = 7 for CC8CLE; z = 15 for CC16CLE

dn = state of referenced input (Dn) one setup time prior to active clock transition

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEO = TC • CE

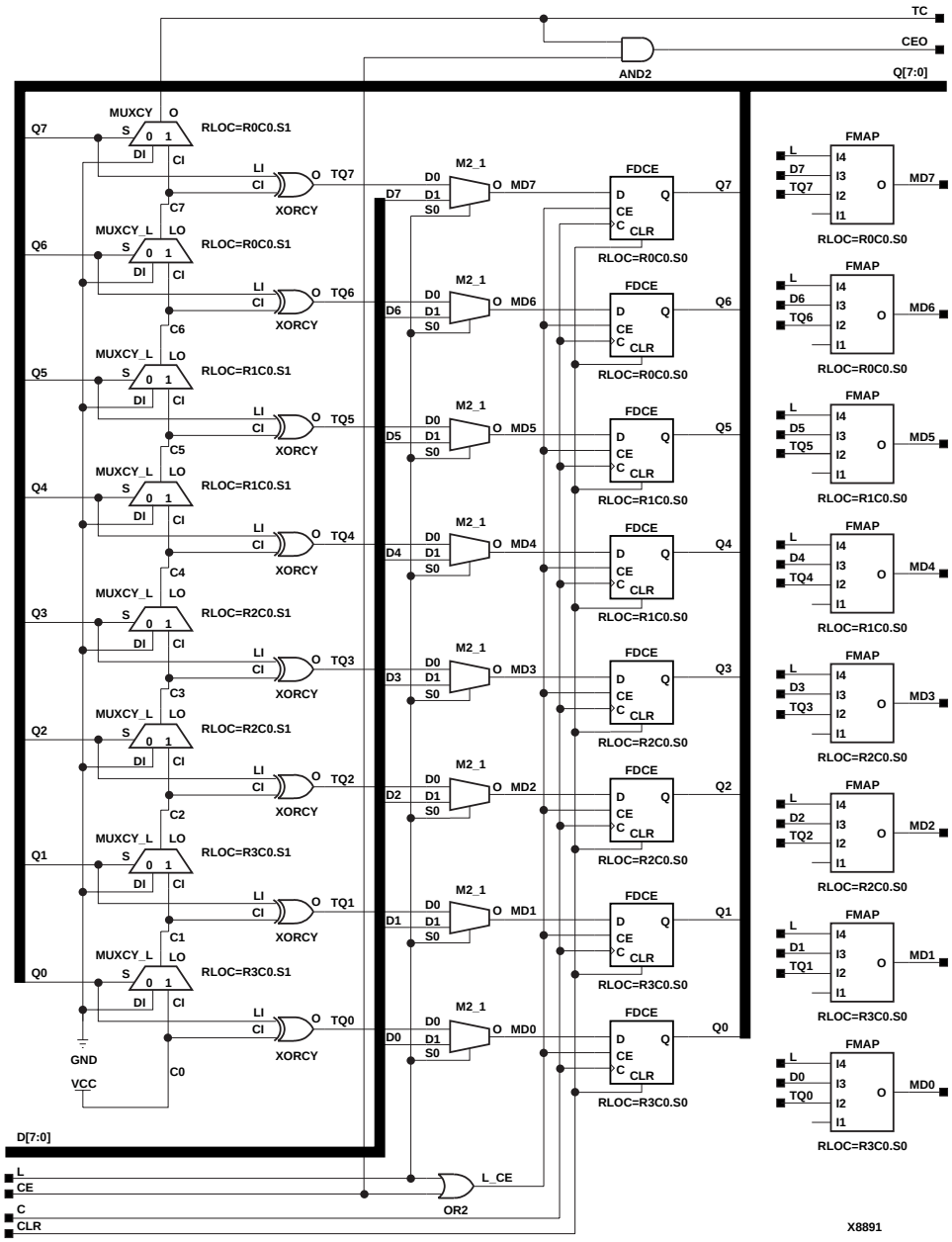


Figure 4-29 CC8CLE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

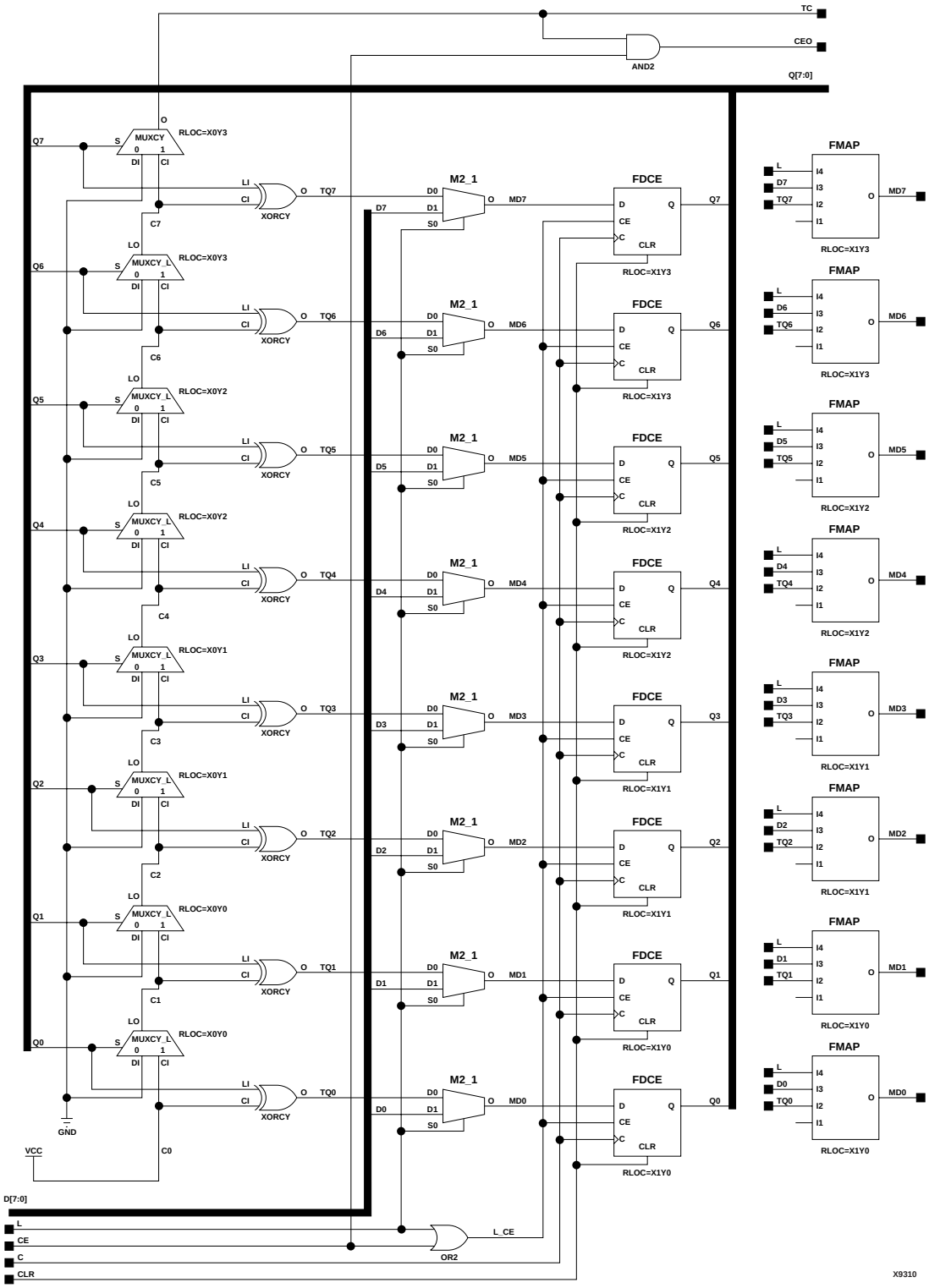
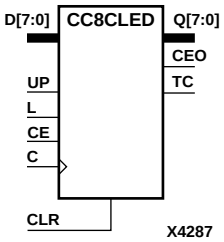


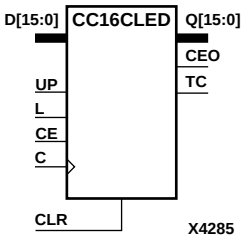
Figure 4-30 CC8CLE Implementation Virtex-II, Virtex-II PRO

CC8CLED, CC16CLED

8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A





CC8CLED and CC16CLED are, respectively, 8- and 16-bit (stage), synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counters. These counters are implemented using carry logic with relative location constraints, which assures most efficient logic placement.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low. To cascade counters, the count enable out (CEO) output of each counter is connected to the CE pin of the next stage. The clock, UP, L, and CLR inputs are connected in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, outputs Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	dn	TC	CEO
0	0	0	X	X	X	No Chg	No Chg	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

z = 7 for CC8CLED; z = 15 for CC16CLED

dn = state of referenced input (Dn) one setup time prior to active clock transition

TC = (Qz • Q(z-1) • Q(z-2) • ... • Q0 • UP) + (Qz • Q(z-1) • Q(z-2) • ... • Q0 • UP)

CEO = TC • CE

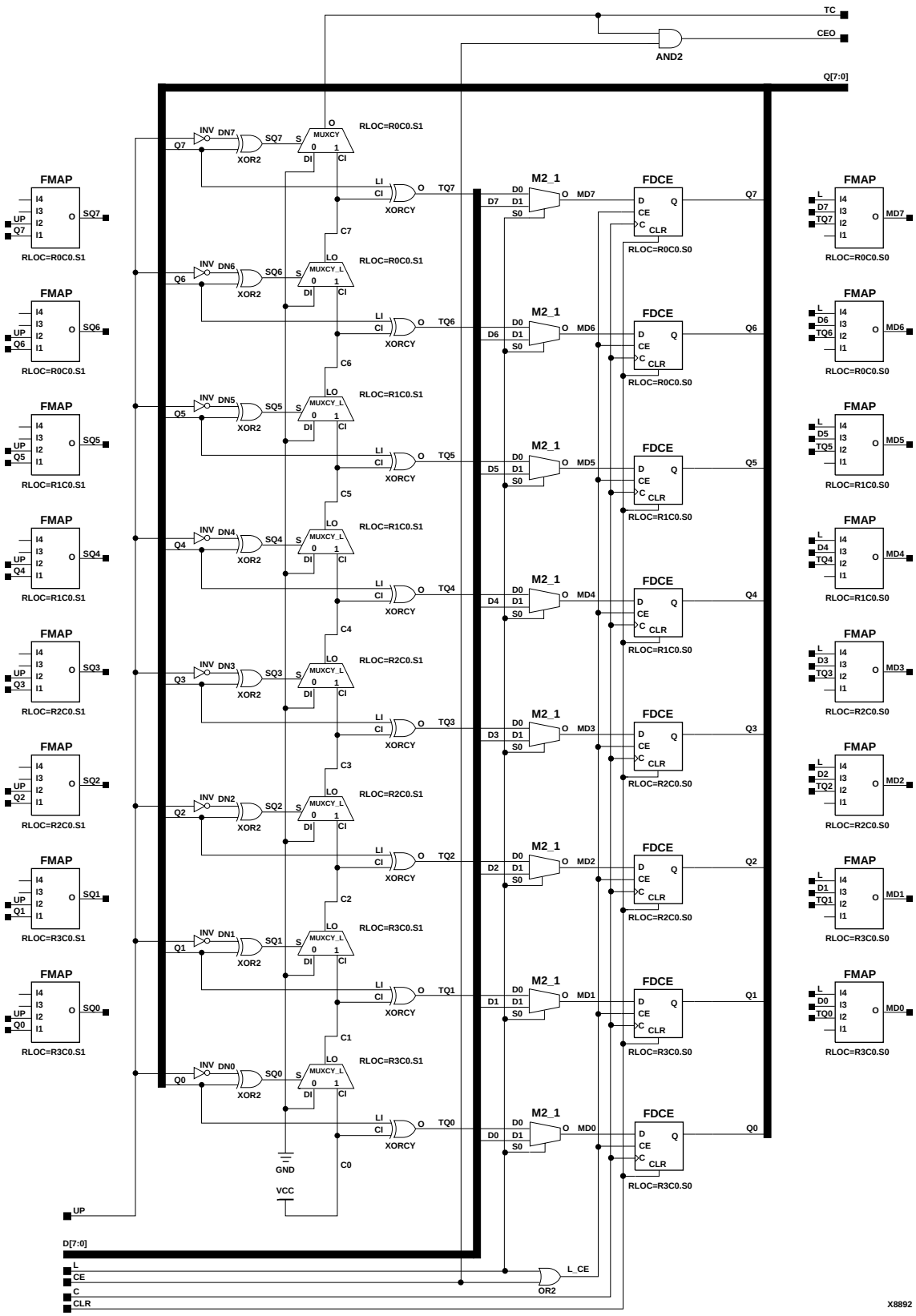


Figure 4-31 CC8CLED Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

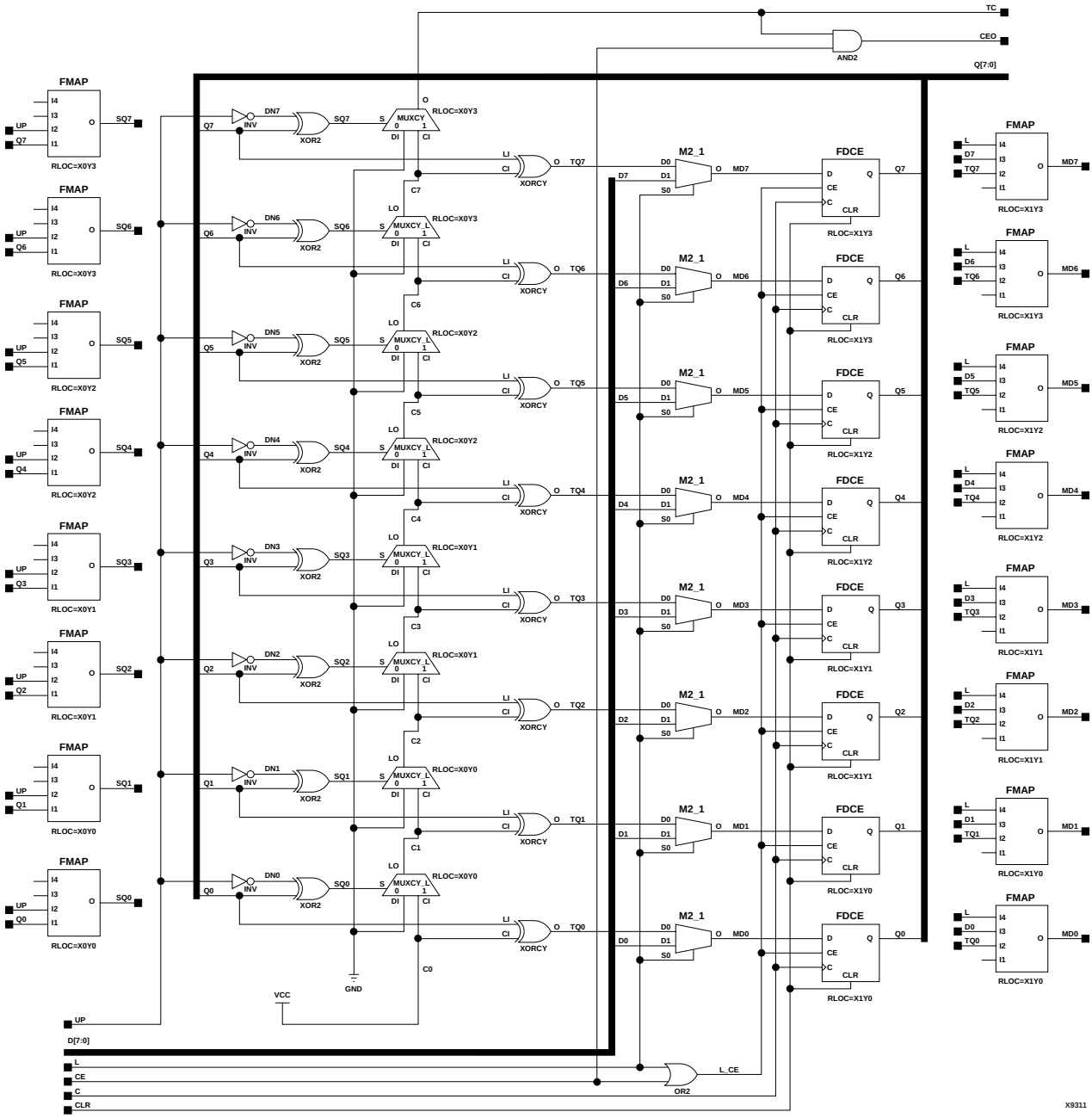
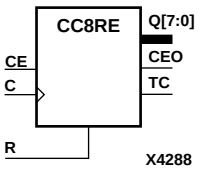


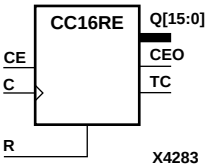
Figure 4-32 CC8CLED Implementation Virtex-II, Virtex-II PRO

CC8RE, CC16RE

8-, 16-Bit Cascadable Binary Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A





CC8RE and CC16RE are, respectively, 8- and 16-bit (stage), synchronous, resettable, cascadable binary counters. These counters are implemented using carry logic with relative location constraints to ensure efficient placement of logic. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, with Low outputs, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs		
R	CE	C	Qz – Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

z = 7 for CC8RE; z = 15 for CC16RE

TC = Qz • Q(z-1) • Q(z-2) • ... • Q0 • CE

CEO = TC • CE

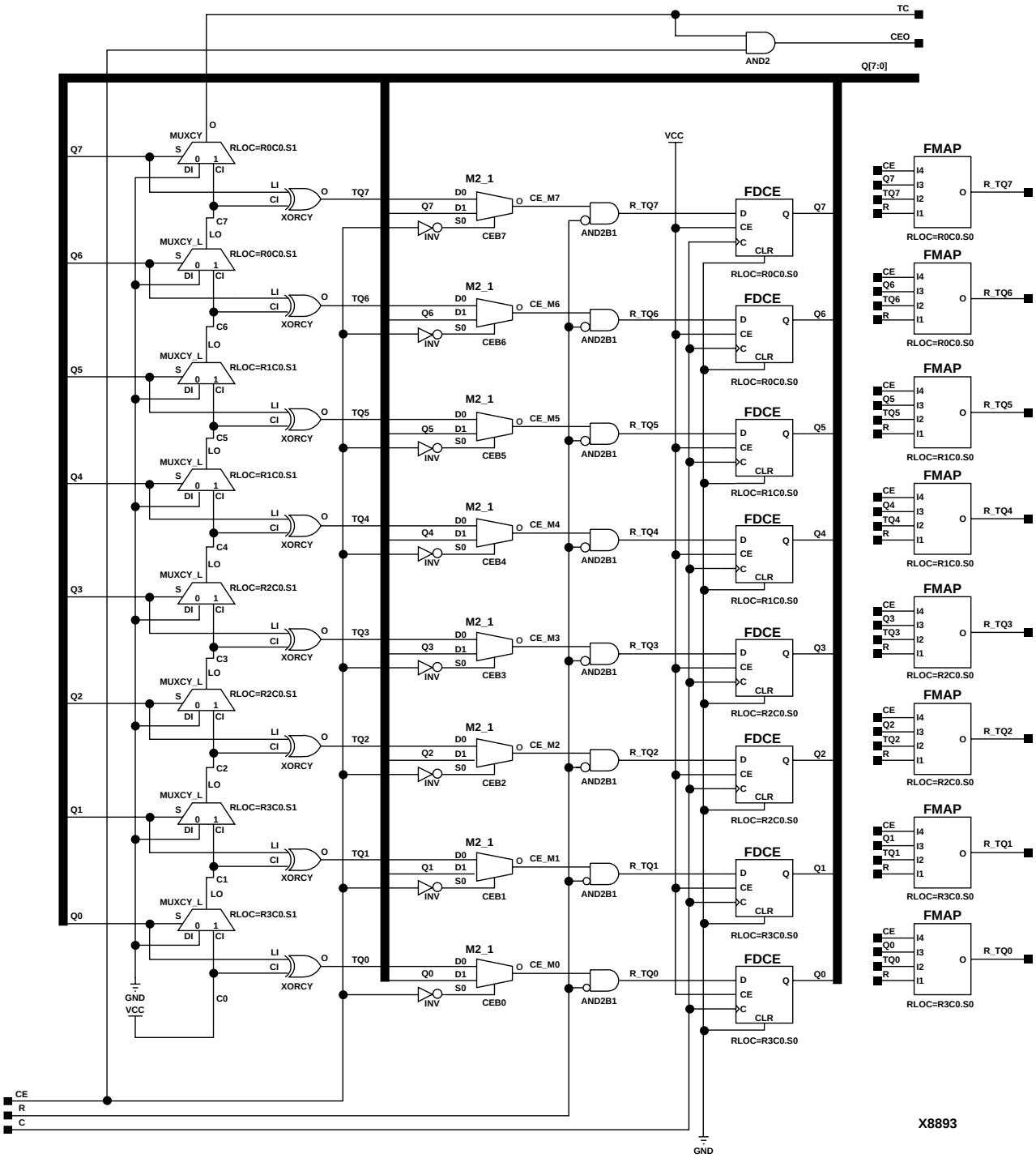


Figure 4-33 CC8RE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

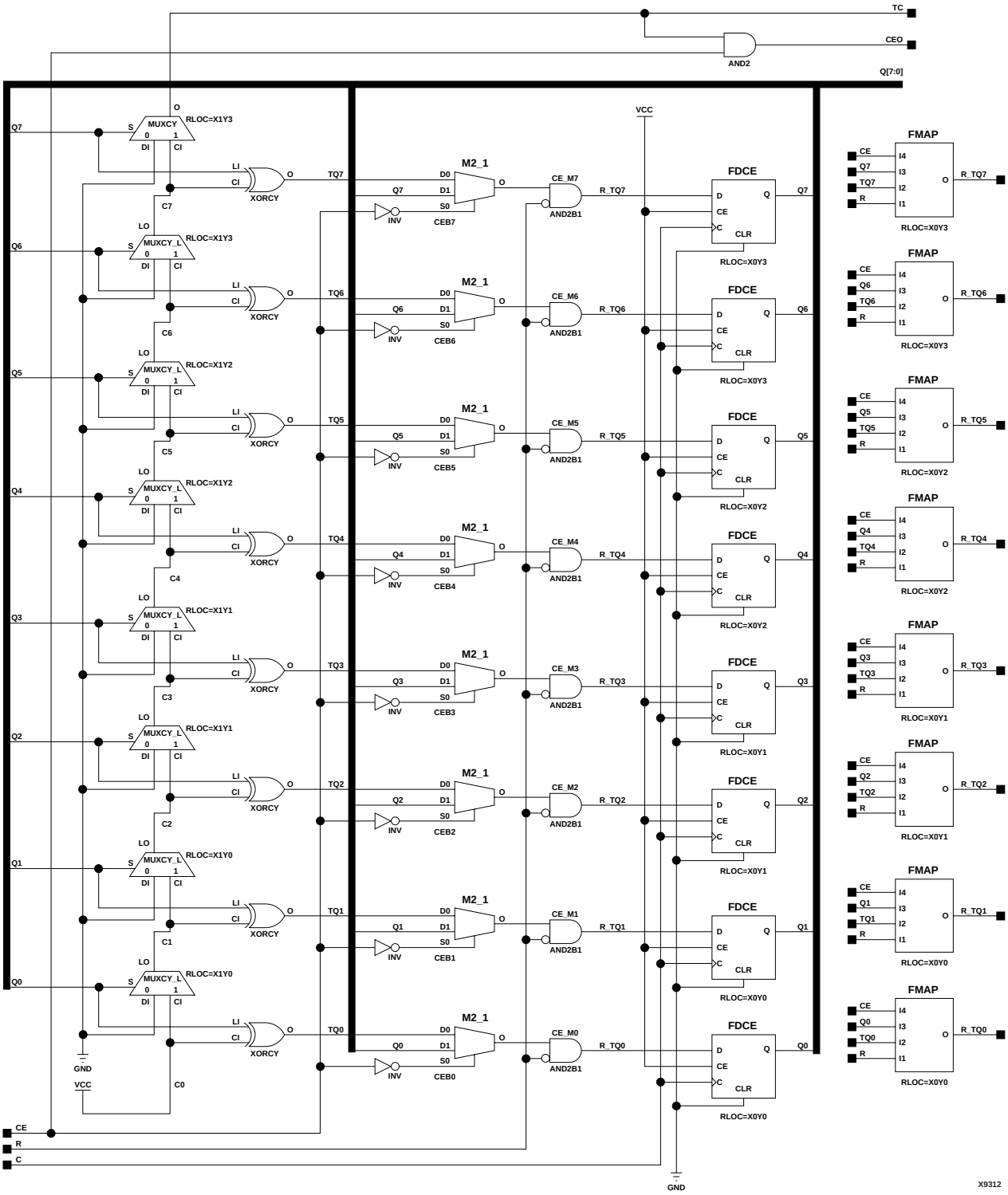
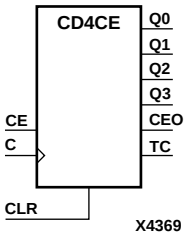


Figure 4-34 CC8RE Implementation Virtex-II, Virtex-II PRO

CD4CE

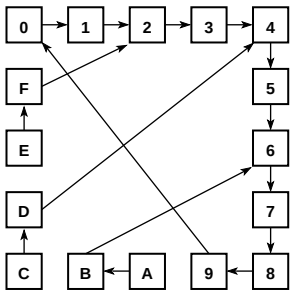
4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



CD4CE is a 4-bit (stage), asynchronous, clearable, cascadable binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, as shown in the following state diagram. For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the CLR and clock inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse to the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs					
CLR	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	1	X	1	0	0	1	1	1

TC = Q3•!Q2•!Q1•Q0

CEO = TC•CE

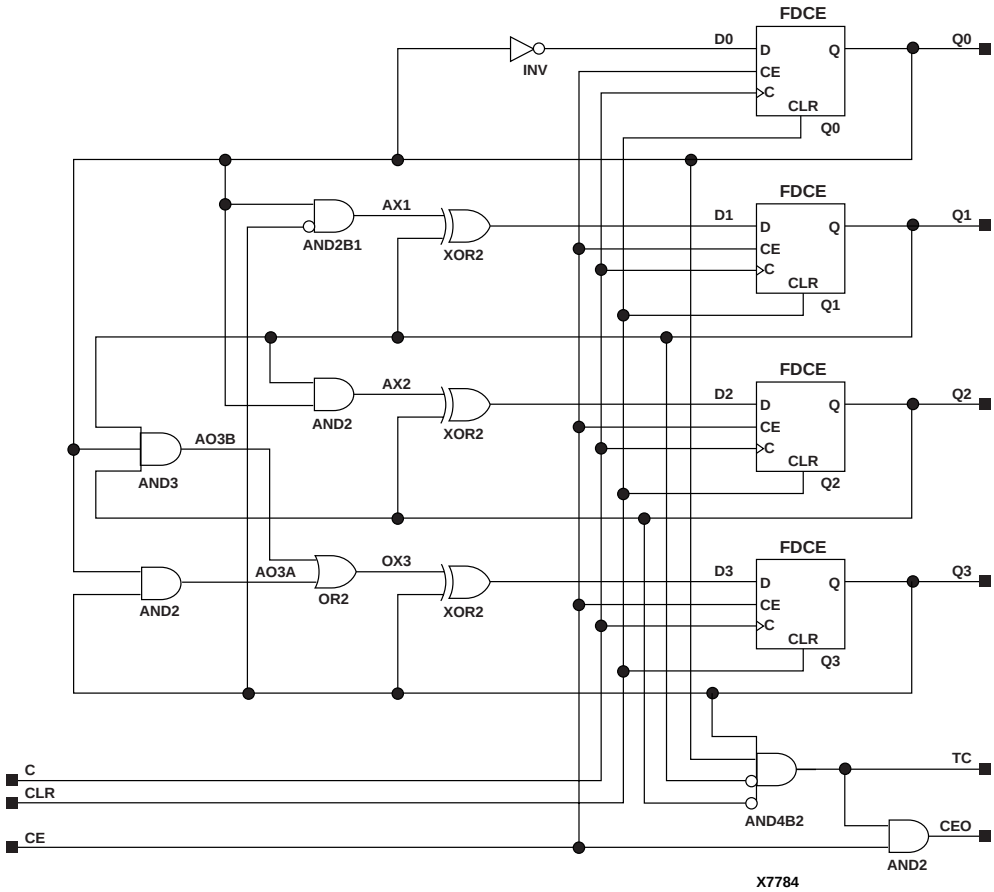


Figure 4-35 CD4CE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

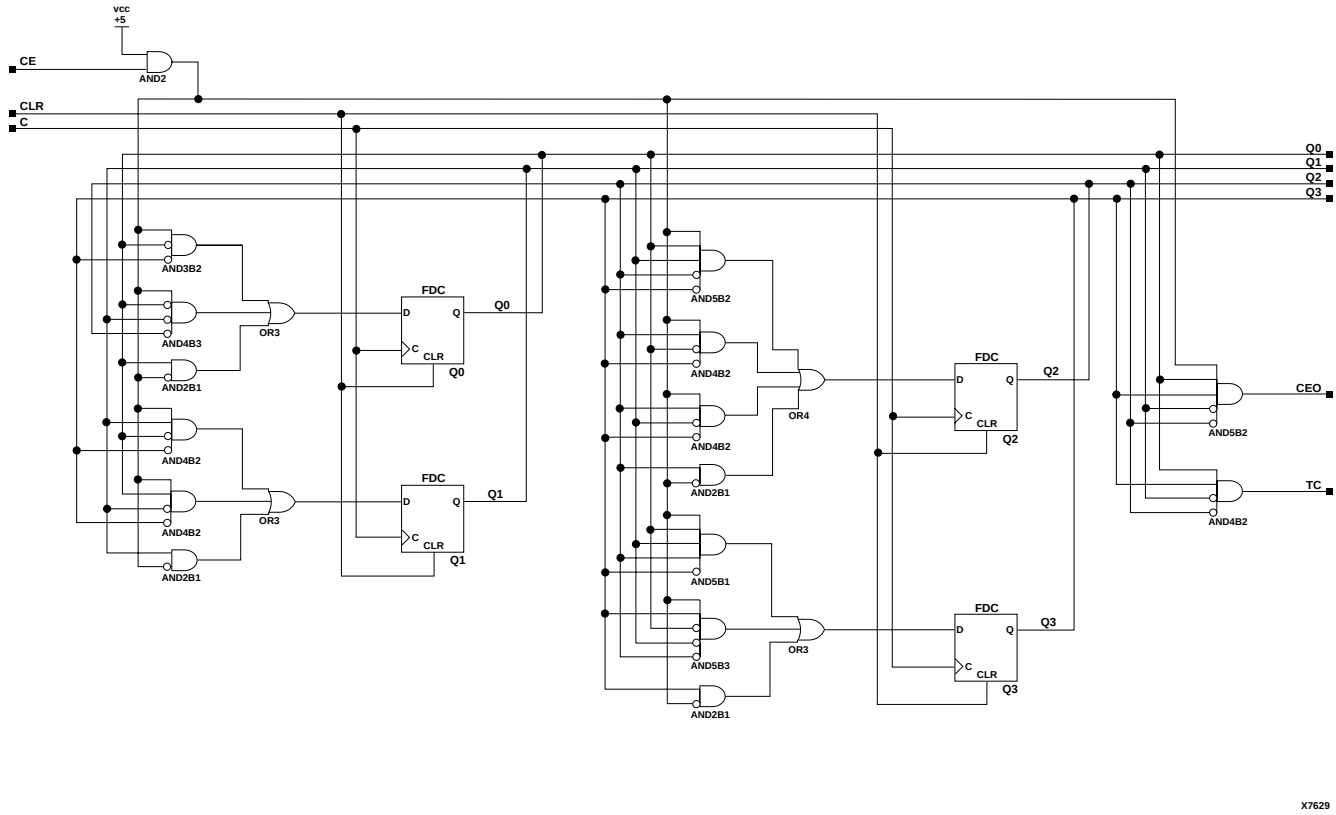
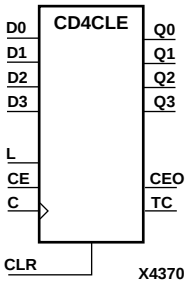


Figure 4-36 CD4CE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

CD4CLE

4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear

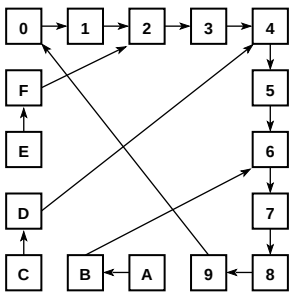
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



CD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, as shown in the following state diagram.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the CLR, L, and C inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs					
CLR	**L**	**CE**	**D3 – D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 – D0	↑	d3	d2	d1	d0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	0	1	X	X	1	0	0	1	1	1

d = state of referenced input one setup time prior to active clock transition

TC = Q3•!Q2•!Q1•Q0

CEO = TC•CE

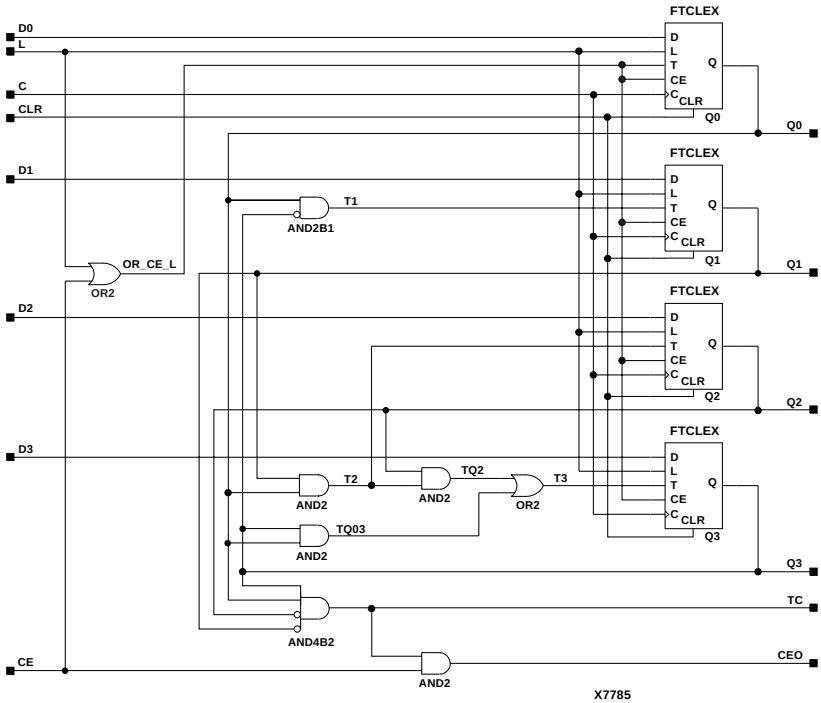


Figure 4-37 CD4CLE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

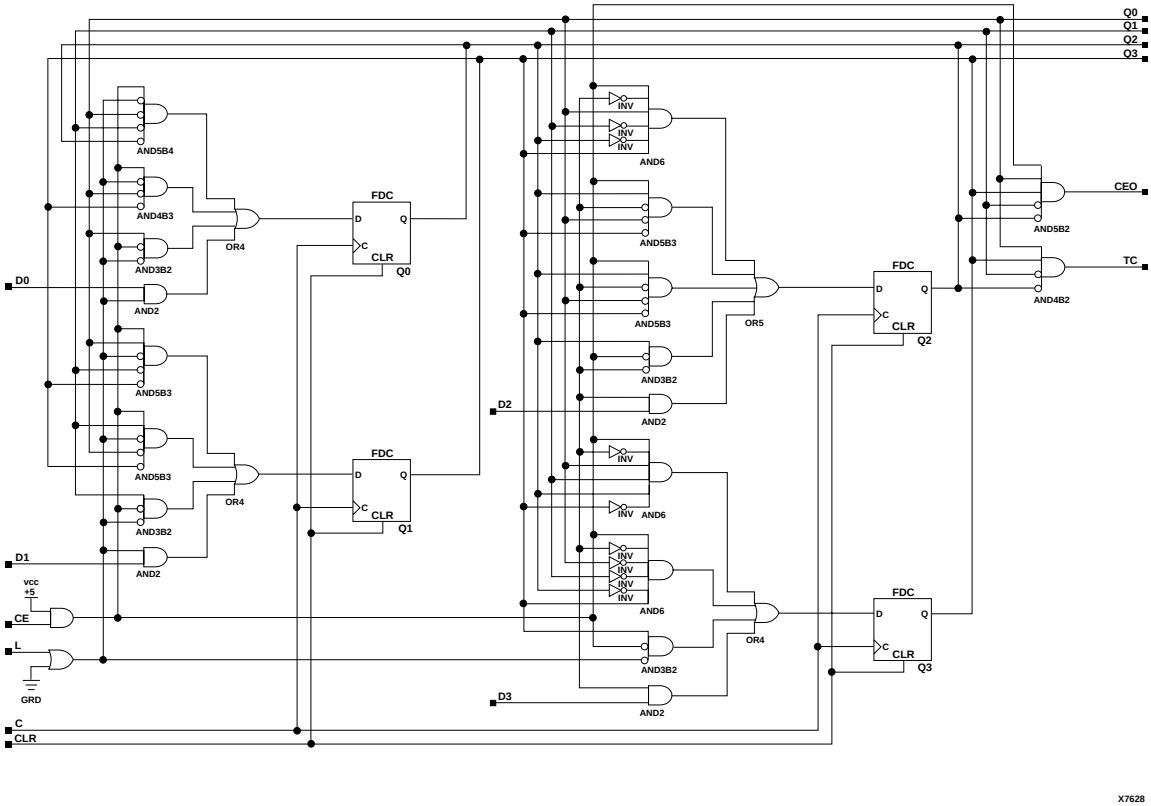
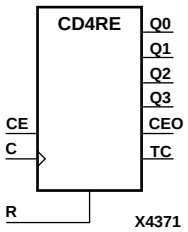


Figure 4-38 CD4CLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

CD4RE

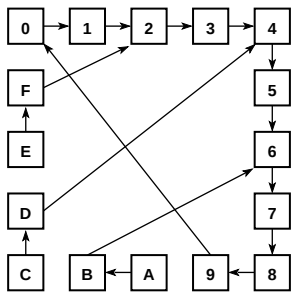
4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



CD4RE is a 4-bit (stage), synchronous, resettable, cascadable binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, as shown in the following state diagram. For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the R and clock inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs					
R	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	↑	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	1	X	1	0	0	1	1	1

TC = Q3•!Q2•!Q1•Q0

CEO = TC•CE

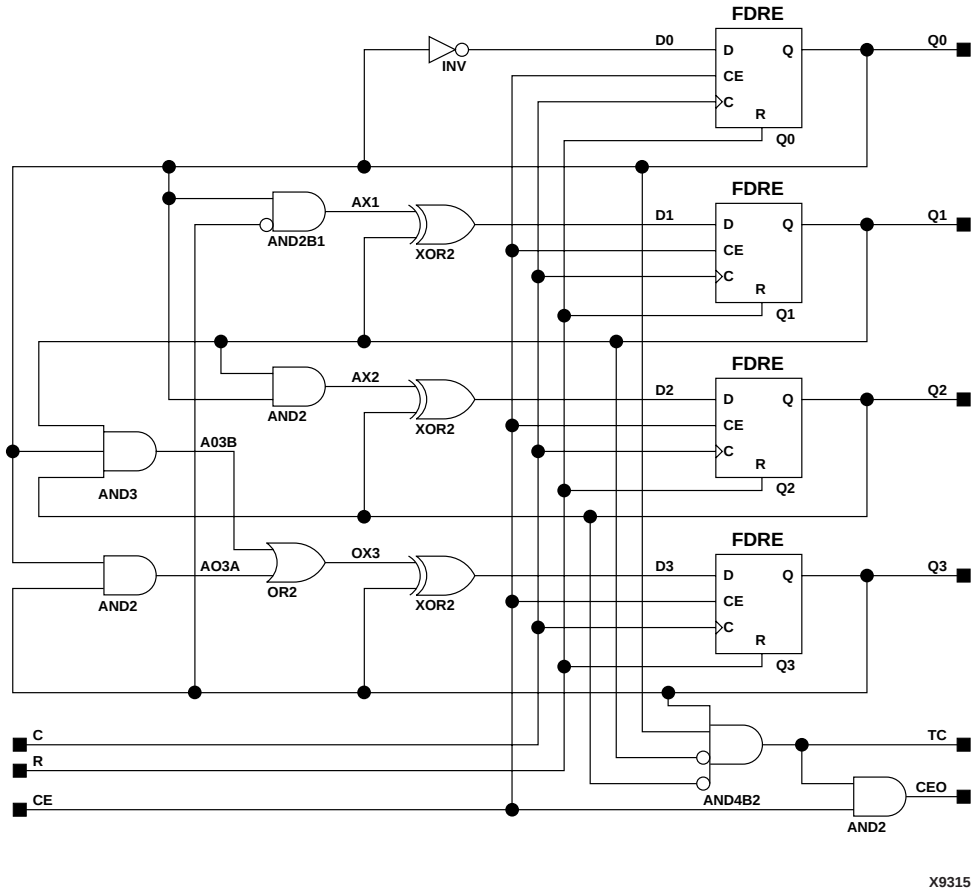


Figure 4-39 CD4RE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

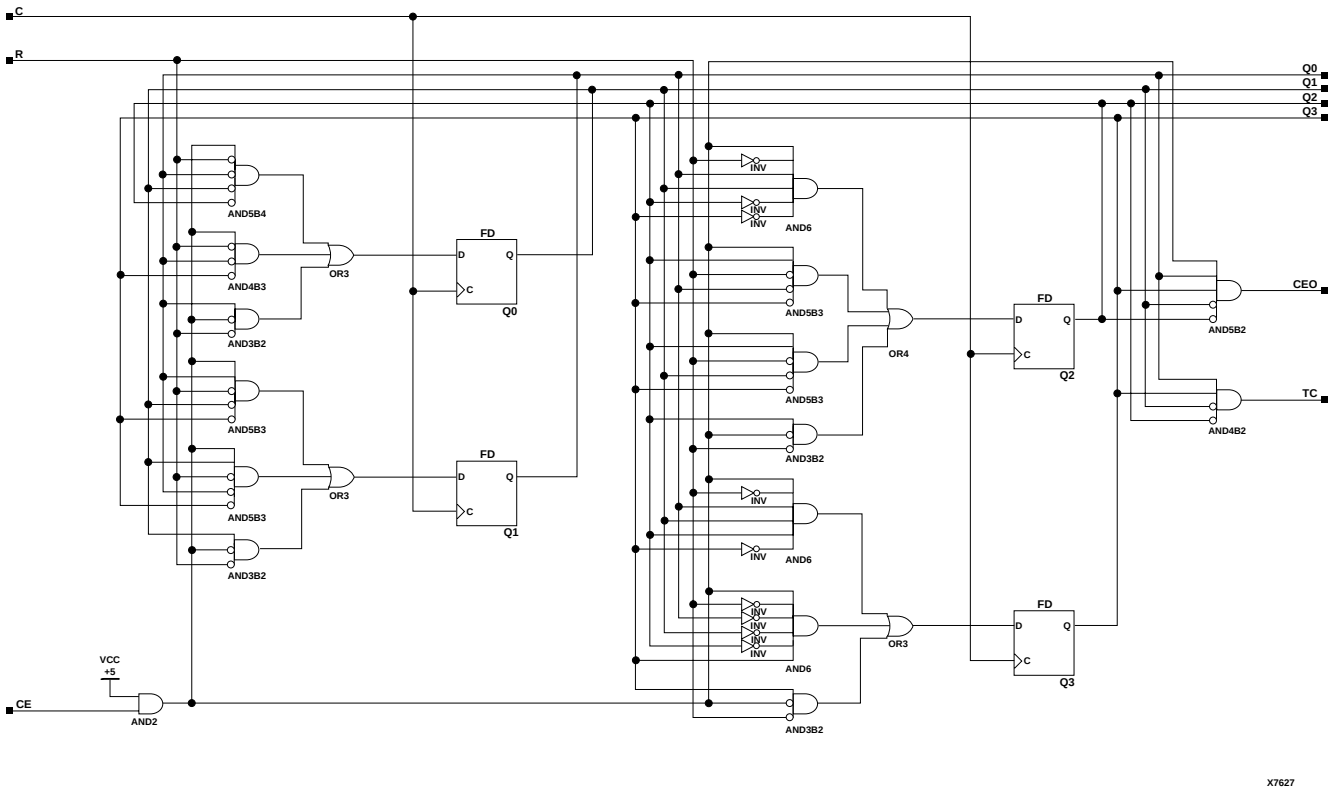
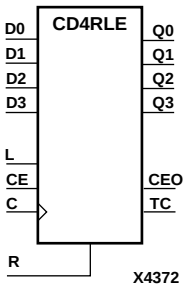


Figure 4-40 CD4RE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

CD4RLE

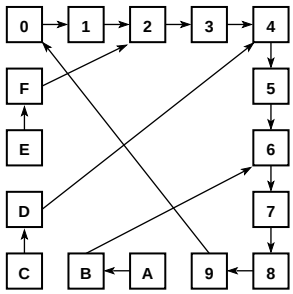
4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



CD4RLE is a 4-bit (stage), synchronous, loadable, resettable, binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, as shown in the following state diagram. For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the R, L, and C inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs					
R	L	CE	D3 – D0	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	X	↑	0	0	0	0	0	0
0	1	X	D3 – D0	↑	d3	d2	d1	d0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	0	1	X	X	1	0	0	1	1	1

d = state of referenced input one setup time prior to active clock transition

TC = Q3•!Q2•!Q1•Q0

CEO = TC•CE

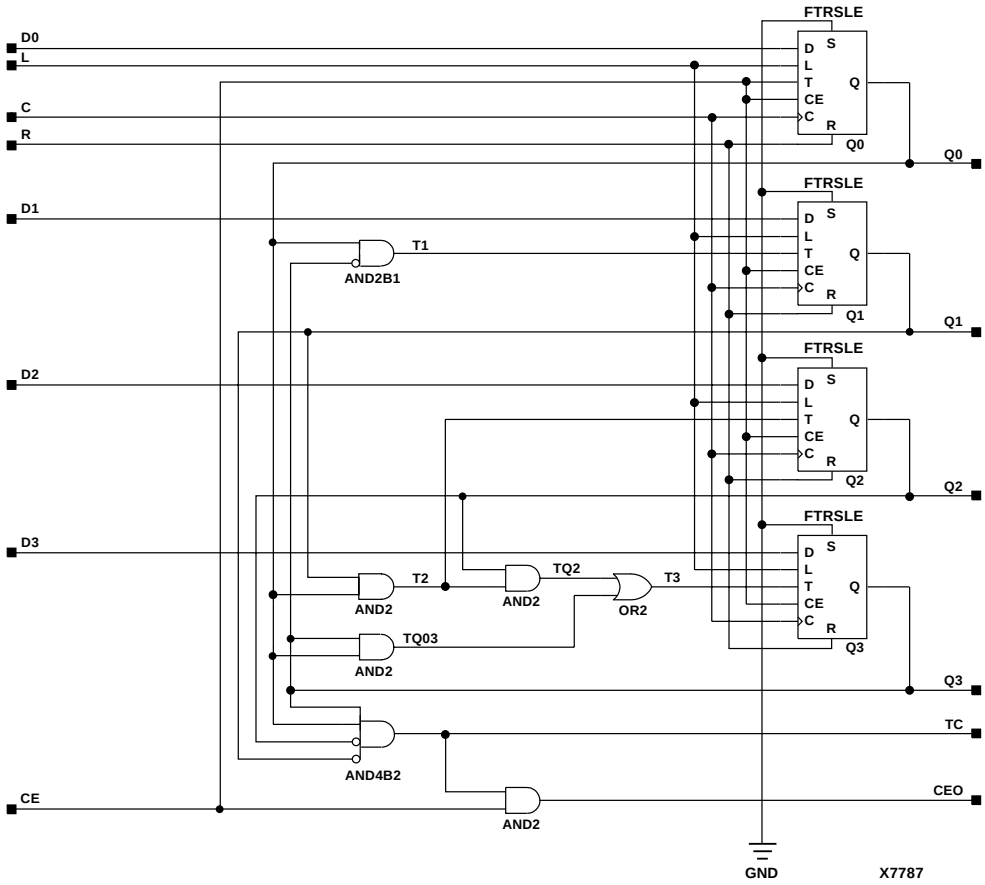


Figure 4-41 CD4RLE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

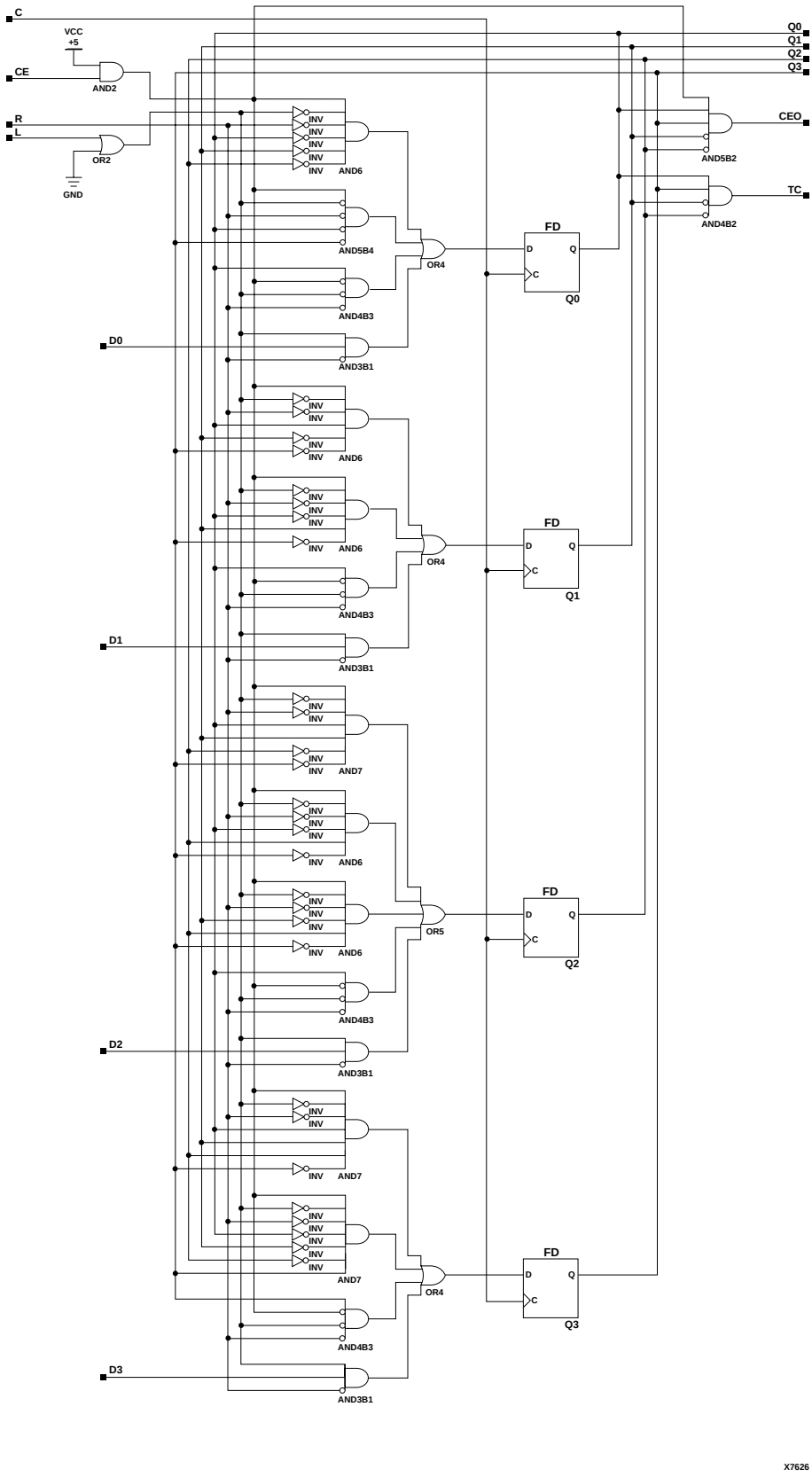
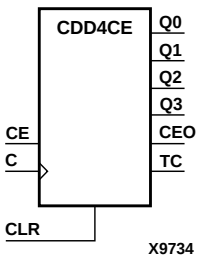


Figure 4-42 CD4RLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

CDD4CE

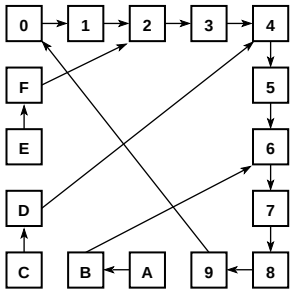
4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro



CD4CE is a 4-bit (stage), asynchronous, clearable, cascadable dual edge triggered Binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles, as shown in the following state diagram. The counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the CLR and clock inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse to the PRLD global net.

Inputs			Outputs					
CLR	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	1	↓	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	1	X	1	0	0	1	1	1

TC = Q3•!Q2•!Q1•Q0

CEO = TC•CE

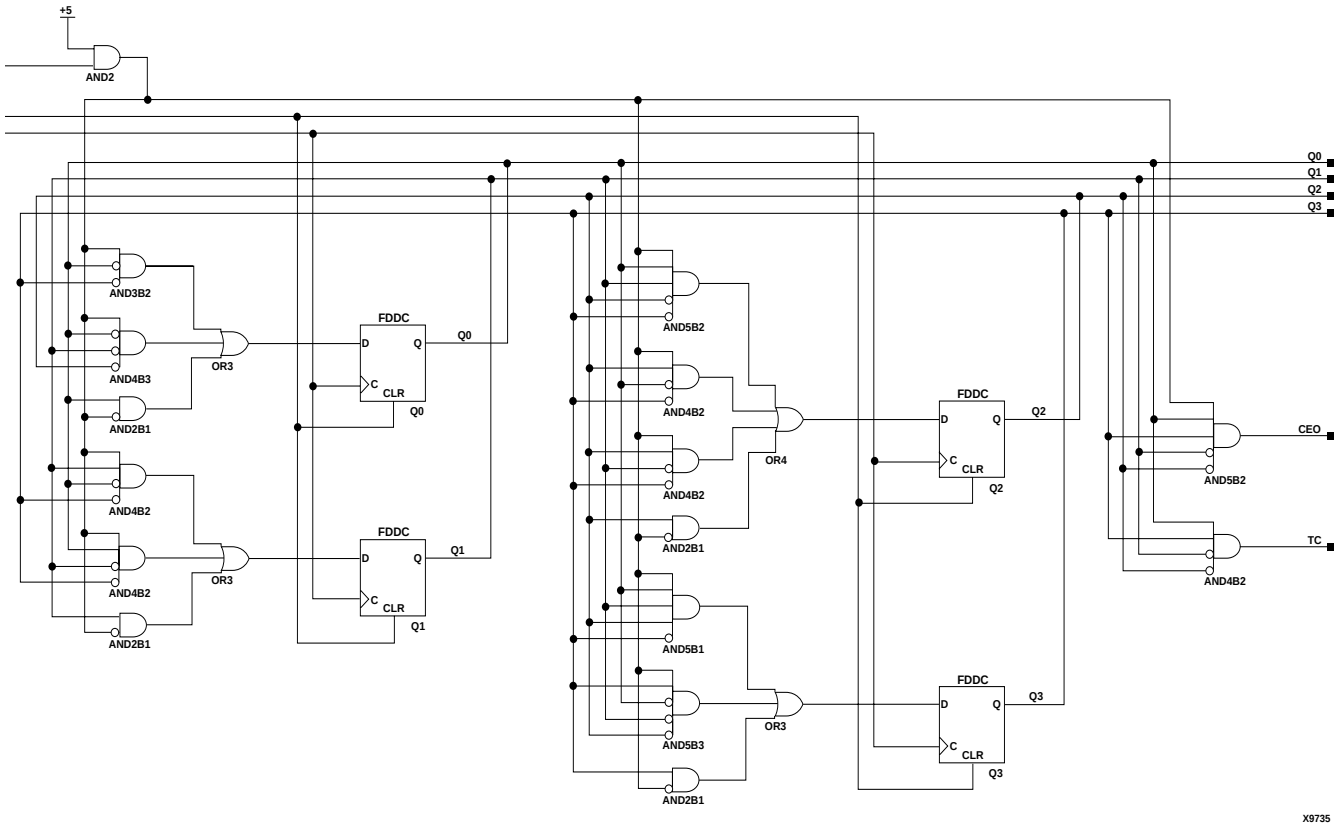
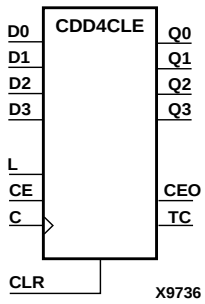


Figure 4-43 CDD4CE Implementation CoolRunner-II

CDD4CLE

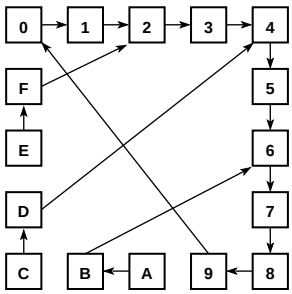
4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro



CDD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, dual edge triggered Binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transitions. The Q outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles, as shown in the following state diagram. The counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the CLR, L, and C inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs					
CLR	**L**	**CE**	**D3 – D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 – D0	↑	d3	d2	d1	d0	TC	CEO
0	1	X	D3 – D0	↓	d3	d2	d1	d0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	1	X	↓	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	0	1	X	X	1	0	0	1	1	1

d = state of referenced input one setup time prior to active clock transition

TC = Q3•!Q2•!Q1•Q0

CEO = TC•CE

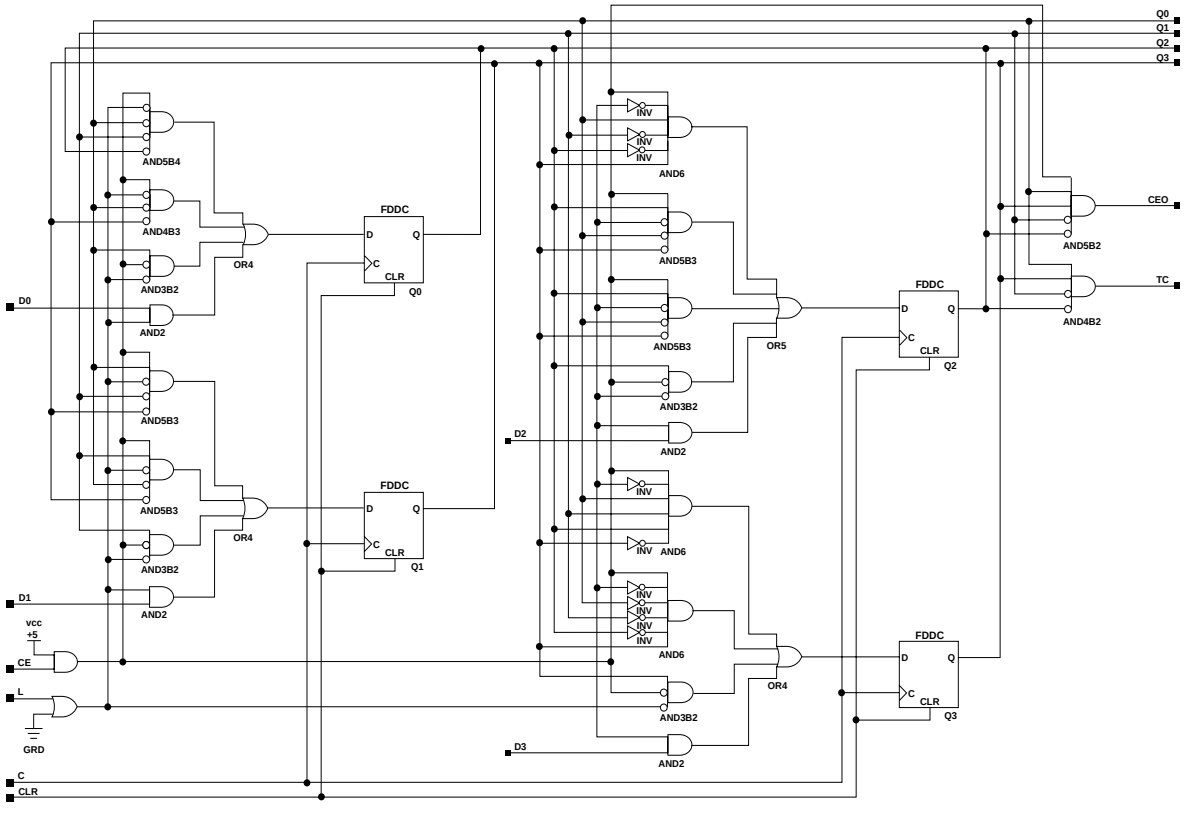
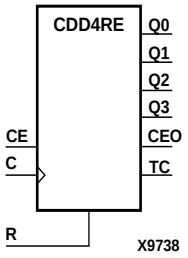


Figure 4-44 CDD4CLE Implementation CoolRunner-II

CDD4RE

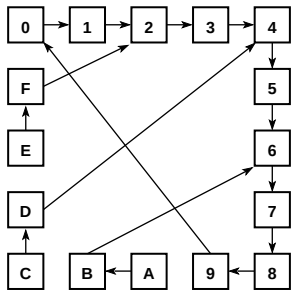
4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro



CD4RE is a 4-bit (stage), synchronous, resettable, cascadable dual edge triggered binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High or High-to-Low clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles, as shown in the following state diagram. The counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the R and clock inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs					
R	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	↑	0	0	0	0	0	0
1	X	↓	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	1	↓	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	1	X	1	0	0	1	1	1

TC = Q3•!Q2•!Q1•Q0

CEO = TC•CE

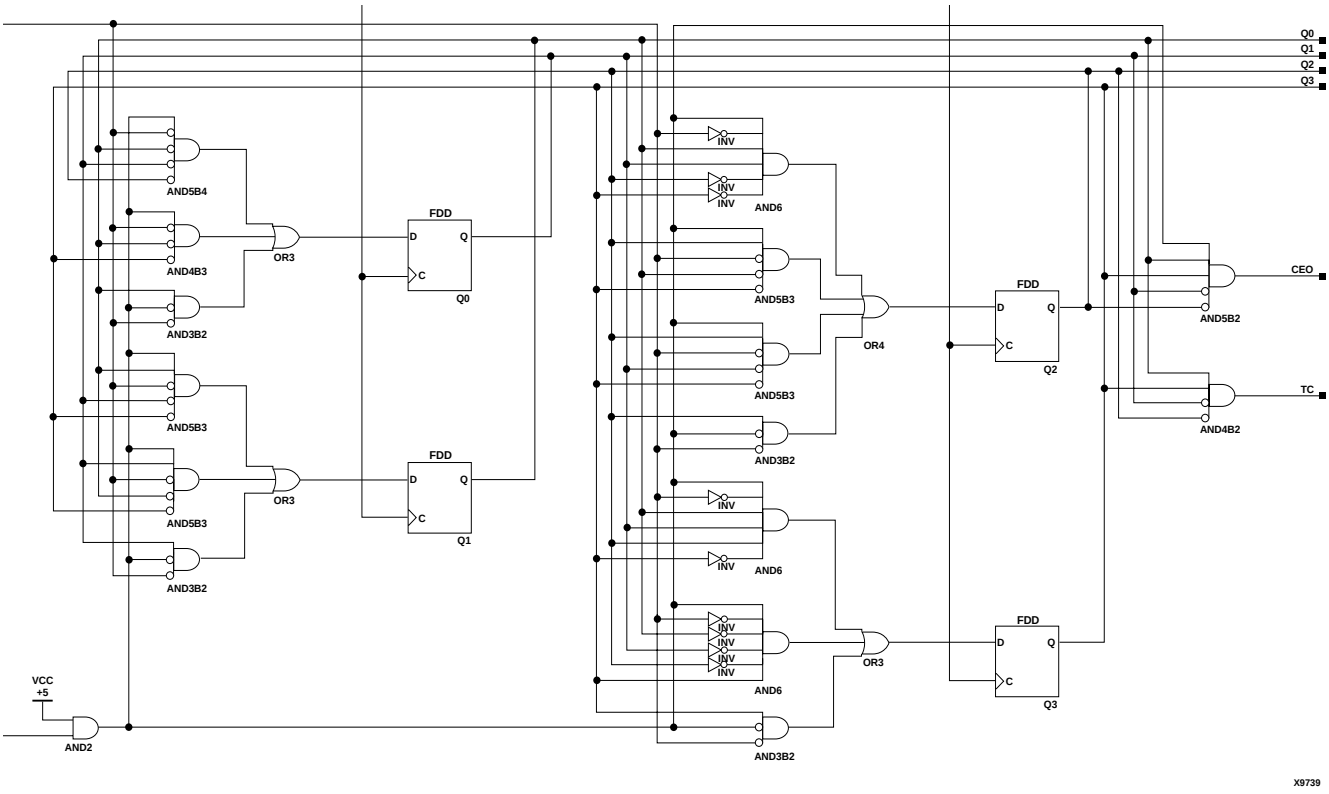
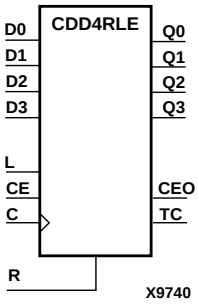


Figure 4-45 CDD4RE Implementation CoolRunner-II

CDD4RLE

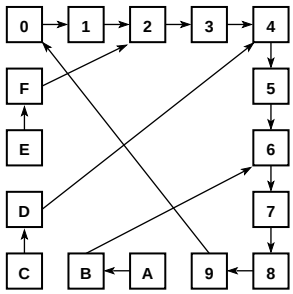
4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



CDD4RLE is a 4-bit (stage), synchronous, loadable, resettable, dual edge triggered binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High or High-to-Low clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles, as shown in the following state diagram. The counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the R, L, and C inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs					
R	**L**	**CE**	**D3 – D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	↑	0	0	0	0	0	0
1	X	X	X	↓	0	0	0	0	0	0
0	1	X	D3 – D0	↑	d3	d2	d1	d0	TC	CEO
0	1	X	D3 – D0	↓	d3	d2	d1	d0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	1	X	↓	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	0	1	X	X	1	0	0	1	1	1

d = state of referenced input one setup time prior to active clock transition

TC = Q3 • !Q2 • !Q1 • Q0

CEO = TC • CE

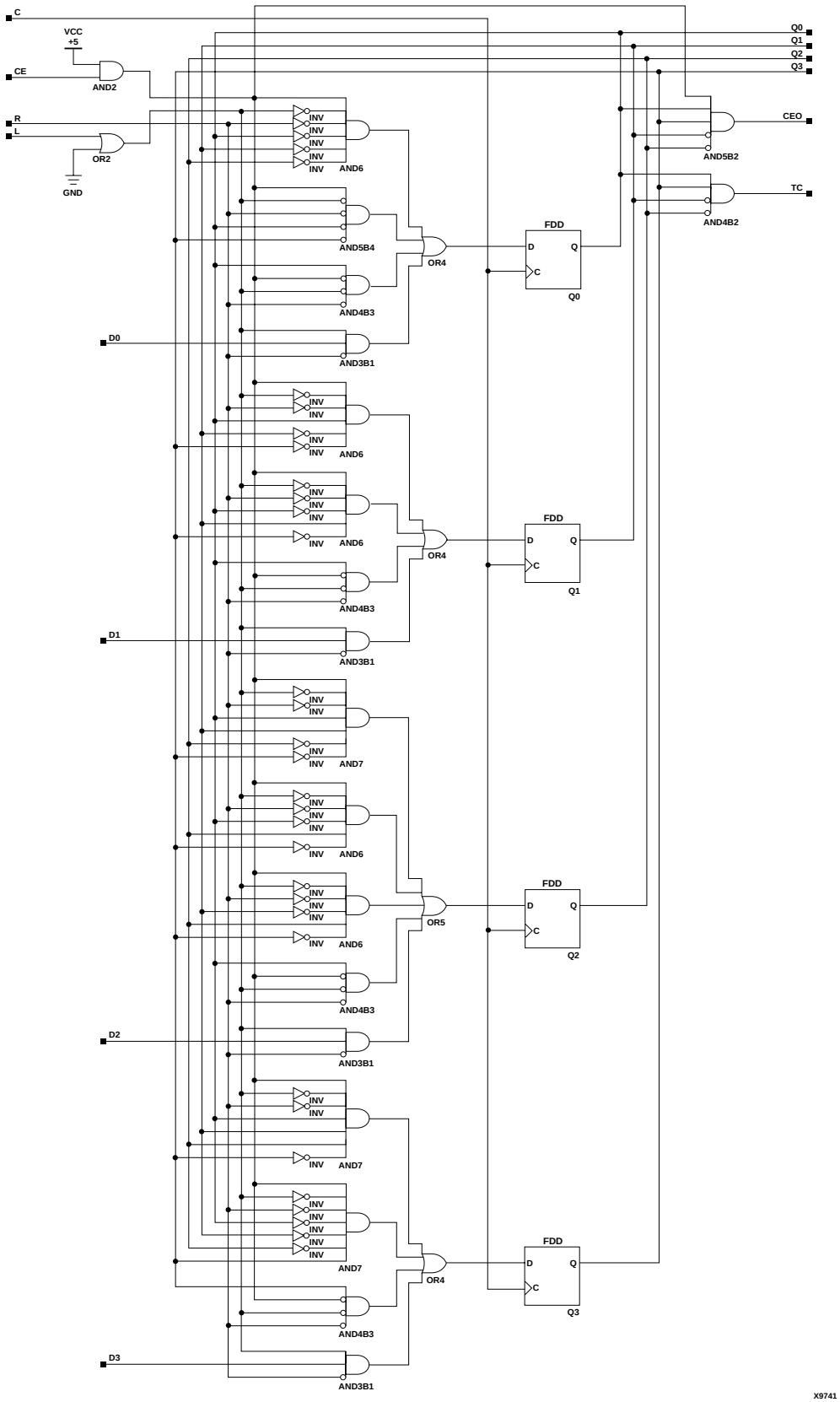
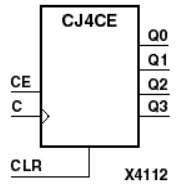


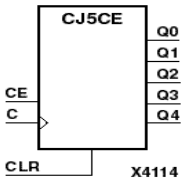
Figure 4-46 CDD4RLE Implementation CoolRunner-II

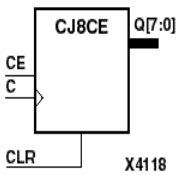
CJ4CE, CJ5CE, CJ8CE

4-, 5-, 8-Bit Johnson Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







CJ4CE, CJ5CE, and CJ8CE are clearable Johnson / shift counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

For CJ4CE, the Q3 output is inverted and fed back to input Q0 to provide continuous counting operation. For CJ5CE, the Q4 output is inverted and fed back to input Q0. For CJ8CE, the Q7 output is inverted and fed back to input Q0.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Table 4-1 CJ4CE Truth Table

Inputs			Outputs			
CLR	CE	C	Q0	Q1	Q2	Q3
1	X	X	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg
0	1	↑	!q3	q0	q1	q2

q = state of referenced output one setup time prior to active clock transition

Table 4-2 CJ5CE Truth Table

Inputs			Outputs				
CLR	CE	C	Q0	Q1	Q2	Q3	Q4
1	X	X	0	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg	No Chg
0	1	↑	!q4	q0	q1	q2	q3

q = state of referenced output one setup time prior to active clock transition

Table 4-3 CJ8CE Truth Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 – Q7**
1	X	X	0	0
0	0	X	No Chg	No Chg
0	1	↑	!q7	q0 – q6

q = state of referenced output one setup time prior to active clock transition

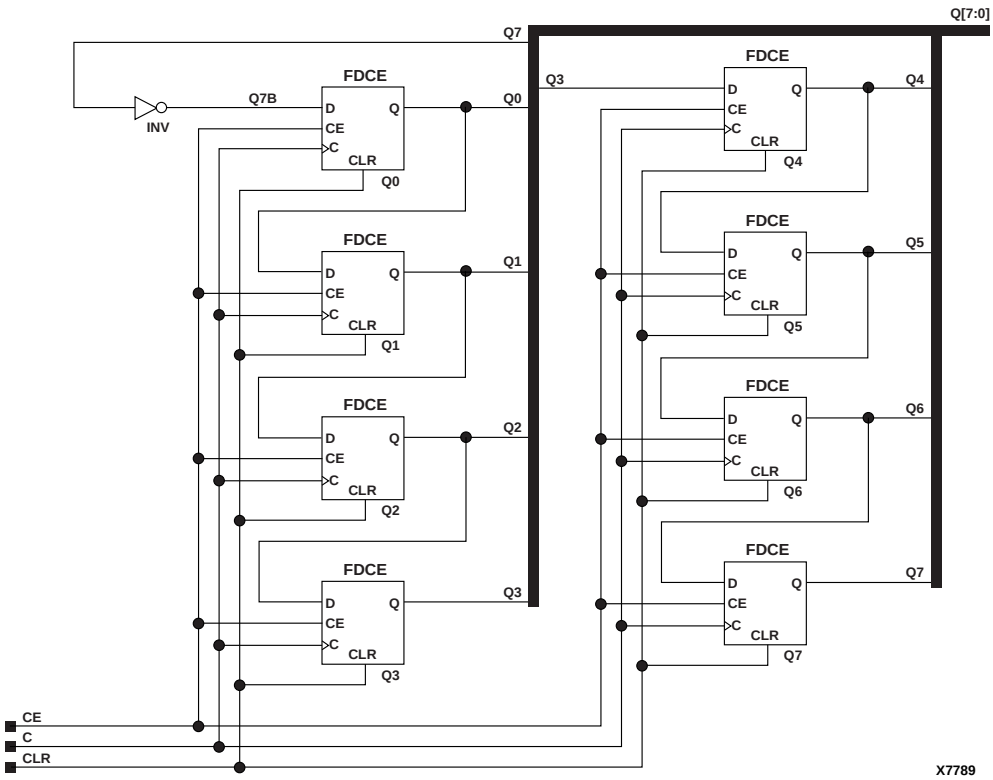
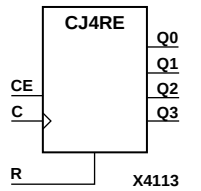


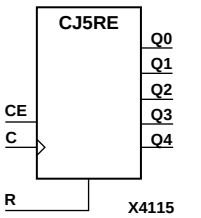
Figure 4-47 CJ8CE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

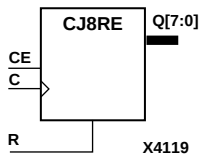
CJ4RE, CJ5RE, CJ8RE

4-, 5-, 8-Bit Johnson Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







CJ4RE, CJ5RE, and CJ8RE are resettable Johnson / shift counters. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

For CJ4RE, the Q3 output is inverted and fed back to input Q0 to provide continuous counting operation. For CJ5RE, the Q4 output is inverted and fed back to input Q0. For CJ8RE, the Q7 output is inverted and fed back to input Q0.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Table 4-4 CJ4RE Truth Table

Inputs			Outputs			
R	CE	C	Q0	Q1	Q2	Q3
1	X	↑	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg
0	1	↑	$\overline{q3}$	q0	q1	q2

q = state of referenced output one setup time prior to active clock transition

Table 4-5 CJ5RE Truth Table

Inputs			Outputs				
R	CE	C	Q0	Q1	Q2	Q3	Q4
1	X	↑	0	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg	No Chg
0	1	↑	$\overline{q4}$	q0	q1	q2	q3

q = state of referenced output one setup time prior to active clock transition

Table 4-6 CJ8RE Truth Table

Inputs			Outputs	
R	**CE**	**C**	**Q0**	**Q1 – Q7**
1	X	↑	0	0
0	0	X	No Chg	No Chg
0	1	↑	$\overline{q7}$	q0 – q6

q = state of referenced output one setup time prior to active clock transition

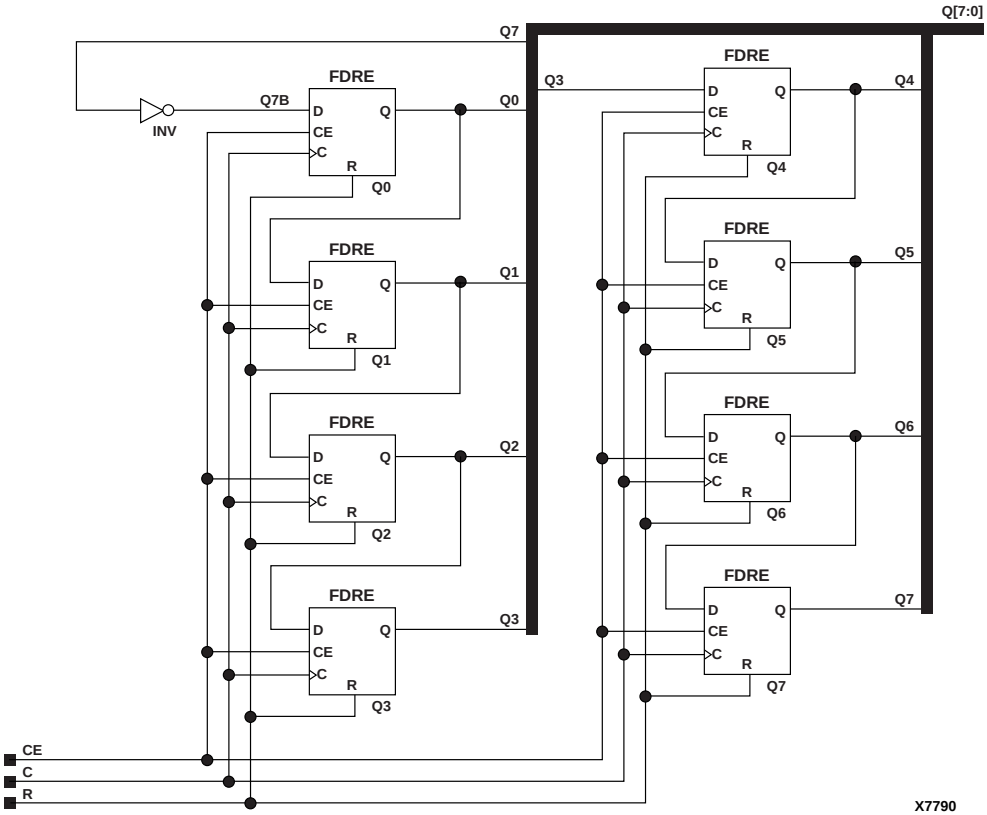
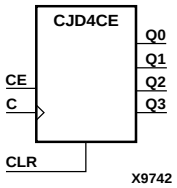


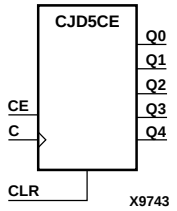
Figure 4-48 CJ8RE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

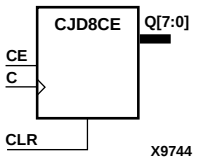
CJD4CE, CJD5CE, CJD8CE

4-, 5-, 8-Bit Dual Edge Triggered Johnson Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro







CJD4CE, CJD5CE, and CJD8CE are dual edge triggered clearable dual edge triggered Johnson/shift counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

For CJD4CE, the Q3 output is inverted and fed back to input Q0 to provide continuous counting operation. For CJD5CE, the Q4 output is inverted and fed back to input Q0. For CJD8CE, the Q7 output is inverted and fed back to input Q0.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Table 4-7 CJD4CE Truth Table

Inputs			Outputs			
CLR	CE	C	Q0	Q1	Q2	Q3
1	X	X	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg
0	1	↑	!q3	q0	q1	q2
0	1	↓	!q3	q0	q1	q2

q = state of referenced output one setup time prior to active clock transition

Table 4-8 CJD5CE Truth Table

Inputs			Outputs				
CLR	CE	C	Q0	Q1	Q2	Q3	Q4
1	X	X	0	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg	No Chg
0	1	↑	!q4	q0	q1	q2	q3
0	1	↓	!q4	q0	q1	q2	q3

q = state of referenced output one setup time prior to active clock transition

Table 4-9 CJD8CE Truth Table

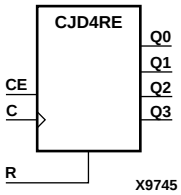
Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 – Q7**
1	X	X	0	0
0	0	X	No Chg	No Chg
0	1	↑	!q7	q0 – q6
0	1	↓	!q7	q0 – q6

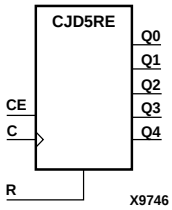
q = state of referenced output one setup time prior to active clock transition

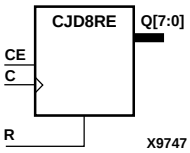
CJD4RE, CJD5RE, CJD8RE

4-, 5-, 8-Bit Dual Edge Triggered Johnson Counters with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro







CJD4RE, CJD5RE, and CJD8RE are resettable dual edge triggered Johnson/shift counters. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High and High-to-Low clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

For CJD4RE, the Q3 output is inverted and fed back to input Q0 to provide continuous counting operation. For CJD5RE, the Q4 output is inverted and fed back to input Q0. For CJD8RE, the Q7 output is inverted and fed back to input Q0.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Table 4-10 CJD4RE Truth Table

Inputs			Outputs			
R	CE	C	Q0	Q1	Q2	Q3
1	X	↑	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg
0	1	↑	$\overline{q3}$	q0	q1	q2
0	1	↓	$\overline{q3}$	q0	q1	q2

q = state of referenced output one setup time prior to active clock transition

Table 4-11 CJD5RE Truth Table

Inputs			Outputs				
R	CE	C	Q0	Q1	Q2	Q3	Q4
1	X	↑	0	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg	No Chg
0	1	↑	$\overline{q4}$	q0	q1	q2	q3
0	1	↓	$\overline{q4}$	q0	q1	q2	q3

q = state of referenced output one setup time prior to active clock transition

Table 4-12 CJD8RE Truth Table

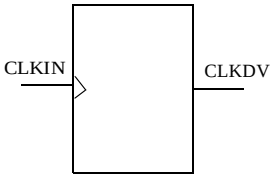
Inputs			Outputs	
R	**CE**	**C**	**Q0**	**Q1 – Q7**
1	X	↑	0	0
1	X	↓	0	0
0	0	X	No Chg	No Chg
0	1	↑	$\overline{q7}$	q0 – q6
0	1	↓	$\overline{q7}$	q0 – q6

q = state of referenced output one setup time prior to active clock transition

CLK_DIV2,4,6,8,10,12,14,16

Global Clock Divider

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Primitive



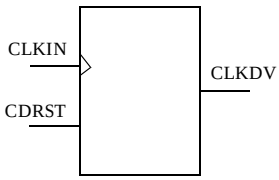
The CLK_DIV2,4,6,8,10,12,14,16 Global Clock Dividers divide a user-provided external clock signal gclk<2> by 2, 4, 6, 8, 10, 12, 14, and 16, respectively. Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 orXC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50.

The CLKDV output is reset low by power-on reset circuitry.

CLK_DIV2,4,6,8,10,12,14,16R

Global Clock Divider with Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Primitive



The CLK_DIV2,4,6,8,10,12,14,16R Global Clock Dividers with Synchronous Reset divide a user-provided external clock signal gclk<2> by 2, 4, 6, 8, 10, 12, 14, and 16, respectively. Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50.

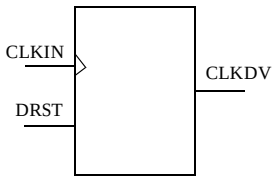
The CDRST input is an active HIGH synchronous reset. If CDRST is input HIGH when the CLKDV output is HIGH, the CLKDV output remains HIGH to complete the last clock pulse, and then goes LOW.

The CLKDV output is reset low by power-on reset circuitry.

CLK_DIV2,4,6,8,10,12,14,16RSD

Global Clock Divider with Synchronous Reset and Start Delay

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Primitive



The CLK_DIV2,4,6,8,10,12,14,16 Global Clock Dividers with Synchronous Reset and Start Delay divide a user-provided external clock signal gclk<2> by 2, 4, 6, 8, 10, 12, 14, and 16, respectively. Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50.

The CDRST input is an active HIGH synchronous reset. If CDRST is input HIGH when the CLKDV output is HIGH, the CLKDV output remains HIGH to complete the last clock pulse, and then goes LOW.

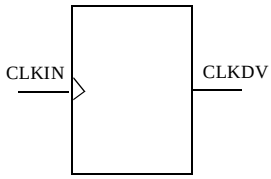
The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

CLK_DIV2,4,6,8,10,12,14,16SD

Global Clock Divider with Start Delay

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Primitive



The CLK_DIV2,4,6,8,10,12,14,16SD Global Clock Dividers with Start Delay divide a user-provided external clock signal gclk<2> by 2, 4, 6, 8, 10, 12, 14, and 16, respectively. Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50.

The start delay function delays the CLKDV output (n + 1) clocks, where n is the divisor for the clock divider.

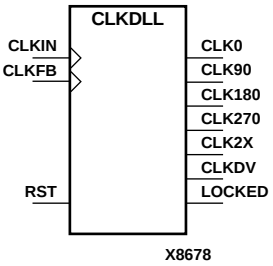
The CLKDV output is reset low by power-on reset circuitry.

CLKDLL

Clock Delay Locked Loop

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner
Primitive	Primitive*	N/A	N/A	N/A	N/A

*Use CLKDLLE for Virtex-E



CLKDLL is a clock delay locked loop used to minimize clock skew. CLKDLL synchronizes the clock signal at the feed back clock input (CLKFB) to the clock signal at the input clock (CLKIN). The locked output (LOCKED) is high when the two signals are in phase. The signals are considered to be in phase when their rising edges are within a specific range of each other (see *The Programmable Logic Data Book* for the most current value).-

The frequency of the clock signal at the CLKIN input must be in a specific range depending on speed grade (see *The Programmable Logic Data Book* for the most current values). The CLKIN pin must be driven by an IBUFG or a BUFG.

On-chip synchronization is achieved by connecting the CLKFB input to a point on the global clock network driven by a BUFG, a global clock buffer. The BUFG connected to the CLKFB input of the CLKDLL must be sourced from either the CLK0 or CLK2X outputs of the same CLKDLL. The CLKIN input should be connected to the output of an IBUFG, with the IBUFG input connected to a pad driven by the system clock.

Off-chip synchronization is achieved by connecting the CLKFB input to the output of an IBUFG, with the IBUFG input connected to a pad. Either the CLK0 or CLK2X output can be used but not both. The CLK0 or CLK2X must be connected to the input of OBUF, an output buffer.

The duty cycle of the CLK0 output is 50-50 unless the DUTY_CYCLE_CORRECTION attribute is set to FALSE, in which case the duty cycle is the same as that of the CLKIN input. The duty cycle of the phase shifted outputs (CLK90, CLK180, and CLK270) is the same as that of the CLK0 output. The duty cycle of the CLK2X and CLKDV outputs is always 50-50. The frequency of the CLKDV output is determined by the value assigned to the CLKDV_DIVIDE attribute.

The master reset input (RST) resets CLKDLL to its initial (power-on) state. The signal at the RST input is asynchronous and must be held High for just 2ns.

Table 4-13 CLKDLL Outputs

Output	Description
CLK0	Clock at 1x CLKIN frequency
CLK90	Clock at 1x CLKIN frequency, shifted 90^{o} with regards to CLK0
CLK180	Clock at 1x CLKIN frequency, shifted 180^{o} with regards to CLK0
CLK270	Clock at 1x CLKIN frequency, shifted 270^{o} with regards to CLK0
CLK2X	Clock at 2x CLKIN frequency

Table 4-13 CLKDLL Outputs

Output	Description
CLKDV	Clock at (1/n)x CLKIN frequency, n=CLKDV_DIVIDE value
LOCKED	CLKDLL locked

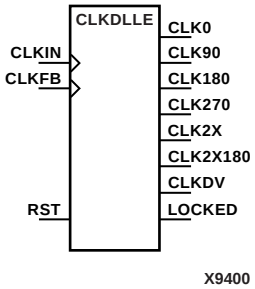
Note See the "PERIOD Specifications on CLKDLLs" section of the "Using Timing Constraints" chapter in the Development System Reference Guide for additional information on using the TNM, TNM_NET, and PERIOD attributes with CLKDLL components.

CLKDLLE

Virtex-E Clock Delay Locked Loop

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner
N/A	Primitive*	N/A	N/A	N/A	N/A

* Supported for Virtex-E devices only



CLKDLLE is a clock delay locked loop used to minimize clock skew for Virtex-E devices. CLKDLLE synchronizes the clock signal at the feed back clock input (CLKFB) to the clock signal at the input clock (CLKIN). The locked output (LOCKED) is high when the two signals are in phase. The signals are considered to be in phase when their rising edges are within a specific rangeof each other (see *The Programmable Logic Data Book* for the most current value).

The frequency of the clock signal at the CLKIN input must be in a specific range depending on speed grade (see *The Programmable Logic Data Book* for the most current values). The CLKIN pin must be driven by an IBUFG or a BUFG.

On-chip synchronization is achieved by connecting the CLKFB input to a point on the global clock network driven by a BUFG, a global clock buffer. The BUFG input can only be connected to the CLK0 or CLK2X output of CLKDLLE. The BUFG connected to the CLKFB input of the CLKDLLE must be sourced from either the CLK0 or CLK2X outputs of the same CLKDLLE. The CLKIN input should be connected to the output of an IBUFG, with the IBUFG input connected to a pad driven by the system clock.

Off-chip synchronization is achieved by connecting the CLKFB input to the output of an IBUFG, with the IBUFG input connected to a pad. Either the CLK0 or CLK2X output can be used but not both. The CLK0 or CLK2X must be connected to the input of OBUF, an output buffer.

The duty cycle of the CLK0 output is 50-50 unless the DUTY_CYCLE_CORRECTION attribute is set to FALSE, in which case the duty cycle is the same as that of the CLKIN input. The duty cycle of the phase shifted outputs (CLK90, CLK180, and CLK270) is the same as that of the CLK0 output. The duty cycle of the CLK2X, CLK2X180, and CLKDV outputs is always 50-50. The frequency of the CLKDV output is determined by the value assigned to the CLKDV_DIVIDE attribute.

The master reset input (RST) resets CLKDLLE to its initial (power-on) state. The signal at the RST input is asynchronous and must be held High for just 2ns.

Table 4-14 CLKDLLE Outputs

Output	Description
CLK0	Clock at 1x CLKIN frequency
CLK90	Clock at 1x CLK0 frequency, shifted 90^o with regards to CLK0
CLK180	Clock at 1x CLK0 frequency, shifted 180^o with regards to CLK0
CLK270	Clock at 1x CLK0 frequency, shifted 270^o with regards to CLK0
CLK2X	Clock at 2x CLK0 frequency, in phase with CLK0
CLK2X180	Clock at 1x CLK2X frequency shifted 180^o with regards to CLK2X

Table 4-14 CLKDLLE Outputs

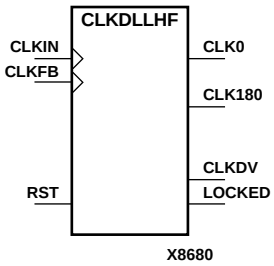
Output	Description
CLKDV	Clock at (1 / n) x CLK0 frequency, where n=CLKDV_DIVIDE value
LOCKED	CLKDLLE locked. CLKIN and CLKFB synchronized.

CLKDLLHF

High Frequency Clock Delay Locked Loop

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner
Primitive	Primitive*	N/A	N/A	N/A	N/A

*Use CLKDLLHF for the Virtex-E DLL in HF mode. In LF mode, both the separate CLKDLLE and CLKDLL primitive can be used.



CLKDLLHF is a high frequency clock delay locked loop used to minimize clock skew. CLKDLLHF synchronizes the clock signal at the feed back clock input (CLKFB) to the clock signal at the input clock (CLKIN). The locked output (LOCKED) is high when the two signals are in phase. The signals are considered to be in phase when their rising edges are within a specific range of each other (see *The Programmable Logic Data Book* for the most current value).

The frequency of the clock signal at the CLKIN input must be in a specific range depending on speed grade (see *The Programmable Logic Data Book* for the most current values). The CLKIN pin must be driven by an IBUFG or a BUFG.

On-chip synchronization is achieved by connecting the CLKFB input to a point on the global clock network driven by a BUFG, a global clock buffer. The BUFG input can only be connected to the CLK0 output of CLKDLLHF. The BUFG connected to the CLKFB input of the CLKDLLHF must be sourced from the CLK0 output of the same CLKDLLHF. The CLKIN input should be connected to the output of an IBUFG, with the IBUFG input connected to a pad driven by the system clock.

Off-chip synchronization is achieved by connecting the CLKFB input to the output of an IBUFG, with the IBUFG input connected to a pad. Only the CLK0 output can be used. CLK0 must be connected to the input of OBUF, an output buffer.

The duty cycle of the CLK0 output is 50-50 unless the DUTY_CYCLE_CORRECTION attribute is set to FALSE, in which case the duty cycle is the same as that of the CLKIN input. The duty cycle of the phase shifted output (CLK180) is the same as that of the CLK0 output. The frequency of the CLKDV output is determined by the value assigned to the CLKDV_DIVIDE attribute.

The master reset input (RST) resets CLKDLLHF to its initial (power-on) state. The signal at the RST input is asynchronous and must be held High for just 2ns.

Table 4-15 CLKDLLHF Outputs

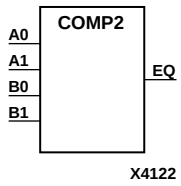
Output	Description
CLK0	Clock at 1x CLKIN frequency
CLK180	Clock at 1x CLKIN frequency, shifted 180^{o} with regards to CLK0
CLKDV	Clock at (1/n)x CLKIN frequency, n=CLKDV_DIVIDE value
LOCKED	CLKDLL locked

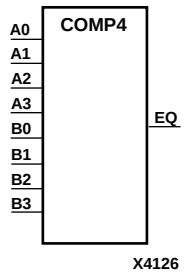
Note See the "PERIOD Specifications on CLKDLLs" section of the "Using Timing Constraints" chapter in the *Development System Reference Guide* for additional information on using the TNM, TNM_NET, and PERIOD attributes with CLKDLLHF components.

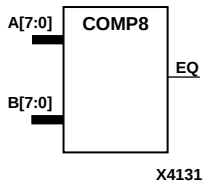
COMP2, 4, 8, 16

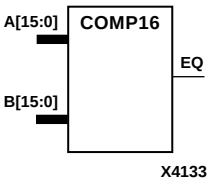
2-, 4-, 8-, 16-Bit Identity Comparators

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro









COMP2, COMP4, COMP8, and COMP16 are, respectively, 2-, 4-, 8-, and 16-bit identity comparators. The equal output (EQ) of the COMP2 2-bit, identity comparator is High when the two words A1 – A0 and B1 – B0 are equal. EQ is high for COMP4 when A3 – A0 and B3 – B0 are equal; for COMP8, when A7 – A0 and B7 – B0 are equal; and for COMP16, when A15 – A0 and B15 – B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

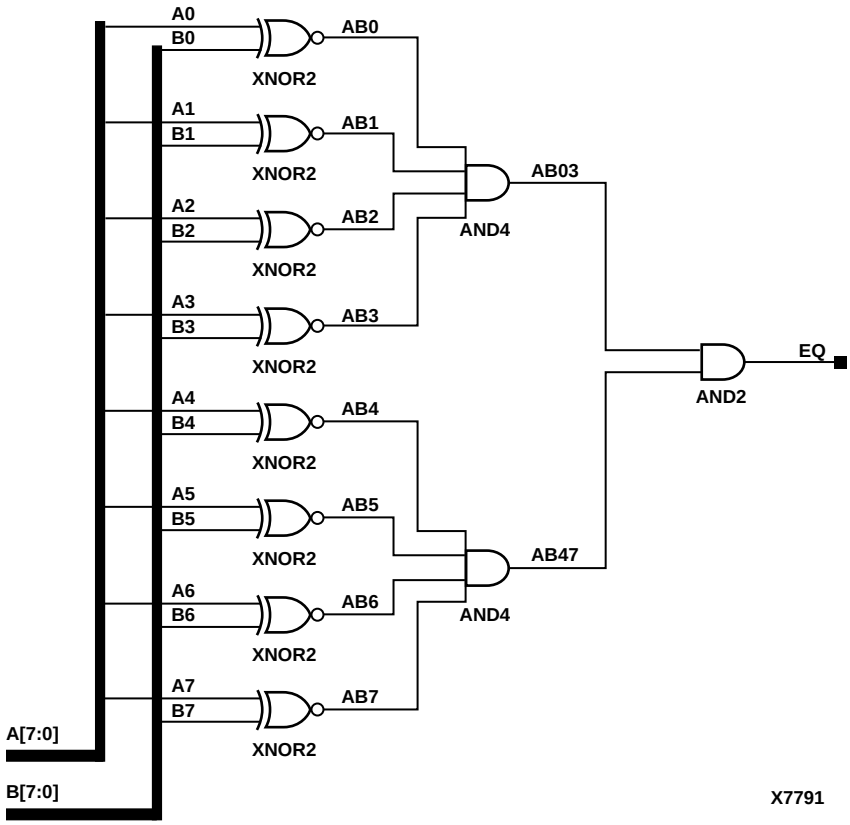
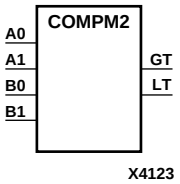


Figure 4-49 COMP8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

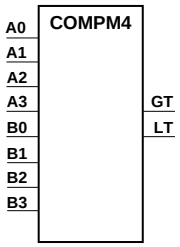
COMPM2, 4, 8, 16

2-, 4-, 8-, 16-Bit Magnitude Comparators

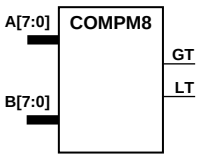
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



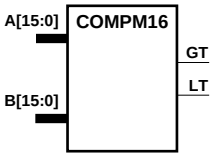
X4123



X4127



X4132



X4134

COMPM2, COMPM4, COMPM8, and COMPM16 are, respectively, 2-, 4-, 8-, and 16-bit magnitude comparators that compare two positive binary-weighted words.

COMPM2 compares A1 – A0 and B1 – B0, where A1 and B1 are the most significant bits. COMPM4 compares A3 – A0 and B3 – B0, where A3 and B3 are the most significant bits. COMPM8 compares A7 – A0 and B7 – B0, where A7 and B7 are the most significant bits. COMPM16 compares A15 – A0 and B15 – B0, where A15 and B15 are the most significant bits.

The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Table 4-16 COMPM2 Truth Table

Inputs				Outputs	
A1	B1	A0	B0	GT	LT
0	0	0	0	0	0
0	0	1	0	1	0
0	0	0	1	0	1
0	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	0
1	1	0	1	0	1
1	1	1	1	0	0
1	0	X	X	1	0
0	1	X	X	0	1

Table 4-17 COMPM4 Truth Table

Inputs				Outputs	
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A3>B3	X	X	X	1	0
A3<B3	X	X	X	0	1
A3=B3	A2>B2	X	X	1	0
A3=B3	A2<B2	X	X	0	1
A3=B3	A2=B2	A1>B1	X	1	0
A3=B3	A2=B2	A1<B1	X	0	1
A3=B3	A2=A2	A1=B1	A0>B0	1	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0

Table 4-18 COMPM8 Truth Table (also representative of COMPM16)

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

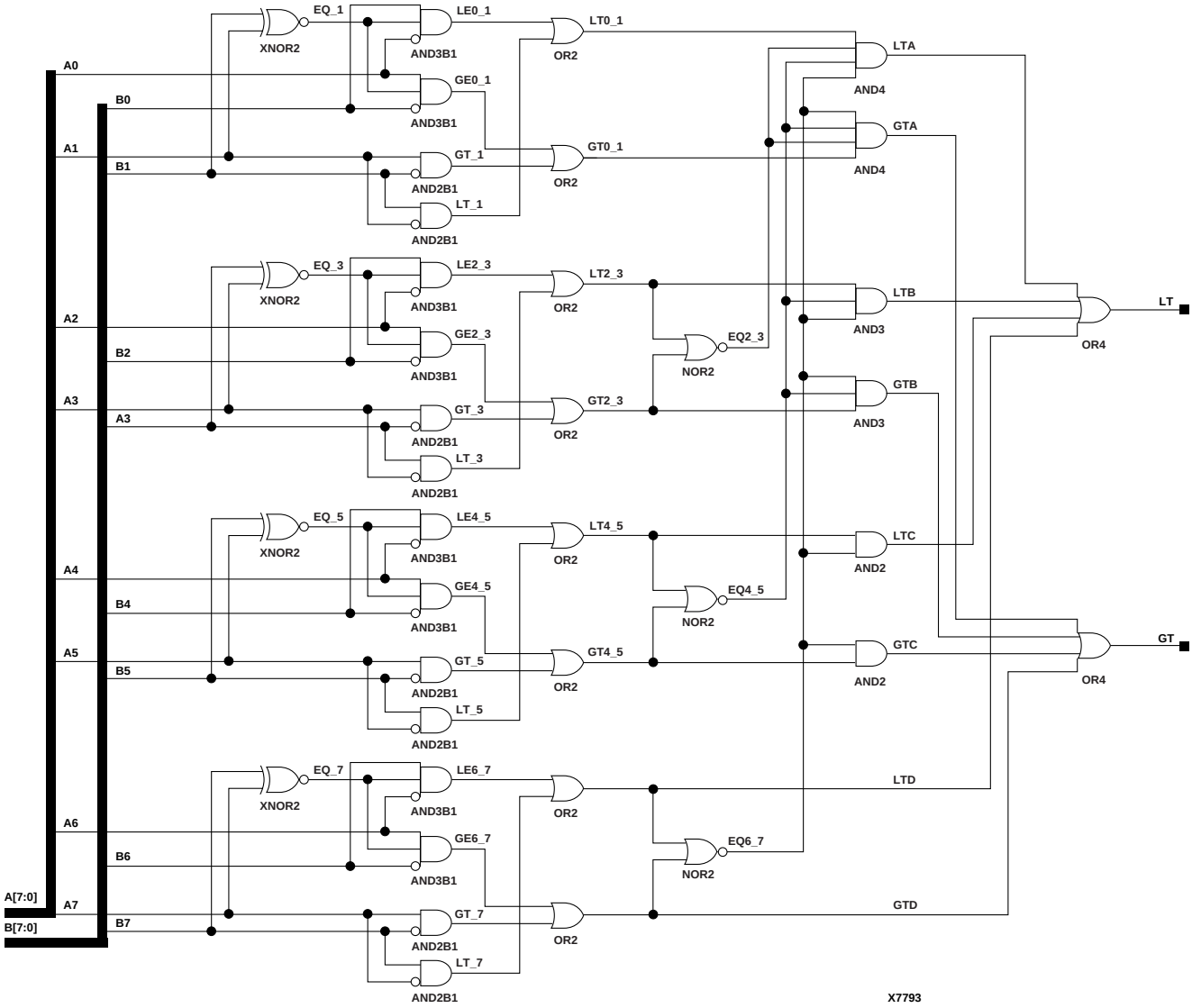


Figure 4-50 COMPM8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

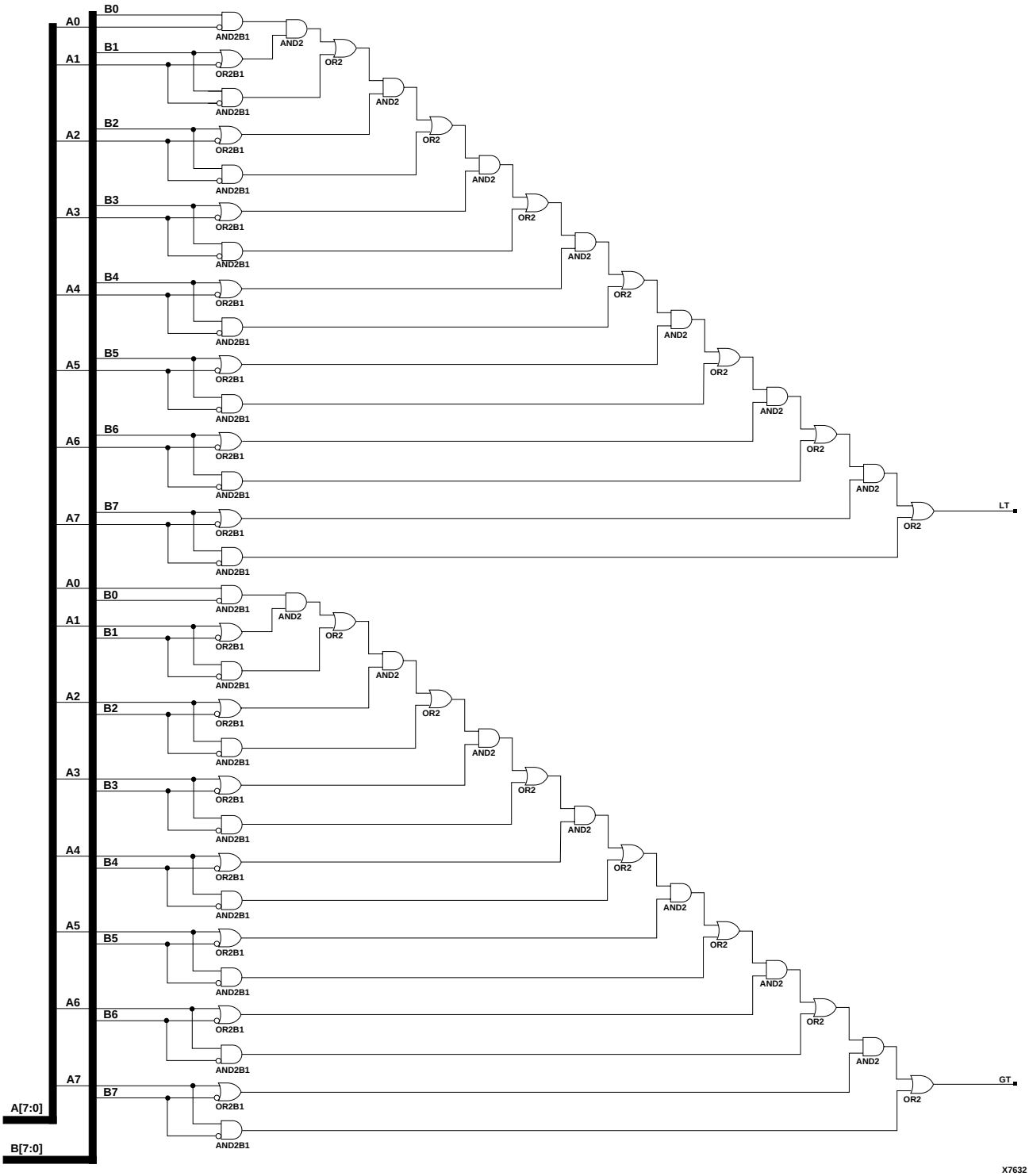
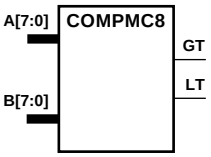


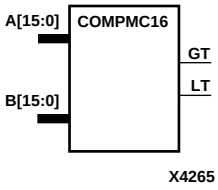
Figure 4-51 COMPM8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

COMPMC8, 16

8-, 16-Bit Magnitude Comparators

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N / A	N / A	N / A





COMPMC8 is an 8-bit, magnitude comparator that compares two positive binary-weighted words A7 – A0 and B7 – B0, where A7 and B7 are the most significant bits. COMPMC16 is a 16-bit, magnitude comparator that compares two positive binary-weighted words A15 – A0 and B15 – B0, where A15 and B15 are the most significant bits.

These comparators are implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Table 4-19 COMPMC8 Truth Table (also representative of COMPMC16)

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

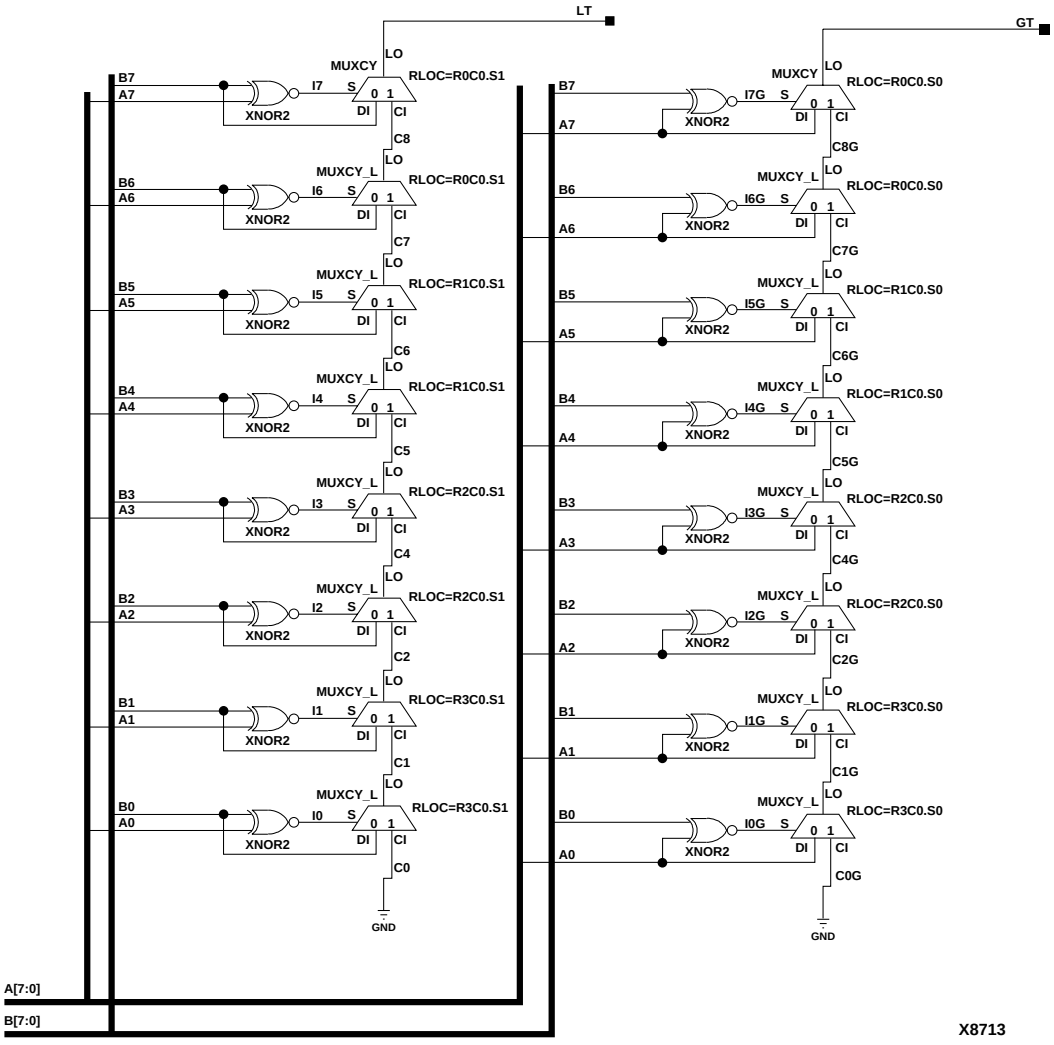


Figure 4-52 COMPMC8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

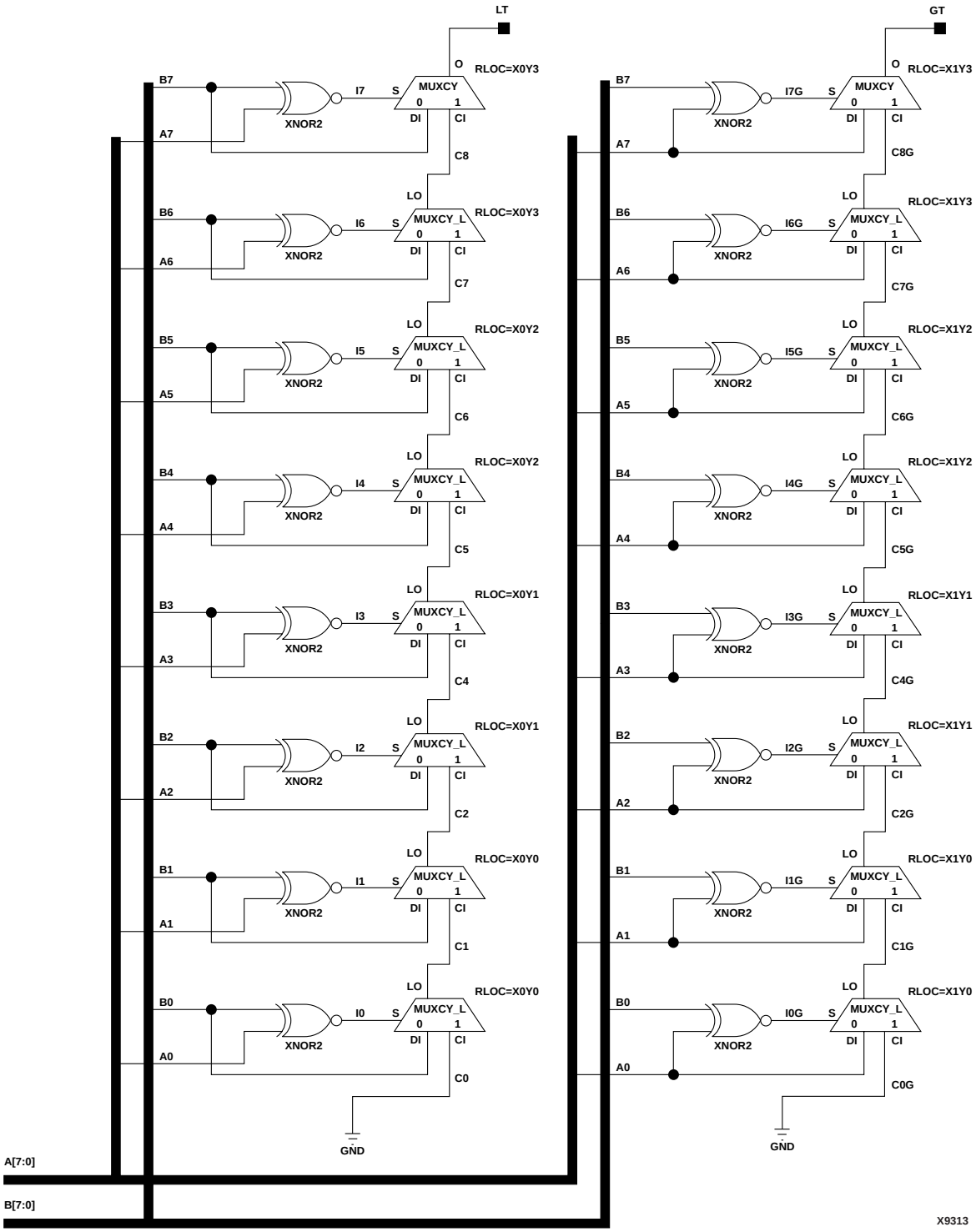
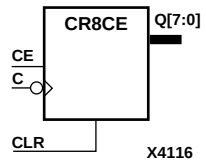


Figure 4-53 COMPMC8 Implementation Virtex-II, Virtex-II PRO

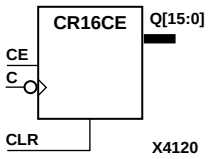
CR8CE, CR16CE

8-, 16-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



X4116



X4120

CR8CE and CR16CE are 8-bit and 16-bit, cascadable, clearable, binary, ripple counters. The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output (Q7 for CR8CE, Q15 for CR16CE) of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is $n(t_{C-Q})$, where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

The counter is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CLR	CE	C	Qz – Q0
1	X	X	0
0	0	X	No Chg
0	1	↓	Inc

z = 7 for CR8CE; z = 15 for CR16CE.

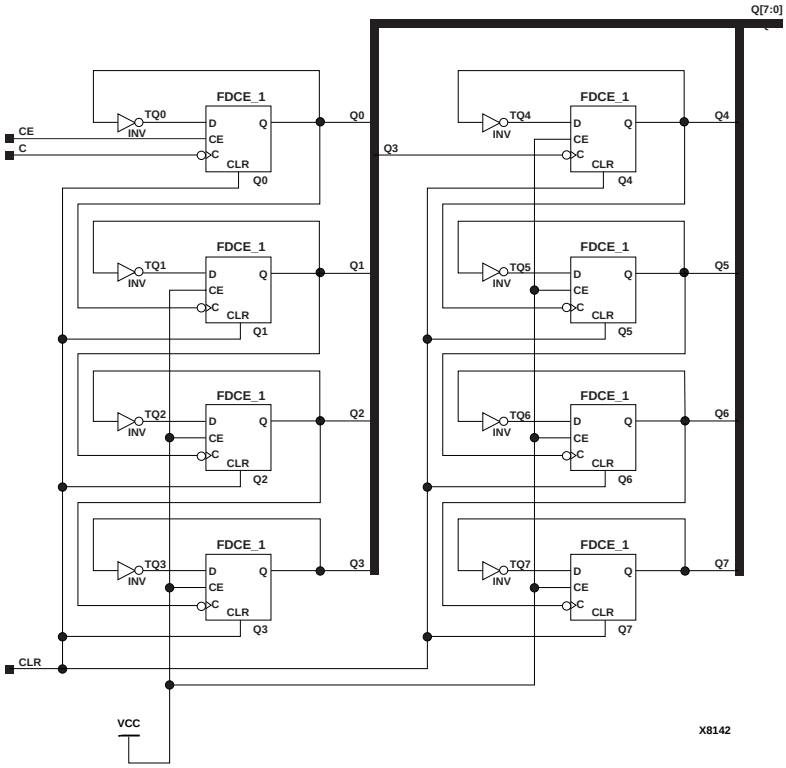


Figure 4-54 CR8CE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

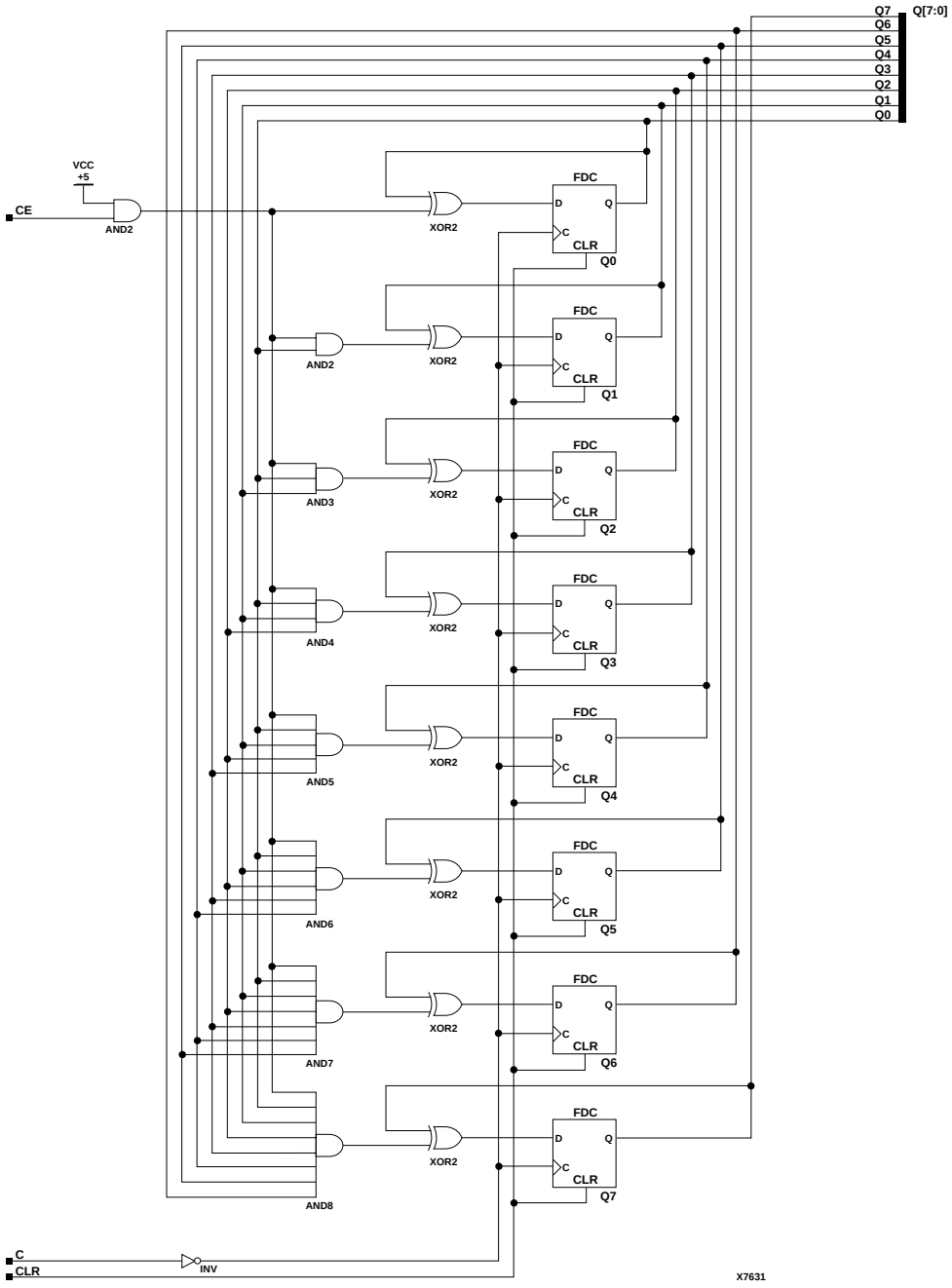
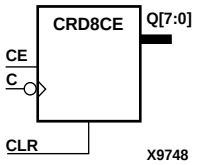


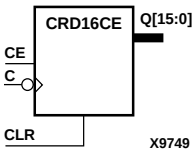
Figure 4-55 CR8CE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

CRD8CE, CRD16CE

8-, 16-Bit Dual-Edge Triggered Binary Ripple Counters with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro





CRD8CE and CRD16CE are dual edge triggered 8-bit and 16-bit, cascadable, clearable, binary, ripple counters. The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low and Low-to-High clock (C) transitions. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output (Q7 for CRD8CE, Q15 for CRD16CE) of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is $n(t_{C-Q})$, where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

The counter is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs
CLR	CE	C	Qz – Q0
1	X	X	0
0	0	X	No Chg
0	1	↑	Inc
0	1	↓	Inc

z = 7 for CR8CE; z = 15 for CR16CE.

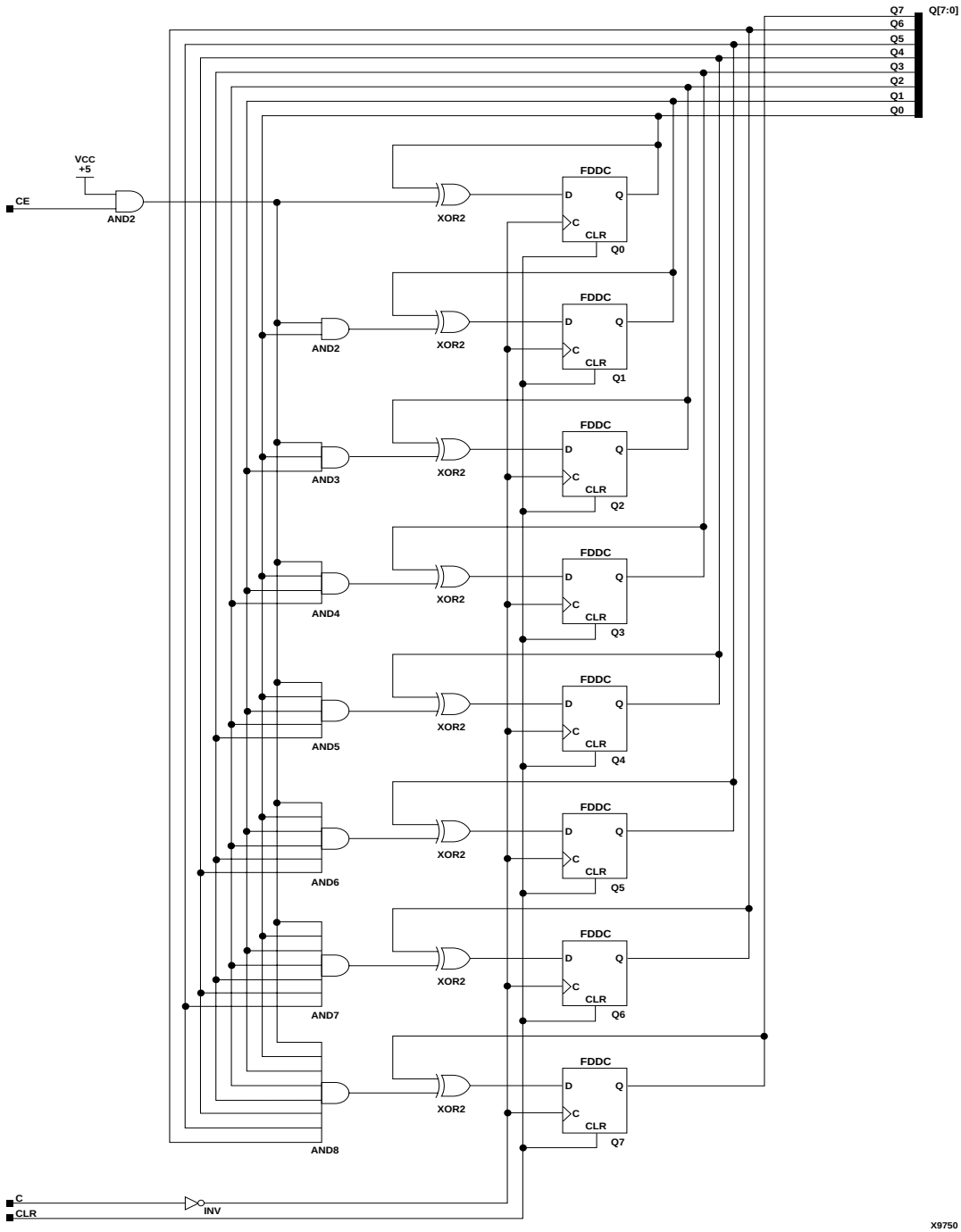
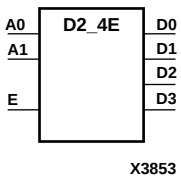


Figure 4-56 CRD8CE Implementation CoolRunner-II

D2_4E

2- to 4-Line Decoder/Demultiplexer with Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



When the enable (EN) input of the D2_4E decoder / demultiplexer is High, one of four active-High outputs (D3 – D0) is selected with a 2-bit binary address (A1 – A0) input. The non-selected outputs are Low. Also, when the EN input is Low, all outputs are Low. In demultiplexer applications, the EN input is the data input.

Inputs			Outputs			
A1	A0	E	D3	D2	D1	D0
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

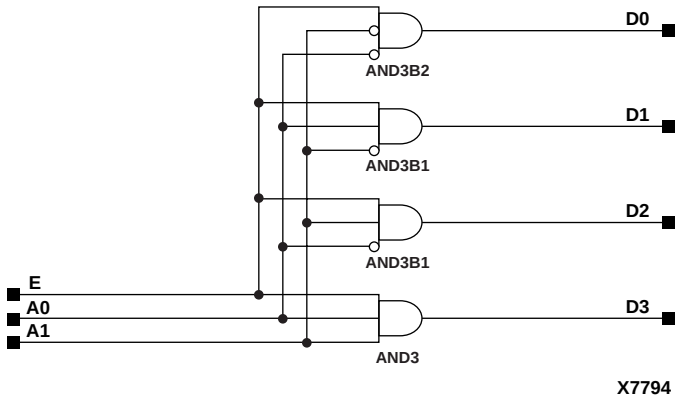
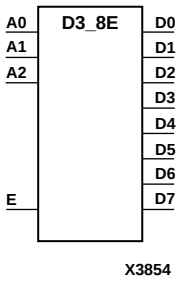


Figure 4-57 D2_4E Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

D3_8E

3- to 8-Line Decoder/Demultiplexer with Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



When the enable (EN) input of the D3_8E decoder / demultiplexer is High, one of eight active-High outputs (D7 – D0) is selected with a 3-bit binary address (A2 – A0) input. The non-selected outputs are Low. Also, when the EN input is Low, all outputs are Low. In demultiplexer applications, the EN input is the data input.

Inputs				Outputs							
A2	A1	A0	E	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

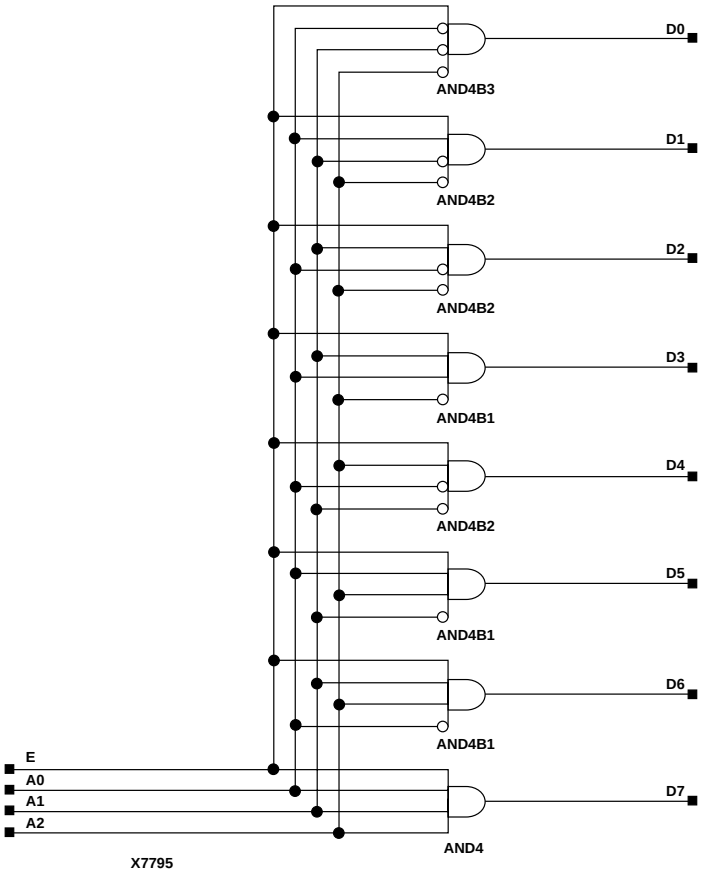
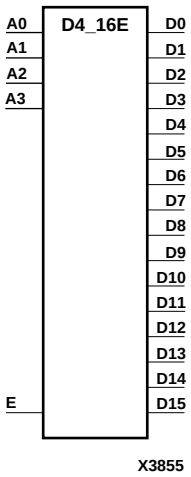


Figure 4-58 D3_8E Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

D4_16E

4- to 16-Line Decoder/Demultiplexer with Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, V irtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



When the enable (EN) input of the D4_16E decoder / demultiplexer is High, one of 16 active-High outputs (D15 – D0) is selected with a 4-bit binary address (A3 – A0) input. The non-selected outputs are Low. Also, when the EN input is Low, all outputs are Low. In demultiplexer applications, the EN input is the data input.

See the "D3_8E" section for a representative truth table derivation.

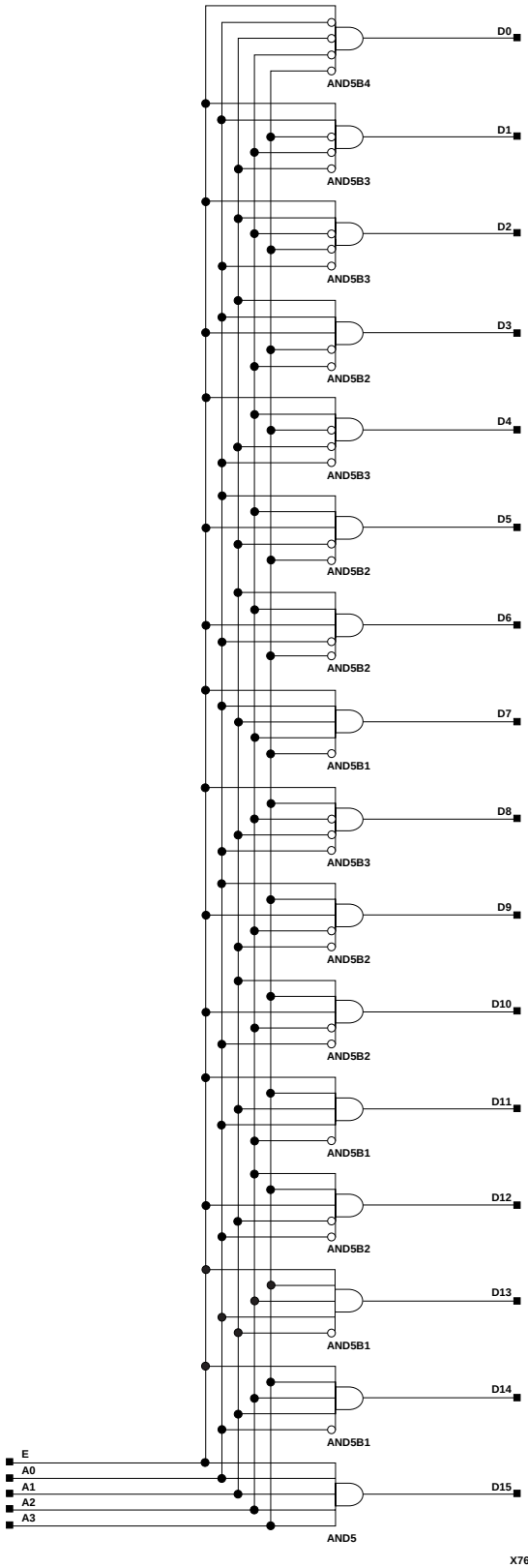
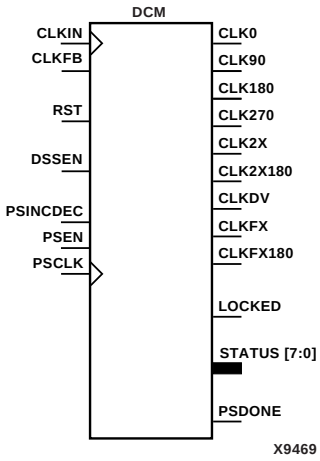


Figure 4-59 D4_16E Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

DCM

Digital Clock Manager

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



DCM is a digital clock manager that provides multiple functions. It can implement a clock delay locked loop, a digital frequency synthesizer, digital phase shifter and a digital spread spectrum.

Note All unused inputs must be driven Low. The program will automatically tie the inputs Low if they are unused.

Clock Delay Locked Loop (DLL)

DCM includes a clock delay locked loop used to minimize clock skew for Virtex-II and Virtex-II PRO devices. DCM synchronizes the clock signal at the feed back clock input (CLKFB) to the clock signal at the input clock (CLKIN). The locked output (LOCKED) is high when the two signals are in phase. The signals are considered to be in phase when their rising edges are within a specified time (ps) of each other. See *The Programmable Logic Data Book* for the specified time value.

DCM supports two frequency modes for the DLL. By default, the DLL_FREQUENCY_MODE attribute is set to LOW and the frequency of the clock signal at the CLKIN input must be in the LOW (DLL_CLKIN_MIN_LF to DLL_CLKIN_MAX_LF) frequency range (MHz). See the *The Programmable Logic Data Book* for the current DLL_CLKIN_MIN_LF to DLL_CLKIN_MAX_LF frequency range values. In LOW frequency mode, the CLK0, CLK90, CLK180, CLK270, CLK2X, CLKDV, and CLK2X180 outputs are available. When the DLL_FREQUENCY_MODE attribute is set to HIGH, the frequency of the clock signal at the CLKIN input must be in the HIGH (DLL_CLKIN_MIN_HF to DLL_CLKIN_MAX_HF)frequency range (MHz). See the *The Programmable Logic Data Book* for the current DLL_CLKIN_MIN_HF to DLL_CLKIN_MAX_HF frequency range values. In HIGH frequency mode, only the CLK0, CLK180, and CLKDV outputs are available.

On-chip synchronization is achieved by connecting the CLKFB input to a point on the global clock network driven by a BUFG, a global clock buffer. The BUFG connected to the CLKFB input of the DCM must be sourced from either the CLK0 or CLK2X outputs of the same DCM. The CLKIN input should be connected to the output of an IBUFG, with the IBUFG input connected to a pad driven by the system clock.

Off-chip synchronization is achieved by connecting the CLKFB input to the output of an IBUFG, with the IBUFG input connected to a pad. Either the CLK0 or CLK2X output can be used but not both. The CLK0 or CLK2X must be connected to the input of OBUF, an output buffer. The CLK_FEEDBACK attribute controls whether the CLK0 output, the default, or the CLK2X output is the source of the CLKFB input.

The duty cycle of the CLK0 output is 50-50 unless the DUTY_CYCLE_CORRECTION attribute is set to FALSE, in which case the duty cycle is the same as that of the CLKIN input. The duty cycle of the phase shifted outputs (CLK90, CLK180, and CLK270) is the same as that of the CLK0 output. The duty cycle of the CLK2X, CLK2X180, and CLKDV outputs is 50-50 unless CLKDV_DIVIDE is a non-integer and the

DLL_FREQUENCY_MODE is HIGH (see the "CLKDV_DIVIDE" section of the *Constraints Guide* for details). The frequency of the CLKDV output is determined by the value assigned to the CLKDV_DIVIDE attribute.

Table 4-20 DCM Clock Delay Lock Loop Outputs

Output	Description
CLK0	Clock at 1x CLKIN frequency
CLK90*	Clock at 1x CLK0 frequency, shifted 90^{o} with regards to CLK0
CLK180	Clock at 1x CLK0 frequency, shifted 180^{o} with regards to CLK0
CLK270*	Clock at 1x CLK0 frequency, shifted 270^{o} with regards to CLK0
CLK2X*	Clock at 2x CLK0 frequency, in phase with CLK0
CLK2X180*	Clock at 2x CLK0 frequency shifted 180^{o} with regards to CLK2X
CLKDV	Clock at (1/n) x CLK0 frequency, where n=CLKDV_DIVIDE value. CLKDV is in phase with CLK0.
LOCKED	All enabled DCM features locked.

* The CLK90, CLK270, CLK2X, and CLK2X180 outputs are *not* available if the DLL_FREQUENCY_MODE is set to High.

Digital Frequency Synthesizer (DFS)

The CLKFX and CLKFX180 outputs in conjunction with the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes provide a frequency synthesizer that can be any multiple or division of CLKIN. CLKFX and CLKIN are in phase every CLKFX_MULTIPLY cycles of CLKFX and every CLKFX_DIVIDE cycles of CLKIN when a feedback is provided to the CLKFB input of the DLL.The frequency of CLKFX is defined by the following equation.

$$Frequency_{CLKFX} = (CLKFX\_MULTIPLY\_value / CLKFX\_DIVIDE\_value) * Frequency_{CLKIN}$$

Both the CLKFX or CLKFX180 output can be used simultaneously.

CLKFX180 is 1x the CLKFX frequency, shifted 180^{o} with regards to CLKFX. CLKFX and CLKFX180 always have a 50/50 duty cycle.

The DFS_FREQUENCY_MODE attribute specifies the allowable input clock and output clock frequency ranges.

See *The Programmable Logic Data Book* for the allowable frequency range of CLKFX.

Digital Phase Shifter (DPS)

The phase shift (skew) between the rising edges of CLKIN and CLKFB may be configured as a fraction of the CLKIN period with the PHASE_SHIFT attribute. This allows the phase shift to remain constant as ambient conditions change. The CLKOUT_PHASE_SHIFT attribute controls the use of the PHASE_SHIFT value. By default, the CLKOUT_PHASE_SHIFT attribute is set to NONE and the PHASE_SHIFT attribute has no effect.

Note By creating skew between CLKIN and CLKFB, all DCM output clocks are phase shifted by the amount of the skew.

When the CLKOUT_PHASE_SHIFT attribute is set to FIXED, the skew set by the PHASE_SHIFT attribute is used at configuration for the rising edges of CLKIN and CLKFB. The skew remains constant.

When the CLKOUT_PHASE_SHIFT attribute is set to VARIABLE, the skew set at configuration is used as a starting point and the skew value can be changed dynamically during operation using the PS* signals. This digital phase shifter feature is controlled by a synchronous interface. The inputs PSEN (phase shift enable) and PSINCDEC (phase shift increment / decrement) are set up to the rising edge of PSCLK (phase shift clock). The PSDONE (phase shift done) output is clocked with the rising edge of PSCLK (the phase shift clock). PSDONE must be connected to implement the complete synchronous interface. The rising-edge skew between CLKIN and CLKFB may be dynamically adjusted after the LOCKED output goes High. The PHASE_SHIFT attribute value specifies the initial phase shift amount when the device is configured. Then the PHASE_SHIFT value is changed one unit when PSEN is activated for one period of PSCLK. The PHASE_SHIFT value is incremented when PSINCDEC is High and decremented when PSINCDEC is Low during the period that PSEN is High. When the DCM completes an increment or decrement operation, the PSDONE output goes High for a single PSCLK cycle to indicate the operation is complete. At this point the next change may be made. When RST (reset) is High, the PHASE_SHIFT attribute value is reset to the skew value set at configuration.

Note If CLKOUT_PHASE_SHIFT is FIXED or NONE, the PSEN, PSINCDEC, and PSCLK inputs must be tied to GND. The program will automatically tie the inputs to GND if they are not connected by the user.

Digital Spread Spectrum (DSS)

The digital spread spectrum function of DCM broadens the frequency spectrum of the output clocks to help meet FCC requirements. Spread spectrum clocking is a simple method to lower electromagnetic interference (EMI). A digital system can create a severe EMI spike at the clock frequency. Spread spectrum clocking speeds up and slows down the clock within a few percent of the target frequency, thus flattening out the EMI peak by spreading it across a range of frequencies.

When the DSS_MODE attribute is set to NONE, the DSSEN input has no effect. When DSS_MODE is set to a value other than NONE and DSSEN is High, the output clock frequency is modulated by the amount of spread specified by the DSS_MODE value.

Additional Status Bits

The STATUS output bits returns the following information.

Table 4-21 DCM Additional Status Bits

Bit	Description
0	Phase Shift Overflow* 1 = |PHASE_SHIFT| > 255
1	DLL CLKIN stopped** 1 = CLKIN stopped toggling
2	N / A
3	N / A
4	N / A
5	N / A

Table 4-21 DCM Additional Status Bits

Bit	Description
6	N/A
7	N/A

Note * Phase Shift Overflow will also go high if the end of the phase shift delay line is reached (see the product data sheet for the most current value of the maximum shifting delay). ** If only the DFS outputs are used (CLKFX & CLKFX180), this status bit will not go high if CLKIN stops

LOCKED

When LOCKED is high, all enabled signals are locked.

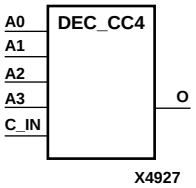
RST

The master reset input (RST) resets DCM to its initial (power-on) state. The signal at the RST input is asynchronous and must be held High for 2ns.

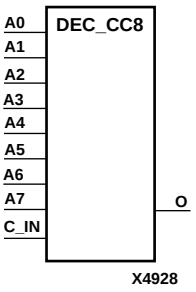
DEC_CC4, 8, 16

4-, 8-, 16-Bit Active Low Decoders

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A

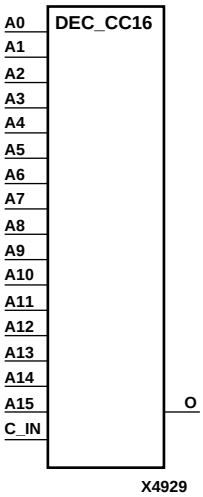


These decoders are used to build wide-decoder functions. They are implemented by cascading CY_MUX elements driven by lookup tables (LUTs). The C_IN pin can only be driven by a CY_INIT or by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.



Inputs					Outputs
A0	A1	...	Az	C_IN	O
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0

z = 3 for DEC_CC4; z = 7 for DECC_CC8; z = 15 for DECC_CC16



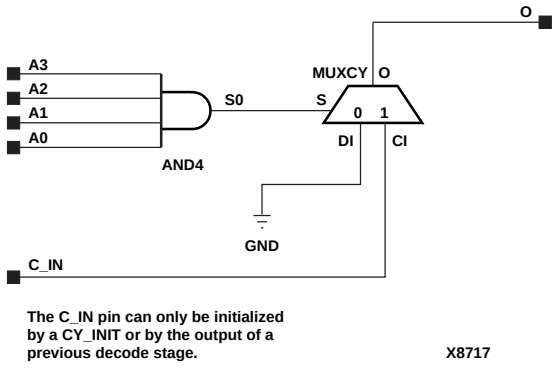


Figure 4-60 DEC_CC4 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

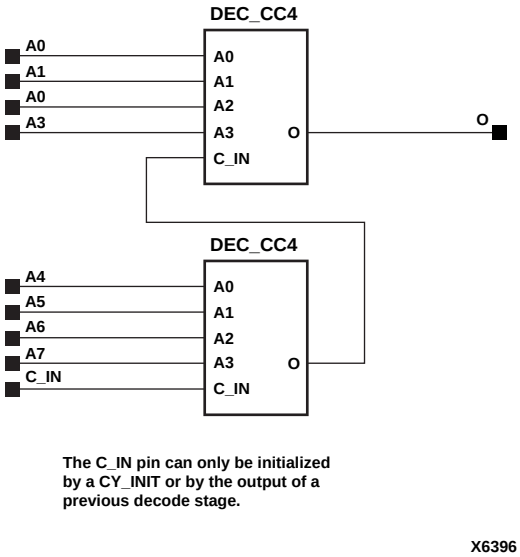


Figure 4-61 DEC_CC8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

DECODE4, 8, 16

4-, 8-, 16-Bit Active-Low Decoders

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A

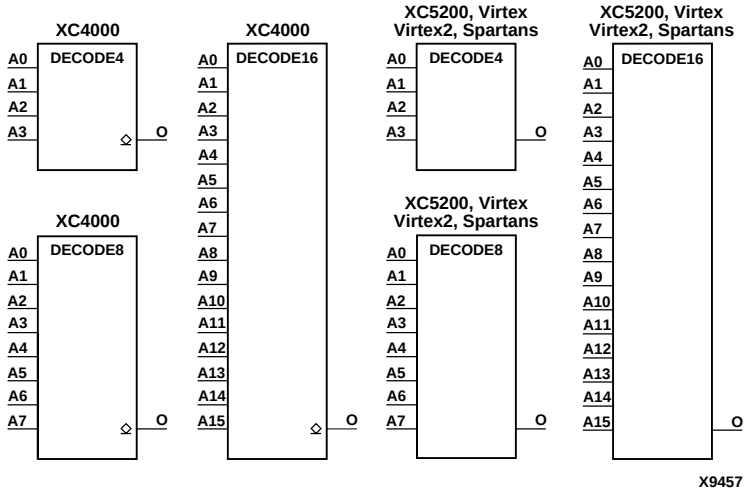


Figure 4-62 DECODE Representations

In Spartan-II, , Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, decoders are implemented using combinations of LUTs and MUXCYs.

Inputs				Outputs*
A0	A1	...	Az	O
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = 3 for DECODE4, z = 7 for DECODE8; z = 15 for DECODE16

*A pull-up resistor must be connected to the output to establish High-level drive current.

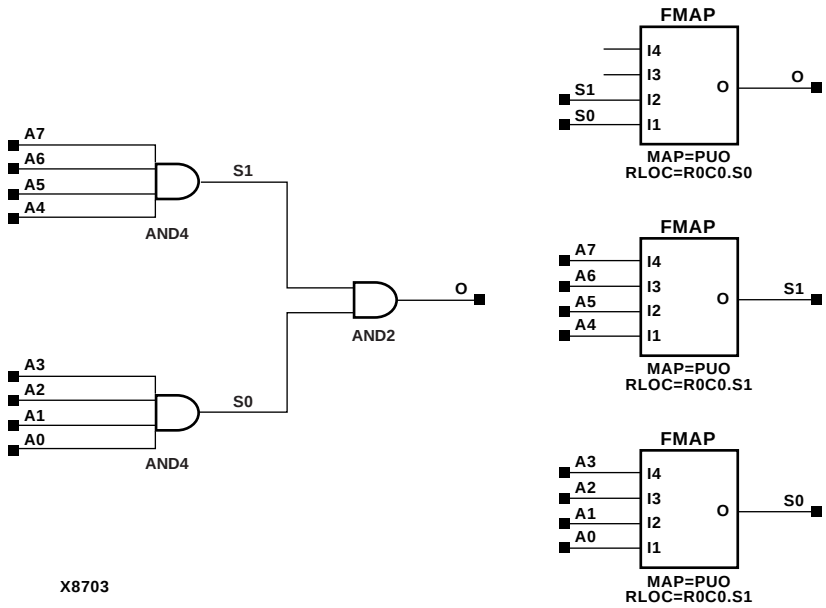


Figure 4-63 DECODE8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

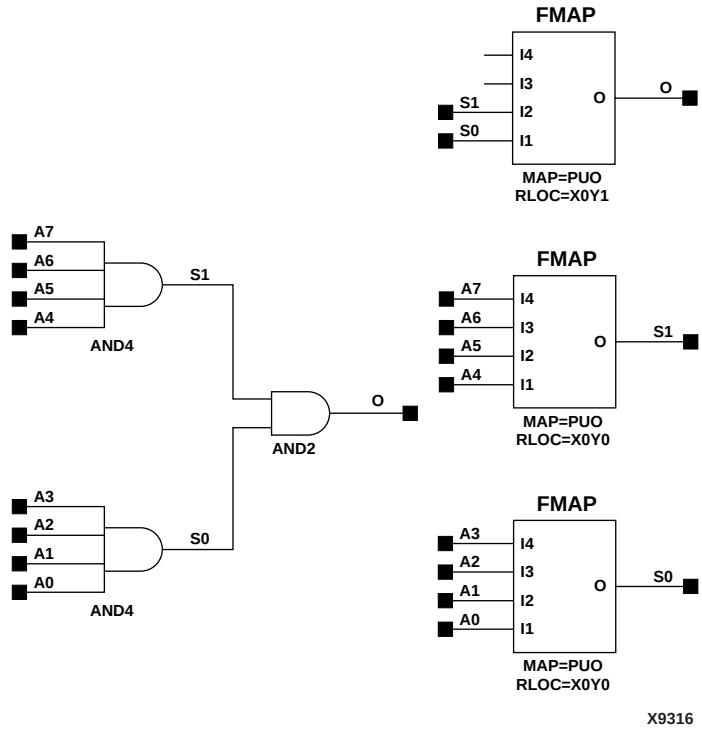
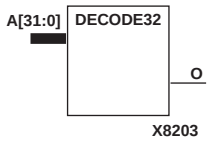


Figure 4-64 DECODE8 Implementation Virtex-II, Virtex-II PRO

DECODE32, 64

32- and 64-Bit Active-Low Decoders

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



DECODE32 and DECODE64 are 32- and 64-bit active-low decoders. These decoders are implemented using combinations of LUTs and MUXCYs.

See the "DECODE4, 8, 16" section for a representative schematic.

Inputs				Outputs
A0	A1	...	Az	O
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = 31 for DECODE32
z = 63 for DECODE64

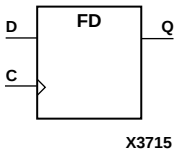
Chapter 5

FD to FTSRLE

FD

D Flip-Flop

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FD is a single D-type flip-flop with data input (D) and data output (Q). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

See the "FD4, 8, 16" section for information on multiple D flip-flops for XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II.

Inputs		Outputs
D	C	Q
0	↑	0
1	↑	1

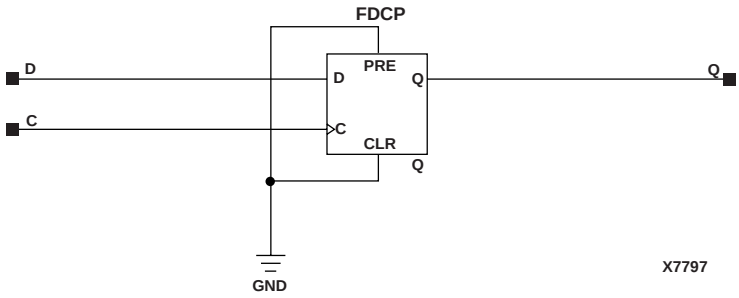
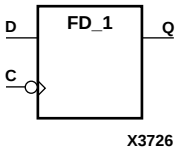


Figure 5-1 FD Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FD_1

D Flip-Flop with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FD_1 is a single D-type flip-flop with data input (D) and data output (Q). The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

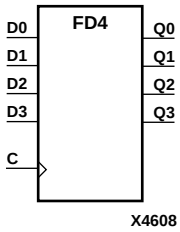
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	C	Q
0	↓	0
1	↓	1

FD4, 8, 16

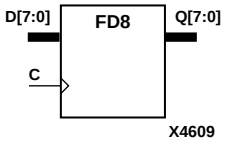
Multiple D Flip-Flops

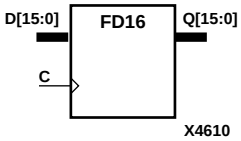
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro



FD4, FD8, FD16 are multiple D-type flip-flops with data inputs (D) and data outputs (Q). FD4, FD8, and FD16 are, respectively, 4-bit, 8-bit, and 16-bit registers, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.





Inputs		Outputs
Dz – D0	C	Qz – Q0
0	↑	0
1	↑	1

z = 3 for FD4; z = 7 for FD8; z = 15 for FD16

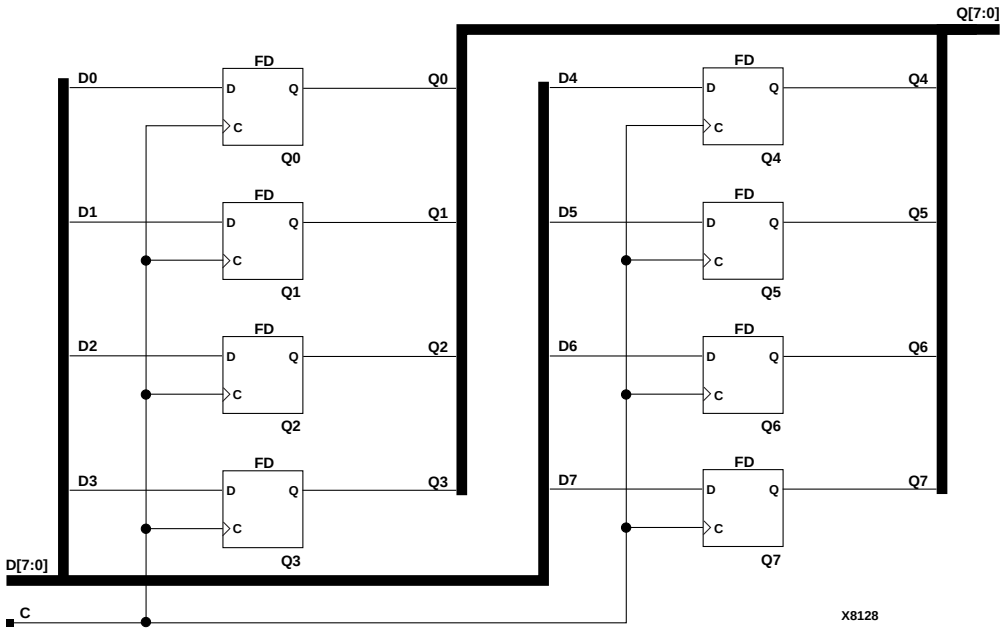
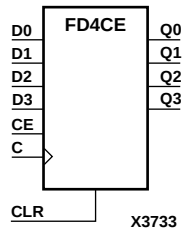


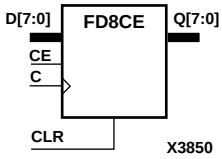
Figure 5-2 FD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

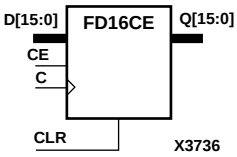
FD4CE, FD8CE, FD16CE

4-, 8-, 16-Bit Data Registers with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







FD4CE, FD8CE, and FD16CE are, respectively, 4-, 8-, and 16-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

The flip-flops are asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
CLR	CE	Dz – D0	C	Qz – Q0
1	X	X	X	0
0	0	X	X	No Chg
0	1	Dn	↑	dn

z = 3 for FD4CE; z = 7 for FD8CE; z = 15 for FD16CE.

dn = state of corresponding input (Dn) one setup time prior to active clock transition

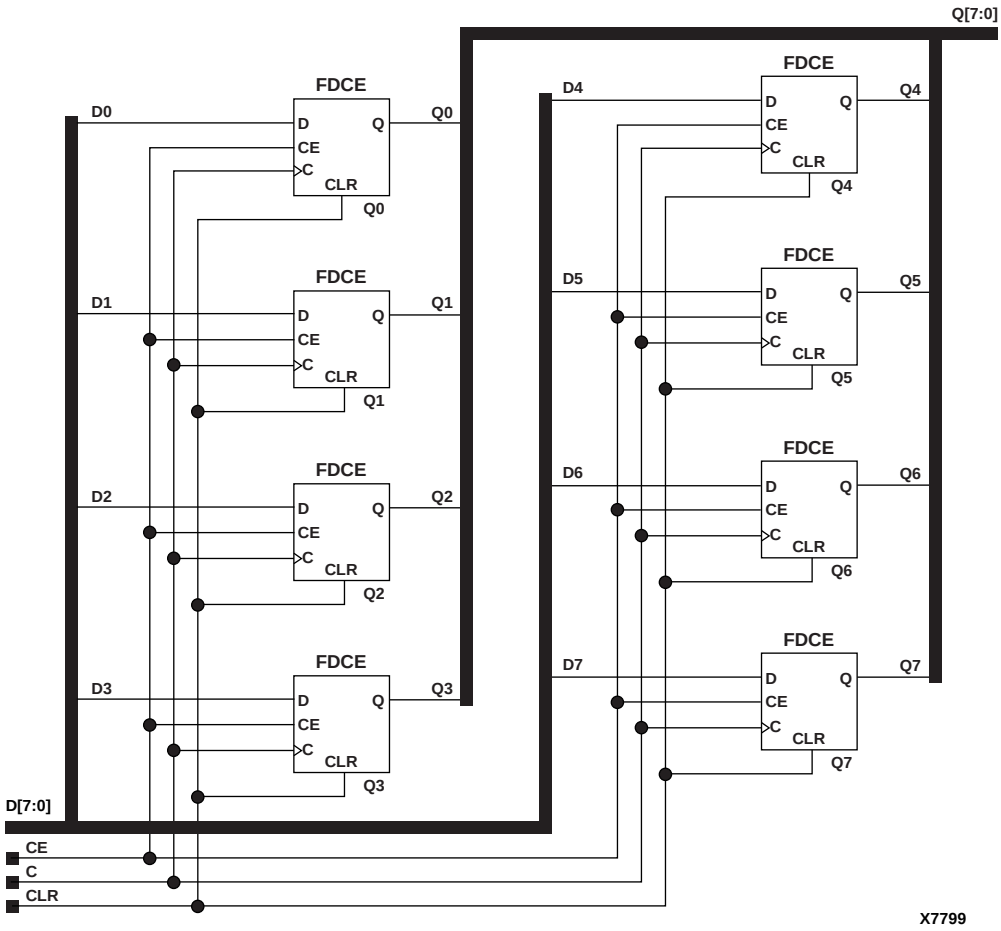
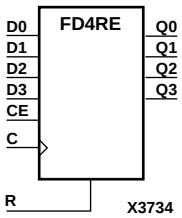


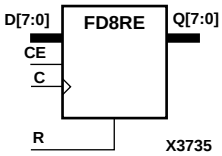
Figure 5-3 FD8CE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

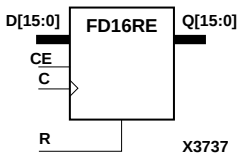
FD4RE, FD8RE, FD16RE

4-, 8-, 16-Bit Data Registers with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







FD4RE, FD8RE, and FD16RE are, respectively, 4-, 8-, and 16-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

The flip-flops are asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
R	CE	Dz – D0	C	Qz – Q0
1	X	X	↑	0
0	0	X	X	No Chg
0	1	Dn	↑	dn

z = 3 for FD4RE; z = 7 for FD8RE; z = 15 for FD16RE

dn = state of referenced input (Dn) one setup time prior to active clock transition

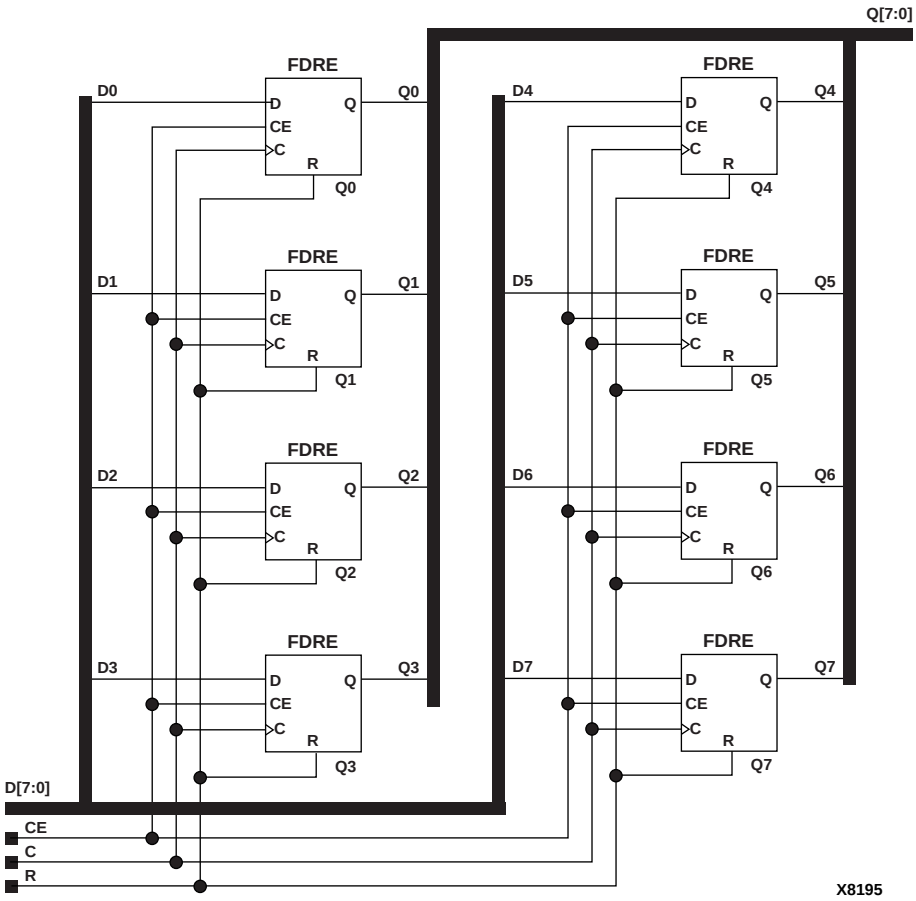
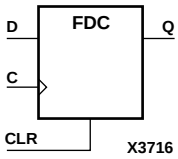


Figure 5-4 FD8RE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

FDC

D Flip-Flop with Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDC is a single D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop when CLR is Low on the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CLR	D	C	Q
1	X	X	0
0	1	↑	1
0	0	↑	0

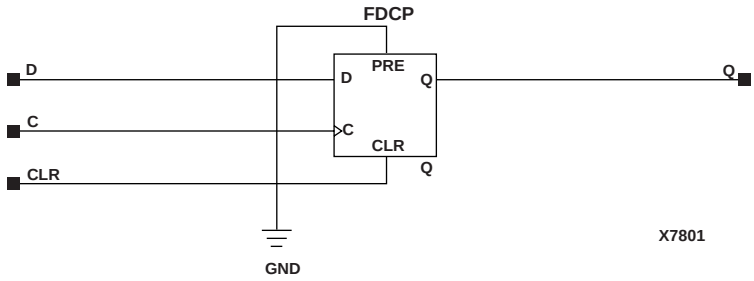
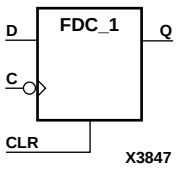


Figure 5-5 FDC Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FDC_1

D Flip-Flop with Negative-Edge Clock and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDC_1 is a single D-type flip-flop with data input (D), asynchronous clear input (CLR), and data output (Q). The asynchronous CLR, when active, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

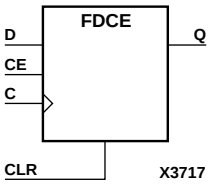
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CLR	D	C	Q
1	X	X	0
0	1	↓	1
0	0	↓	0

FDCE

D Flip-Flop with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive



FDCE is a single D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of FDCE is transferred to the corresponding data output (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

For XC9500XL and XC9500XV devices, logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDCE and FDPE flip-flops primitives may take advantage of the clock-enable p-term.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

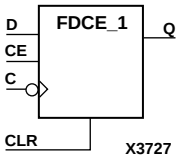
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
CLR	CE	D	C	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0

FDCE_1

D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDCE_1 is a single D-type flip-flop with data (D), clock enable (CE), asynchronous clear (CLR) inputs, and data output (Q). The asynchronous CLR input, when High, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop when CLR is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

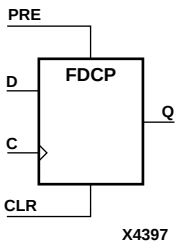
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
CLR	CE	D	C	Q
1	X	X	X	0
0	0	X	↓	No Chg
0	1	1	↓	1
0	1	0	↓	0

FDCP

D Flip-Flop Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive



FDCP is a single D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low on the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

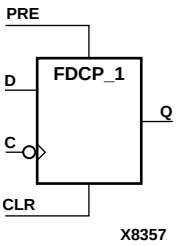
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
CLR	PRE	D	C	Q
1	X	X	X	0
0	1	X	X	1
0	0	0	↑	0
0	0	1	↑	1

FDCP_1

D Flip-Flop with Negative-Edge Clock and Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDCP_1 is a single D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low on the High-to-Low clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

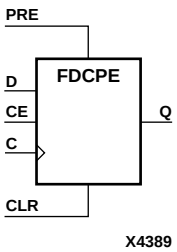
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
CLR	PRE	D	C	Q
1	X	X	X	0
0	1	X	X	1
0	0	0	↓	0
0	0	1	↓	1

FDCPE

D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDCPE is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs
CLR	PRE	CE	D	C	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	↑	0
0	0	1	1	↑	1

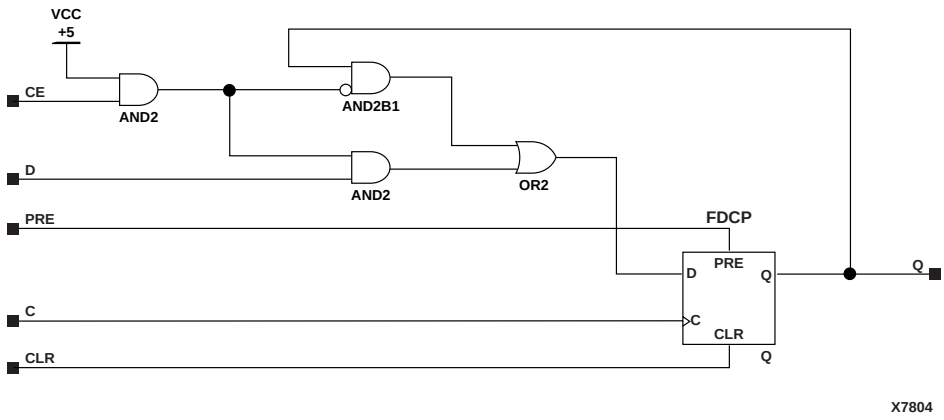
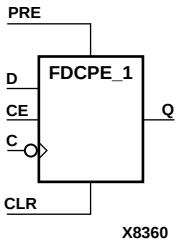


Figure 5-6 FDCPE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FDCPE_1

D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDCPE_1 is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

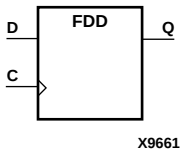
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs
CLR	PRE	CE	D	C	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	↓	0
0	0	1	1	↓	1

FDD

Dual Edge Triggered D Flip-Flop

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDD is a single dual edge triggered D-type flip-flop with data input (D) and data output (Q). The data on the D input is loaded into the flip-flop during the Low-to-High and the High-to-Low clock (C) transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

See the FDD4,8,16 section for information on multiple D flip-flops for the XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II.

Inputs		Outputs
D	C	Q
0	↑	0
1	↑	1
0	↓	0
1	↓	1

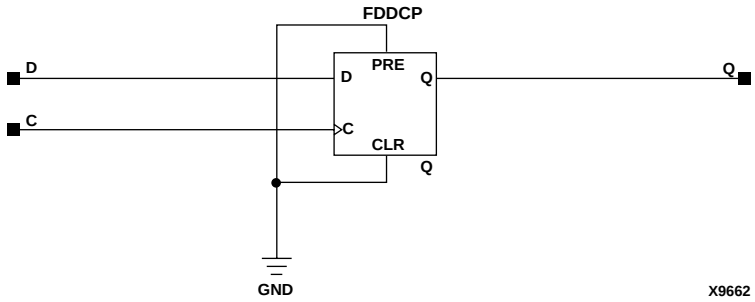
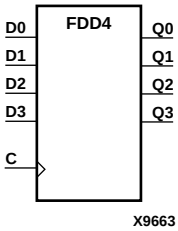


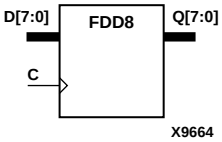
Figure 5-7 FDD Implementation CoolRunner-II

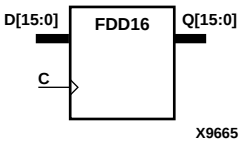
FDD4,8,16

Multiple Dual Edge Triggered D Flip-Flops

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro







FDD4, FDD8, FDD16 are multiple dual edge triggered D-type flip-flops with data inputs (D) and data outputs (Q). FDD4, FDD8, and FDD16 are, respectively, 4-bit, 8-bit, and 16-bit registers, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions.

The flip-flops are asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs		Outputs
Dz – D0	C	Qz – Q0
0	↑	0
1	↑	1
0	↓	0
1	↓	1

z = 3 for FDD4; z = 7 for FDD8; z = 15 for FDD16

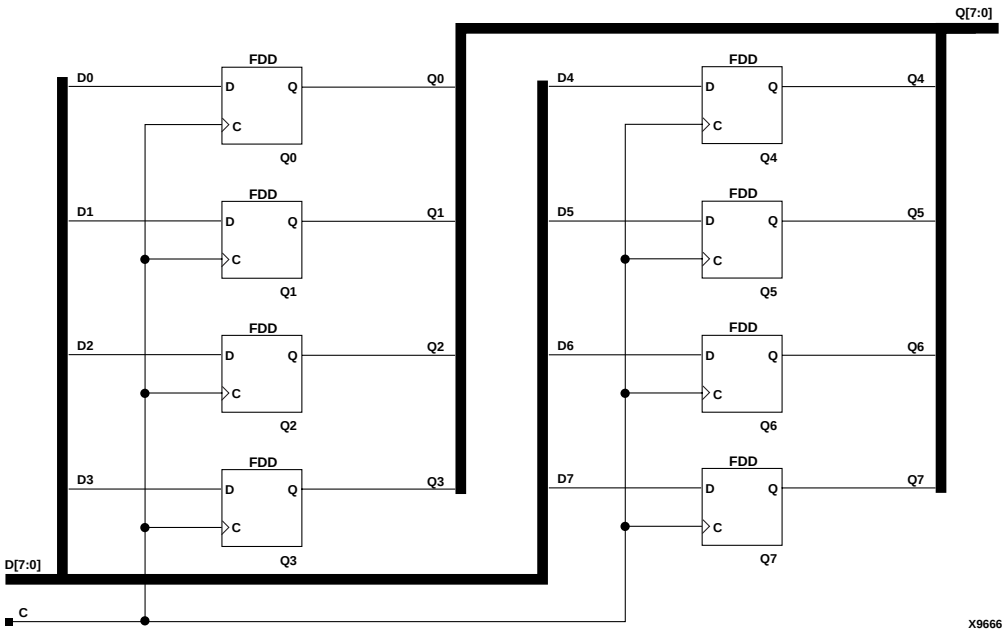
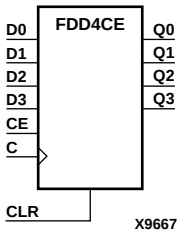


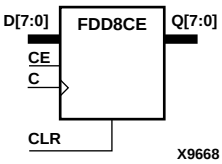
Figure 5-8 FDD8 Implementation CoolRunner-II

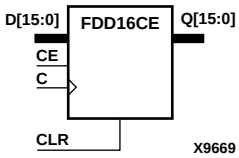
FDD4CE, FDD8CE, FDD16CE

4-, 8-, 16-Bit Dual Edge Triggered Data Registers with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro







FDD4CE, FDD8CE, and FDD16CE are, respectively, 4-, 8-, and 16-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

The flip-flops are asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
CLR	CE	Dz – D0	C	Qz – Q0
1	X	X	X	0
0	0	X	X	No Chg
0	1	Dn	↑	dn
0	1	Dn	↓	dn

z = 3 for FDD4CE; z = 7 for FDD8CE; z = 15 for FDD16CE.

dn = state of corresponding input (Dn) one setup time prior to active clock transitions

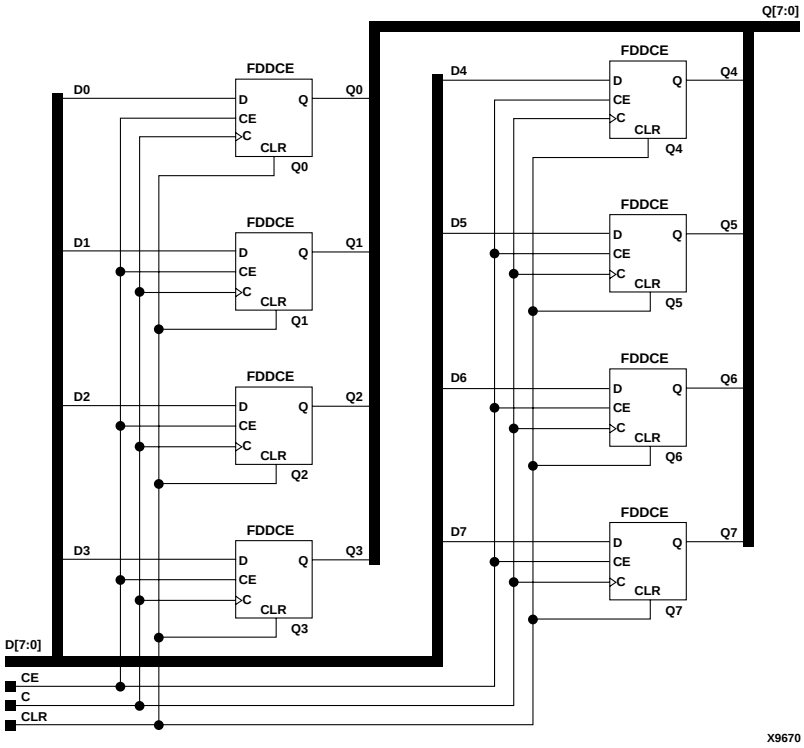
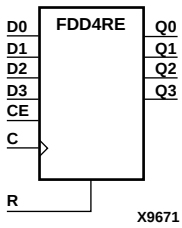


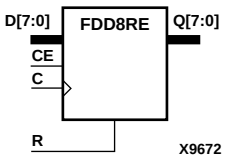
Figure 5-9 FDD8CE Implementation CoolRunner-II

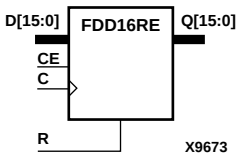
FDD4RE, FDD8RE, FDD16RE

4-, 8-, 16-Bit Dual Edge Triggered Data Registers with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro







FDD4RE, FDD8RE, and FDD16RE are, respectively, 4-, 8-, and 16-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High or High-to-Low clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

The flip-flops are asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
R	CE	Dz – D0	C	Qz – Q0
1	X	X	↑	0
1	X	X	↓	0
0	0	X	X	No Chg
0	1	Dn	↑	dn
0	1	Dn	↓	dn

z = 3 for FDD4RE; z = 7 for FDD8RE; z = 15 for FDD16RE

dn = state of referenced input (Dn) one setup time prior to active clock transitions

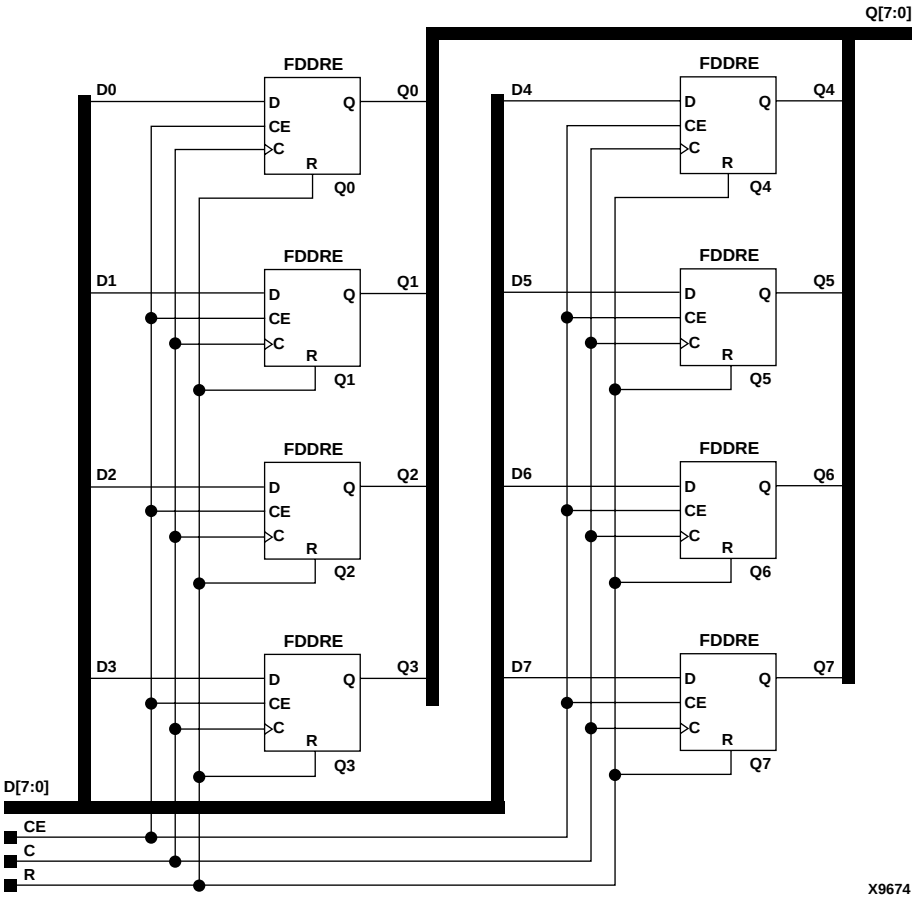
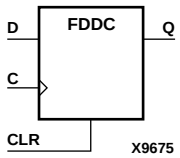


Figure 5-10 FDD8RE Implementation CoolRunner-II

FDDC

D Dual Edge Triggered Flip-Flop with Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDDC is a single dual edge triggered D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop when CLR is Low on the Low-to-High and High-to-Low clock (C) transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs
CLR	D	C	Q
1	X	X	0
0	1	↑	1
0	1	↓	1
0	0	↑	0
0	0	↓	0

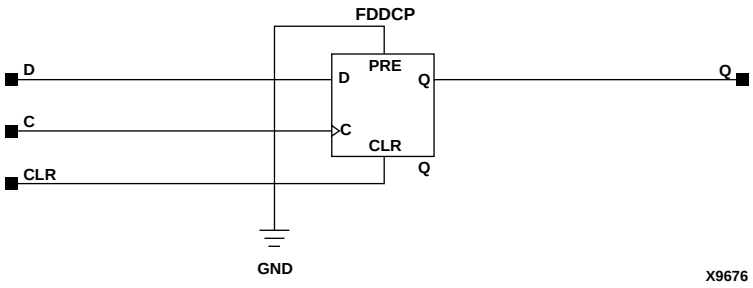
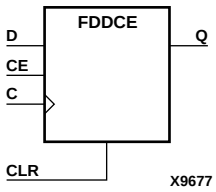


Figure 5-11 FDDC Implementation CoolRunner-II

FDDCE

Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Primitive



FDDCE is a single dual edge triggered D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of FDDCE is transferred to the corresponding data output (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

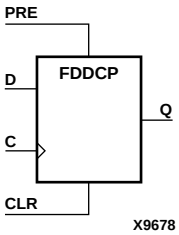
Logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDDCE and FDDPE flip-flops primitives may take advantage of the clock-enable p-term.

Inputs				Outputs
CLR	CE	D	C	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0
0	1	1	↓	1
0	1	0	↓	0

FDDCP

Dual Edge Triggered D Flip-Flop Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Primitive



FDDCP is a single dual edge triggered D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low on the Low-to-High and High-to-Low clock (C) transitions.

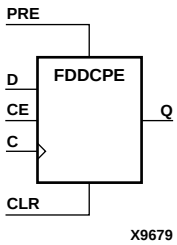
The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
CLR	PRE	D	C	Q
1	X	X	X	0
0	1	X	X	1
0	0	0	↑	0
0	0	1	↑	1
0	0	0	↓	0
0	0	1	↓	1

FDDCPE

Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro



FDDCPE is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
CLR	PRE	CE	D	C	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	↑	0
0	0	1	1	↑	1
0	0	1	0	↓	0
0	0	1	1	↓	1

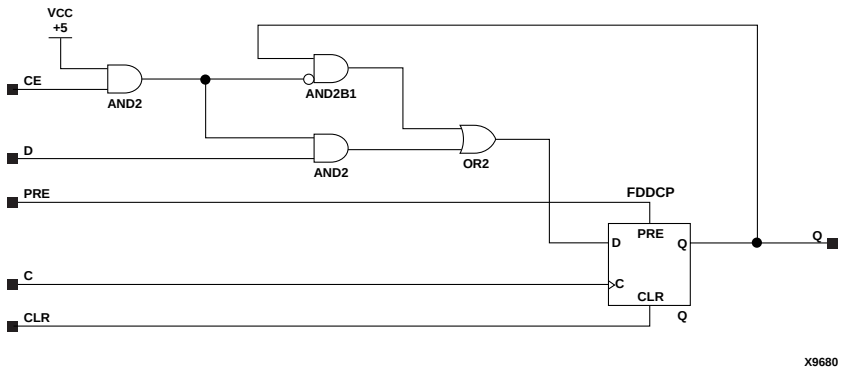
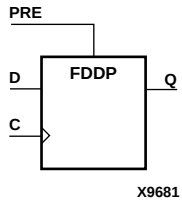


Figure 5-12 FDDCPE Implementation CoolRunner-II

FDDP

Dual Edge Triggered D Flip-Flop with Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDDP is a single dual edge triggered D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the Low-to-High and High-to-Low clock (C) transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs
PRE	C	D	Q
1	X	X	1
0	↑	1	1
0	↑	0	0
0	↓	1	1
0	↓	0	0

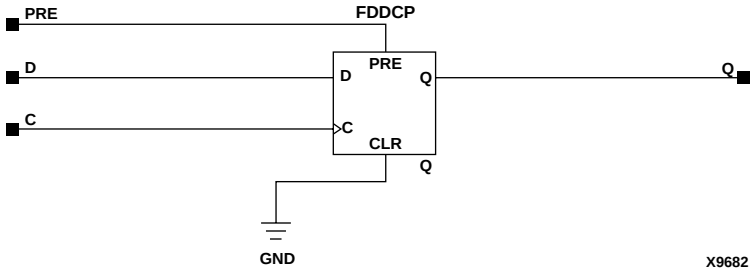
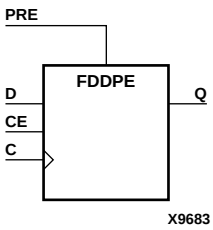


Figure 5-13 FDDP Implementation CoolRunner-II

FDDPE

Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Primitive



FDDPE is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

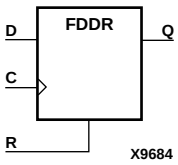
Logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDDCE and FDDPE flip-flops primitives may take advantage of the clock-enable p-term.

Inputs				Outputs
PRE	CE	D	C	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	0	↑	0
0	1	1	↑	1
0	1	0	↓	0
0	1	1	↓	1

FDDR

Dual Edge Triggered D Flip-Flop with Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDDR is a single dual edge triggered D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High and High-to-Low clock (C) transitions. The data on the D input is loaded into the flip-flop when R is Low during the Low-to-High or High-to-Low clock transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs
R	D	C	Q
1	X	↑	0
1	X	↓	0
0	1	↑	1
0	0	↑	0
0	1	↓	1
0	0	↓	0

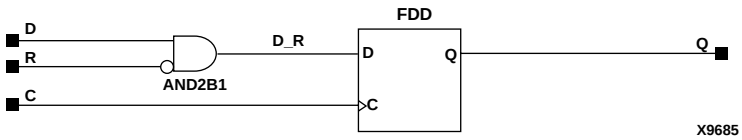
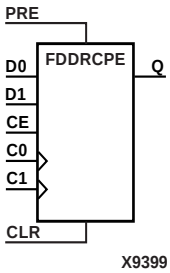


Figure 5-14 FDDR Implementation CoolRunner-II

FDDRCPE

Dual Data Rate D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



FDDRCPE is a Dual Data Rate (DDR) D flip-flop with two separate clocks (C0 and C1) phase shifted 180 degrees that allow selection of two separate data inputs (D0 and D1). It also has clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D0 input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High C0 clock transition. Data on the D1 input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High C1 clock transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

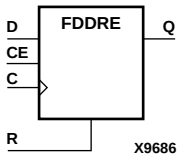
Use the INIT0 attribute to initialize FDDRCPE during configuration.

Inputs							Outputs
C0	C1	CE	D0	D1	CLR	PRE	Q
X	X	X	X	X	1	0	0
X	X	X	X	X	0	1	1
X	X	X	X	X	1	1	0
X	X	0	X	X	0	0	No Chg
↑	X	1	D0	X	0	0	D0
X	↑	1	X	D1	0	0	D1

FDDRE

Dual Edge Triggered D Flip-Flop with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro



FDDRE is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High and High-to-Low clock transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
R	CE	D	C	Q
1	X	X	↑	0
1	X	X	↓	0
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0
0	1	1	↓	1
0	1	0	↓	0

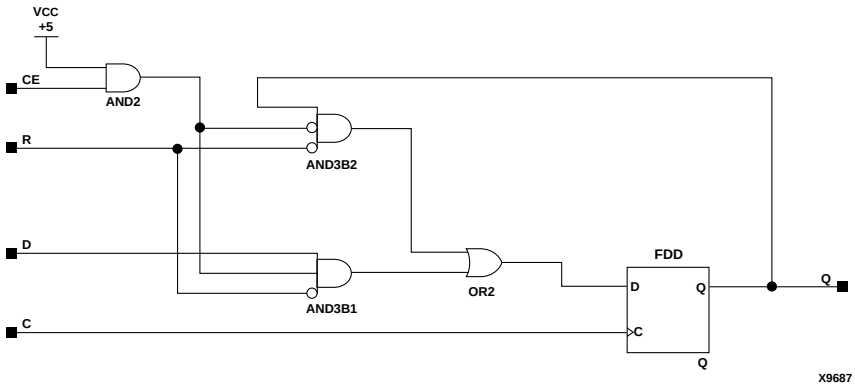
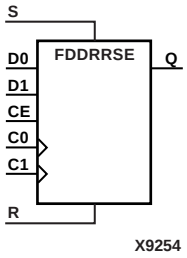


Figure 5-15 FDDRE Implementation CoolRunner-II

FDDRRSE

Dual Data Rate D Flip-Flop with Clock Enable and Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



FDDRRSE is a Dual Data Rate (DDR) D flip-flop with two separate clocks (C0 and C1) phase shifted 180 degrees that allow selection of two separate data inputs (D0 and D1). It also has synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the Q output Low during any Low-to-High clock transition (C0 or C1). (Reset has precedence over Set.) When the S input is High and R is Low, the flip-flop is set, output High, during a Low-to-High clock transition (C0 or C1). Data on the D0 input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High C0 clock transition. Data on the D1 input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High C1 clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

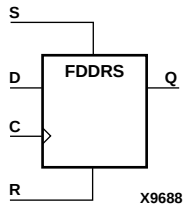
Use the INIT attribute to initialize FDDRRSE during configuration.

Inputs							Outputs
C0	C1	CE	D0	D1	R	S	Q
↑	X	X	X	X	1	0	0
↑	X	X	X	X	0	1	1
↑	X	X	X	X	1	1	0
X	↑	X	X	X	1	0	0
X	↑	X	X	X	0	1	1
X	↑	X	X	X	1	1	0
X	X	0	X	X	0	0	No Chg
↑	X	1	D0	X	0	0	D0
X	↑	1	X	D1	0	0	D1

FDDRS

Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDDRS is a single dual edge triggered D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High or High-to-Low clock (C) transitions. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the Low-to-High or Low-to-High clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the Low-to-High and High-to-Low clock transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
R	S	D	C	Q
1	X	X	↑	0
1	X	X	↓	0
0	1	X	↑	1
0	1	X	↓	1
0	0	1	↑	1
0	0	1	↓	1
0	0	0	↑	0
0	0	0	↓	0

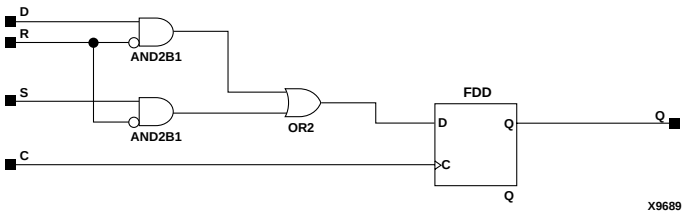
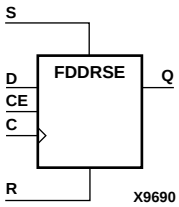


Figure 5-16 FDDRS Implementation CoolRunner-II

FDDRSE

Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro



FDDRSE is a single dual edge triggered D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High or High-to-Low clock transitions. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High or Low-to-High clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High and High-to-Low clock transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↑	0
1	X	X	X	↓	0
0	1	X	X	↑	1
0	1	X	X	↓	1
0	0	0	X	X	No Chg
0	0	1	1	↑	1
0	0	1	0	↑	0
0	0	1	1	↓	1
0	0	1	0	↓	0

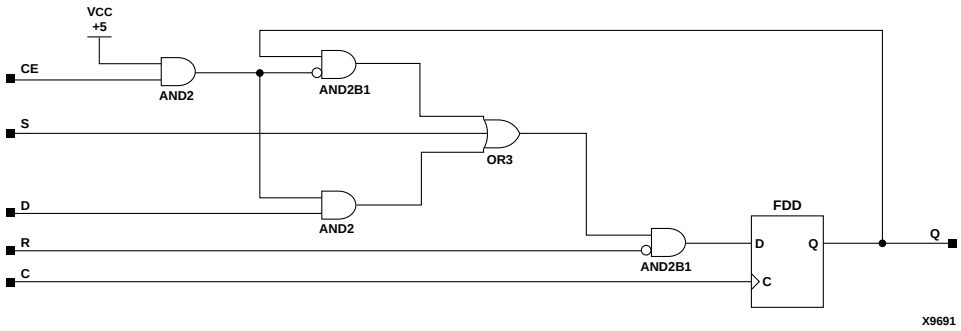
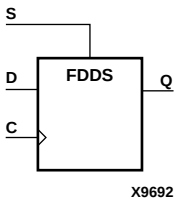


Figure 5-17 FDDRSE Implementation CoolRunner-II

FDDS

Dual Edge Triggered D Flip-Flop with Synchronous Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDDS is a single dual edge triggered D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High and High-to-Low clock (C) transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs
S	D	C	Q
1	X	↑	1
1	X	↓	1
0	1	↑	1
0	0	↑	0
0	1	↓	1
0	0	↓	0

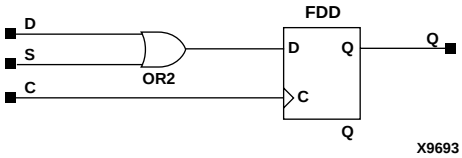
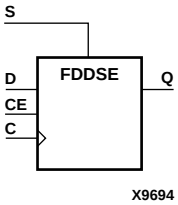


Figure 5-18 FDDS Implementation CoolRunner-II

FDDSE

D Flip-Flop with Clock Enable and Synchronous Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDDSE is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High and High-to-Low clock (C) transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
S	CE	D	C	Q
1	X	X	↑	1
1	X	X	↓	1
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0
0	1	1	↓	1
0	1	0	↓	0

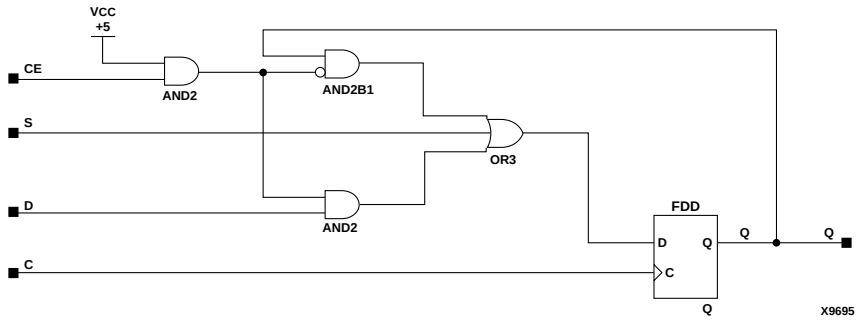
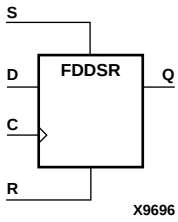


Figure 5-19 FDDSE Implementation CoolRunner-II

FDDSR

Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDDSR is a single dual edge triggered D-type flip-flop with data (D), synchronous reset (R) and synchronous set (S) inputs and data output (Q). When the set (S) input is High, it overrides all other inputs and sets the Q output High during the Low-to-High or High-to-Low clock transition. (Set has precedence over Reset.) When reset (R) is High and S is Low, the flip-flop is reset, output Low, on the Low-to-High or High-to-Low clock transition. Data on the D input is loaded into the flip-flop when S and R are Low on the Low-to-High and High-to-Low clock transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
S	R	D	C	Q
1	X	X	↑	1
1	X	X	↓	1
0	1	X	↑	0
0	1	X	↓	0
0	0	1	↑	1
0	0	0	↑	0
0	0	1	↓	1
0	0	0	↓	0

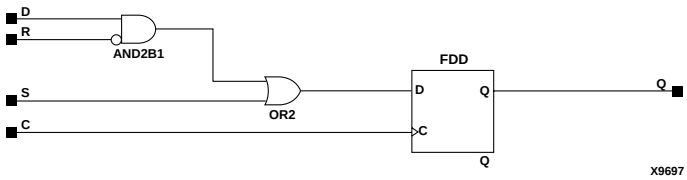
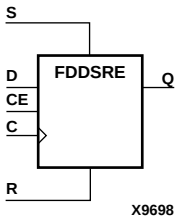


Figure 5-20 FDDSR Implementation CoolRunner-II

FDDSRE

Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FDDSRE is a single dual edge triggered D-type flip-flop with synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High, it overrides all other inputs and sets the Q output High during the Low-to-High or High-to-Low clock transition. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low during the Low-to-High or High-to-Low clock transition. Data is loaded into the flip-flop when S and R are Low and CE is High during the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
S	R	CE	D	C	Q
1	X	X	X	↑	1
1	X	X	X	↓	1
0	1	X	X	↑	0
0	1	X	X	↓	0
0	0	0	X	X	No Chg
0	0	1	1	↑	1
0	0	1	0	↑	0
0	0	1	1	↓	1
0	0	1	0	↓	0

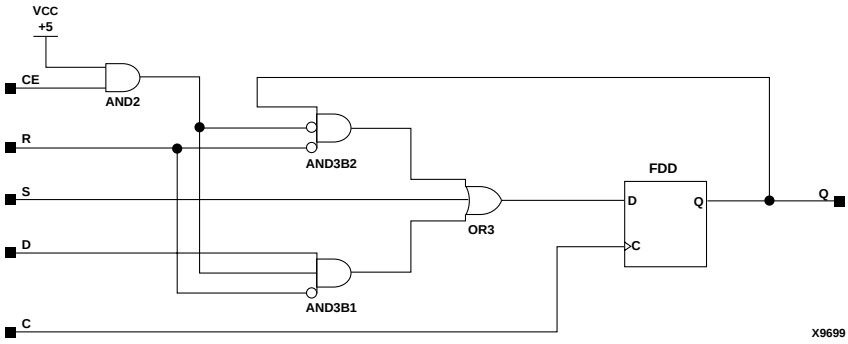
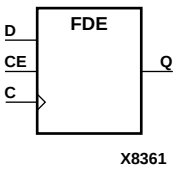


Figure 5-21 FDDSRE Implementation CoolRunner-II

FDE

D Flip-Flop with Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDE is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the D input is loaded into the flip-flop during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

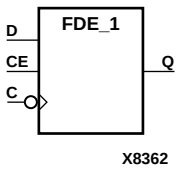
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CE	D	C	Q
0	X	X	No Chg
1	0	↑	0
1	1	↑	1

FDE_1

D Flip-Flop with Negative-Edge Clock and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDE_1 is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

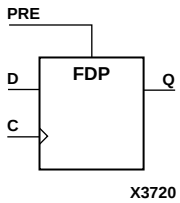
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CE	D	C	Q
0	X	X	No Chg
1	0	↓	0
1	1	↓	1

FDP

D Flip-Flop with Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDP is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

The active level of the GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
PRE	C	D	Q
1	X	X	1
0	↑	1	1
0	↑	0	0

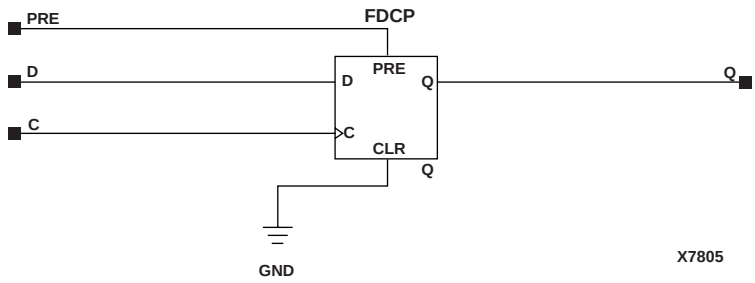
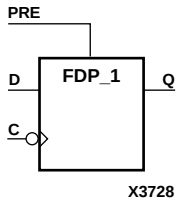


Figure 5-22 FDP Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FDP_1

D Flip-Flop with Negative-Edge Clock and Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDP_1 is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the High-to-Low clock (C) transition.

The flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

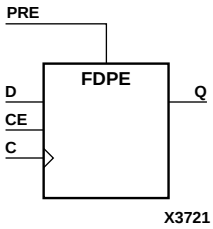
The active level of the GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
PRE	C	D	Q
1	X	X	1
0	↓	1	1
0	↓	0	0

FDPE

D Flip-Flop with Clock Enable and Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive



FDPE is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

For XC9500XL and XC9500XV devices, logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDCE and FDPE flip-flops primitives may take advantage of the clock-enable p-term.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset, output High, when power is applied. These devices simulate power-on when global set/reset (GSR) is active.

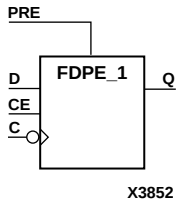
The active level of the GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
PRE	CE	D	C	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	0	↑	0
0	1	1	↑	1

FDPE_1

D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDPE_1 is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

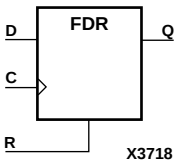
The active level of the GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
PRE	CE	D	C	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	1	↓	1
0	1	0	↓	0

FDR

D Flip-Flop with Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDR is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

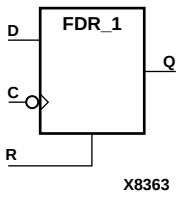
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
R	D	C	Q
1	X	↑	0
0	1	↑	1
0	0	↑	0

FDR_1

D Flip-Flop with Negative-Edge Clock and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDR_1 is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low during the High-to-Low clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

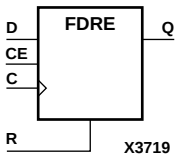
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
R	D	C	Q
1	X	↓	0
0	1	↓	1
0	0	↓	0

FDRE

D Flip-Flop with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDRE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
R	CE	D	C	Q
1	X	X	↑	0
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0

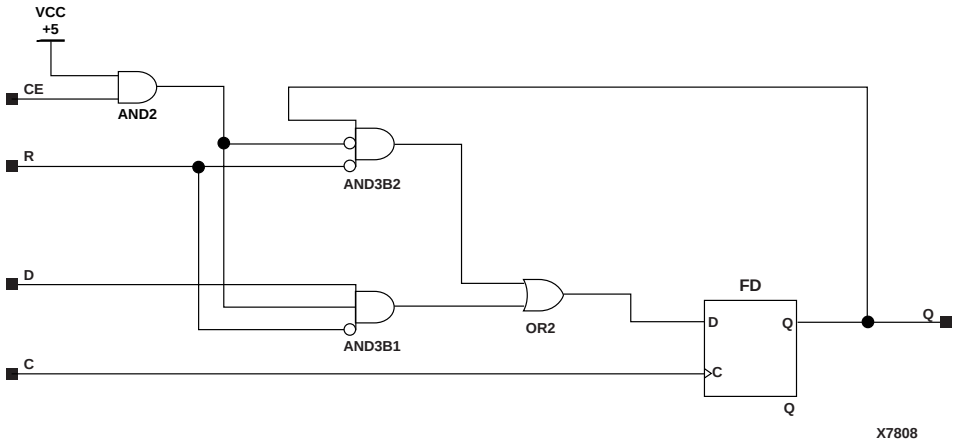
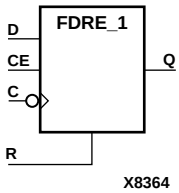


Figure 5-23 FDRE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FDRE_1

D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDRE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low and CE is High during the High-to-Low clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

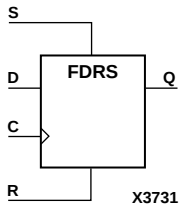
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
R	CE	D	C	Q
1	X	X	↓	0
0	0	X	X	No Chg
0	1	1	↓	1
0	1	0	↓	0

FDRS

D Flip-Flop with Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDRS is a single D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High clock (C) transition. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
R	S	D	C	Q
1	X	X	↑	0
0	1	X	↑	1
0	0	1	↑	1
0	0	0	↑	0

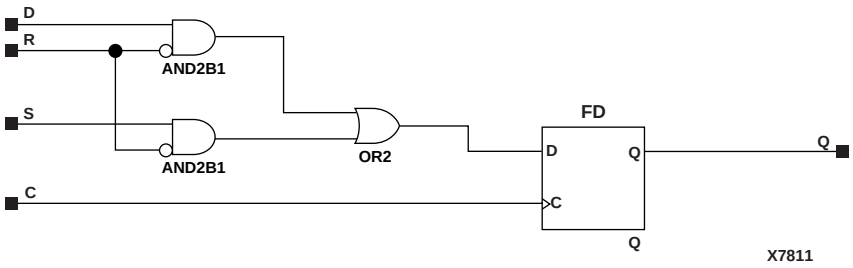
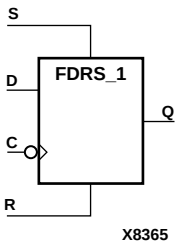


Figure 5-24 FDRS Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FDRS_1

D Flip-Flop with Negative-Clock Edge and Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDRS_1 is a single D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low during the High-to-Low clock (C) transition. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the High-to-Low clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the High-to-Low clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

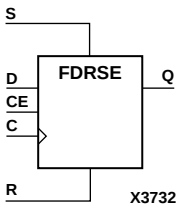
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
R	S	D	C	Q
1	X	X	↓	0
0	1	X	↓	1
0	0	1	↓	1
0	0	0	↓	0

FDRSE

D Flip-Flop with Synchronous Reset and Set and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDRSE is a single D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Chg
0	0	1	1	↑	1
0	0	1	0	↑	0

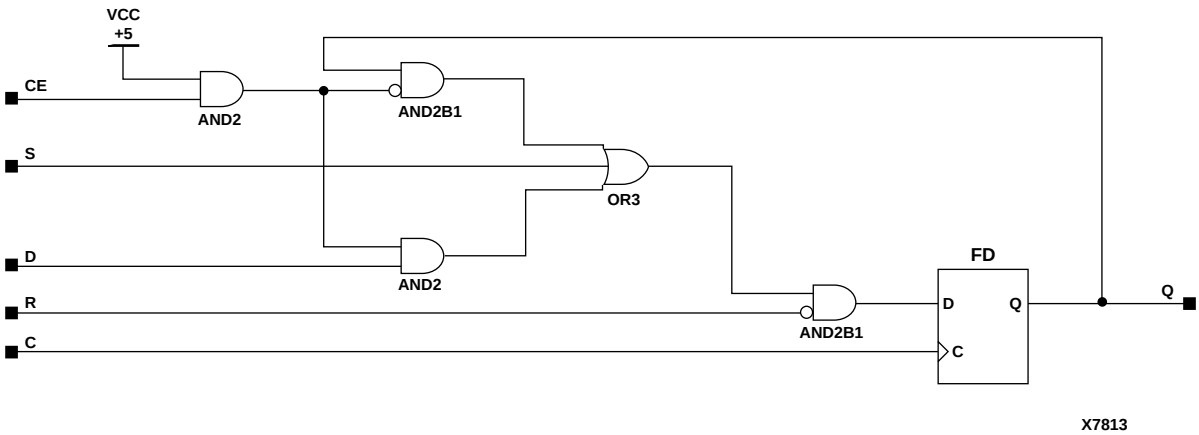
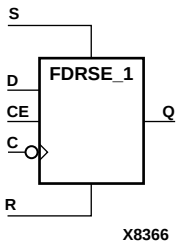


Figure 5-25 FDRSE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FDRSE_1

D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDRSE_1 is a single D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the High-to-Low clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the High-to-Low clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the High-to-Low clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

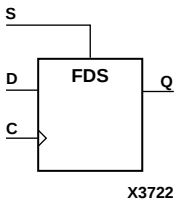
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↓	0
0	1	X	X	↓	1
0	0	0	X	X	No Chg
0	0	1	1	↓	1
0	0	1	0	↓	0

FDS

D Flip-Flop with Synchronous Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset, output High, when power is applied. For all other devices (XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II), the flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

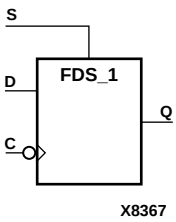
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
S	D	C	Q
1	X	↑	1
0	1	↑	1
0	0	↑	0

FDS_1

D Flip-Flop with Negative-Edge Clock and Synchronous Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDS_1 is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the High-to-Low clock (C) transition.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

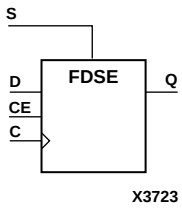
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
S	D	C	Q
1	X	↓	1
0	1	↓	1
0	0	↓	0

FDSE

D Flip-Flop with Clock Enable and Synchronous Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Macro	Macro



FDSE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High clock (C) transition.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO the flip-flop is asynchronously preset, output High, when power is applied.

For all other devices (XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II), the flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
S	CE	D	C	Q
1	X	X	↑	1
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0

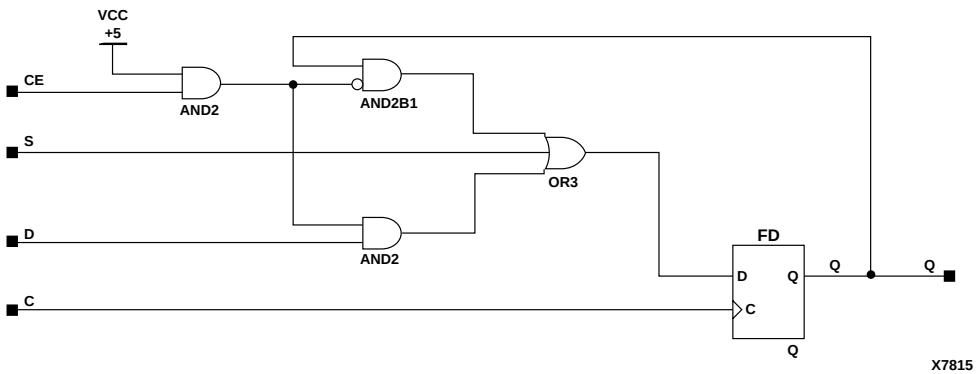
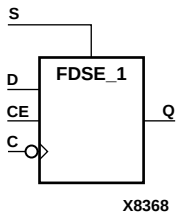


Figure 5-26 FDSE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FDSE_1

D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



FDSE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the High-to-Low clock (C) transition.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

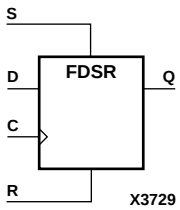
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
S	CE	D	C	Q
1	X	X	↓	1
0	0	X	X	No Chg
0	1	1	↓	1
0	1	0	↓	0

FDSR

D Flip-Flop with Synchronous Set and Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



FDSR is a single D-type flip-flop with data (D), synchronous reset (R) and synchronous set (S) inputs and data output (Q). When the set (S) input is High, it overrides all other inputs and sets the Q output High during the Low-to-High clock transition. (Set has precedence over Reset.) When reset (R) is High and S is Low, the flip-flop is reset, output Low, on the Low-to-High clock transition. Data on the D input is loaded into the flip-flop when S and R are Low on the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
S	R	D	C	Q
1	X	X	↑	1
0	1	X	↑	0
0	0	1	↑	1
0	0	0	↑	0

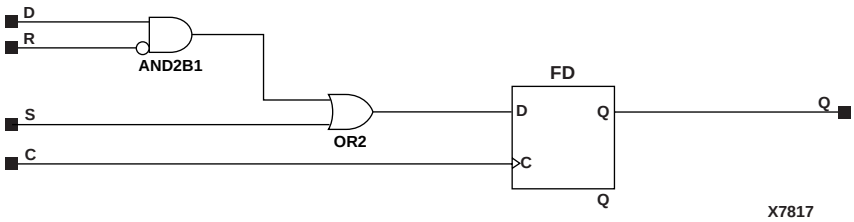
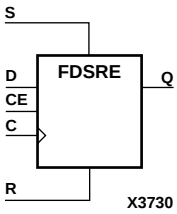


Figure 5-27 FDSR Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FDSRE

D Flip-Flop with Synchronous Set and Reset and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro



FDSRE is a single D-type flip-flop with synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High, it overrides all other inputs and sets the Q output High during the Low-to-High clock transition. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low during the Low-to-High clock transition. Data is loaded into the flip-flop when S and R are Low and CE is High during the Low-to-high clock transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
S	R	CE	D	C	Q
1	X	X	X	↑	1
0	1	X	X	↑	0
0	0	0	X	X	No Chg
0	0	1	1	↑	1
0	0	1	0	↑	0

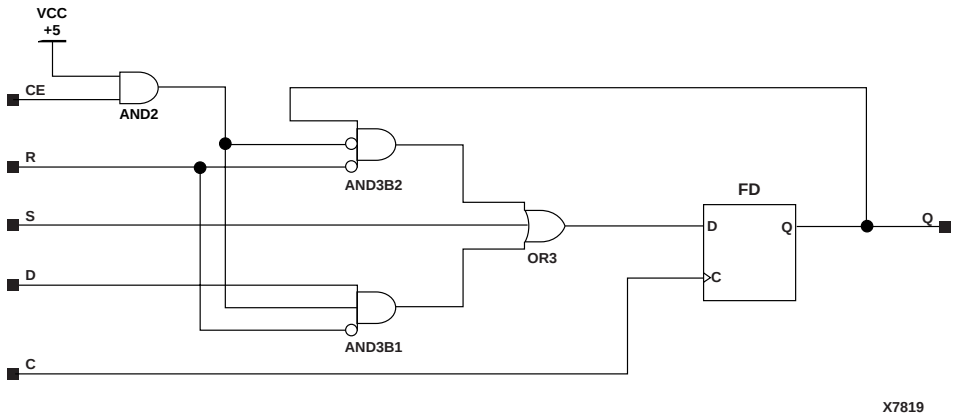
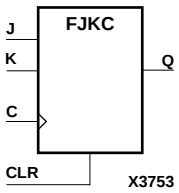


Figure 5-28 FDSRE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FJKC

J-K Flip-Flop with Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FJKC is a single J-K-type flip-flop with J, K, and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the Q output Low. When CLR is Low, the output responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
CLR	J	K	C	Q
1	X	X	X	0
0	0	0	↑	No Chg
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

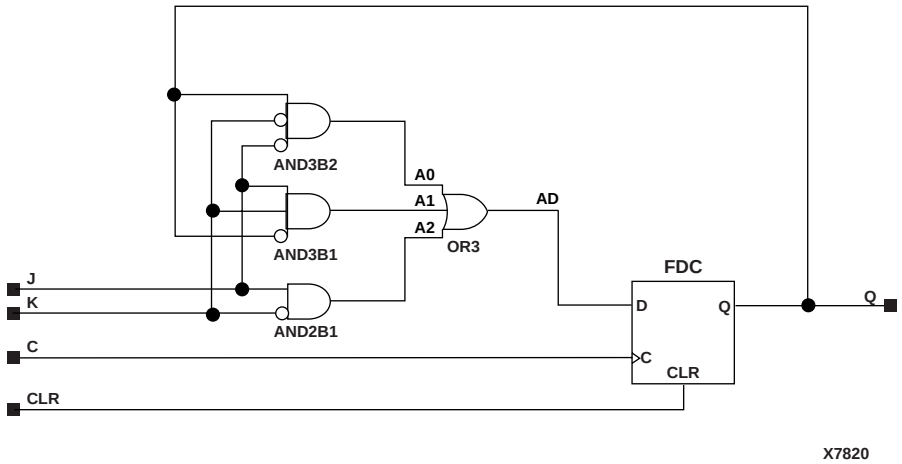


Figure 5-29 FJKC Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

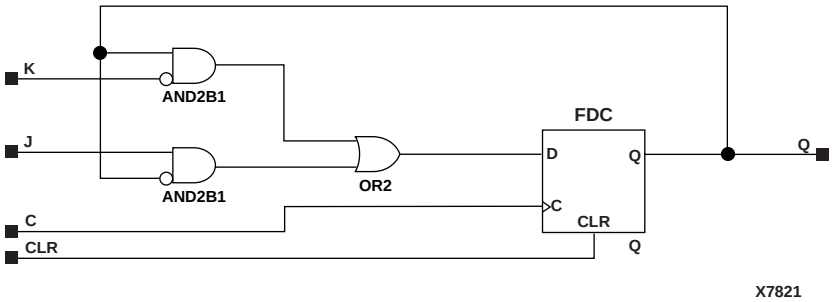
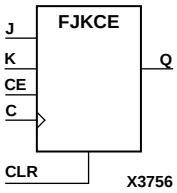


Figure 5-30 FJKC Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FJKCE

J-K Flip-Flop with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FJKCE is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR), when High, overrides all other inputs and resets the Q output Low. When CLR is Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs
CLR	CE	J	K	C	Q
1	X	X	X	X	0
0	0	X	X	X	No Chg
0	1	0	0	X	No Chg
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

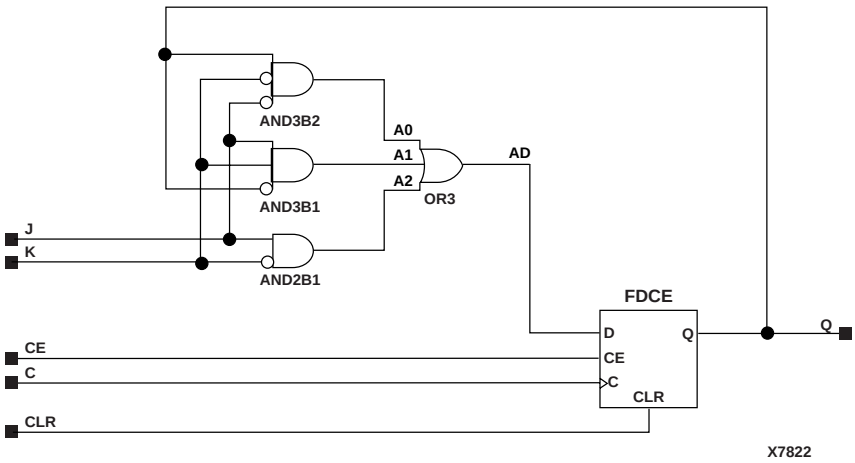


Figure 5-31 FJKCE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

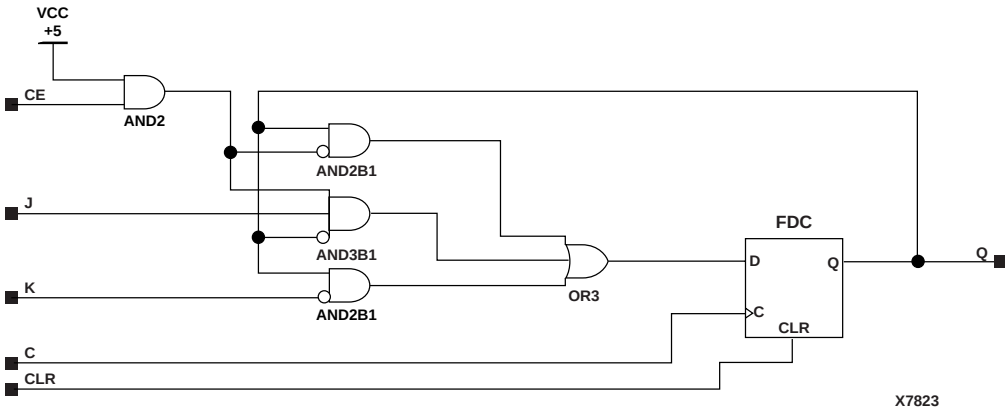
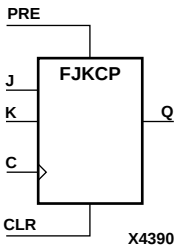


Figure 5-32 FJKCE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FJKCP

J-K Flip-Flop with Asynchronous Clear and Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro



FJKCP is a single J-K-type flip-flop with J, K, asynchronous clear (CLR), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous clear input (CLR), when High, overrides all other inputs and resets the Q output Low. The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the Q output High. When CLR and PRE are Low, Q responds to the state of the J and K inputs during the Low-to-High clock transition, as shown in the following truth table.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
CLR	PRE	J	K	C	Q
1	0	X	X	X	0
0	1	X	X	X	1
0	0	0	0	X	No Chg
0	0	0	1	↑	0
0	0	1	0	↑	1
0	0	1	1	↑	Toggle

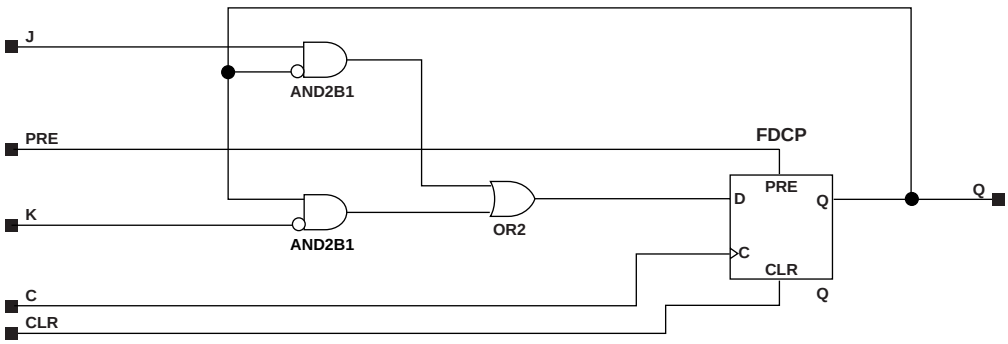
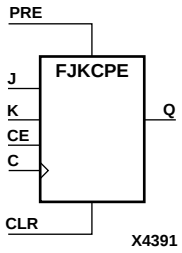


Figure 5-33 FJKCP Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FJKCPE

J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



FJKCPE is a single J-K-type flip-flop with J, K, asynchronous clear (CLR), asynchronous preset (PRE), and clock enable (CE) inputs and data output (Q). The asynchronous clear input (CLR), when High, overrides all other inputs and resets the Q output Low. The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the Q output High. When CLR and PRE are Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs
CLR	PRE	CE	J	K	C	Q
1	X	X	X	X	X	0
0	1	X	X	X	X	1
0	0	0	0	X	X	No Chg
0	0	1	0	0	X	No Chg
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

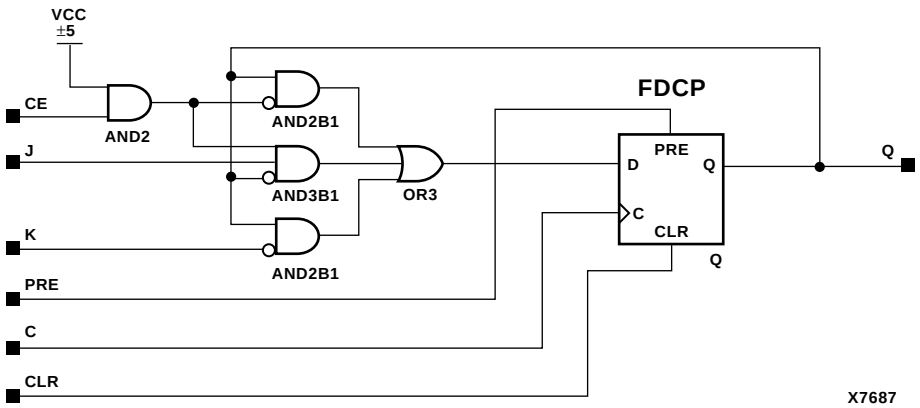
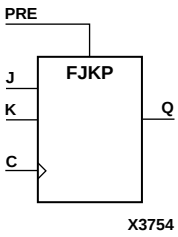


Figure 5-34 FJKCPE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FJKP

J-K Flip-Flop with Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FJKP is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the Q output High. When PRE is Low, the Q output responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock transition.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

The GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
PRE	J	K	C	Q
1	X	X	X	1
0	0	0	X	No Chg
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

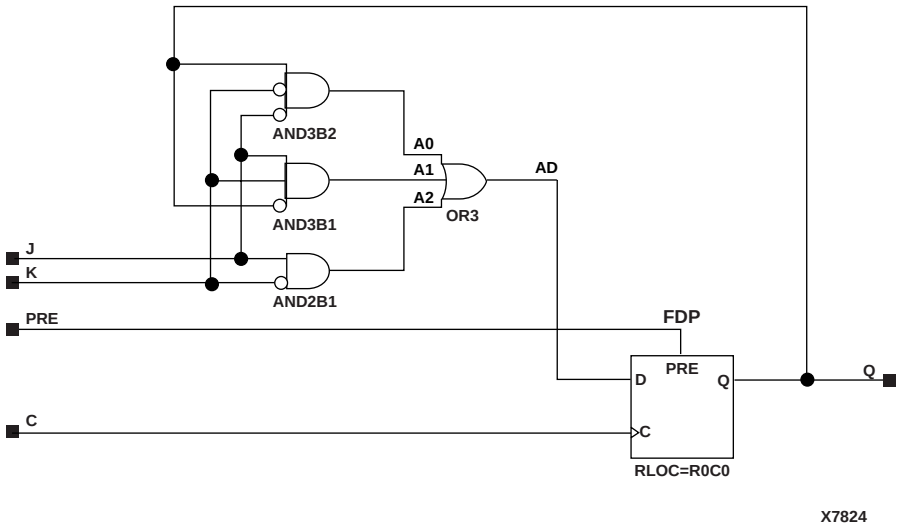


Figure 5-35 FJKP Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

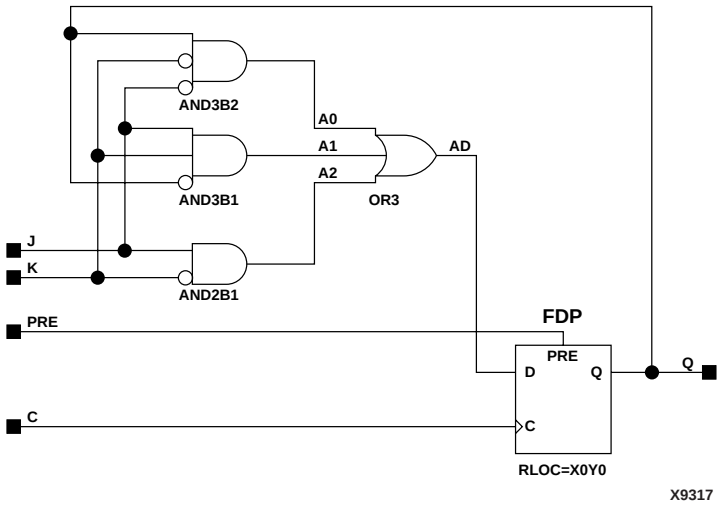


Figure 5-36 FJKP Implementation Virtex-II, Virtex-II PRO

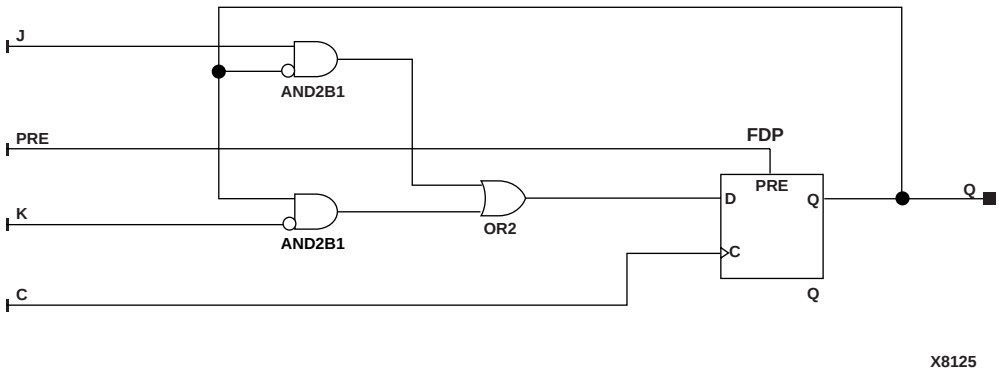
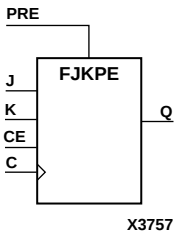


Figure 5-37 FJKP Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FJKPE

J-K Flip-Flop with Clock Enable and Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FJKPE is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the Q output High. When PRE is Low and CE is High, the Q output responds to the state of the J and K inputs, as shown in the truth table, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

The GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
PRE	CE	J	K	C	Q
1	X	X	X	X	1
0	0	X	X	X	No Chg
0	1	0	0	X	No Chg
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

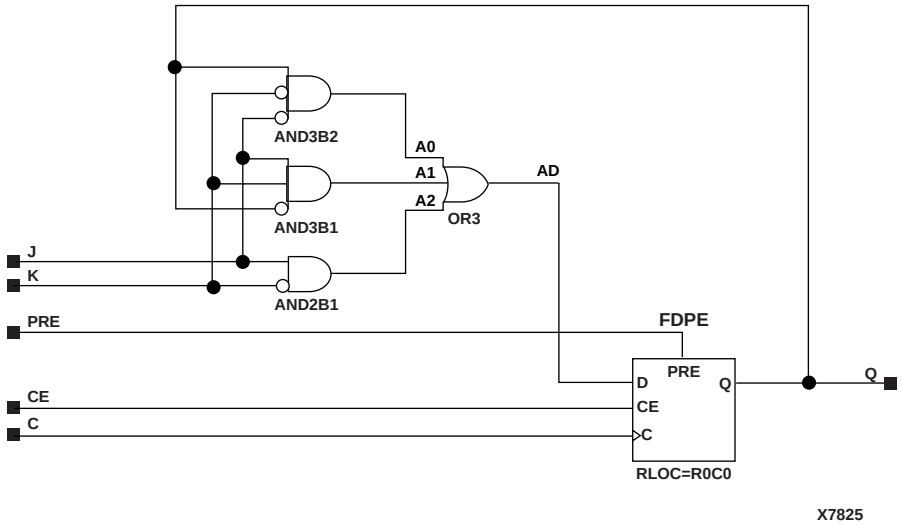


Figure 5-38 FJKPE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

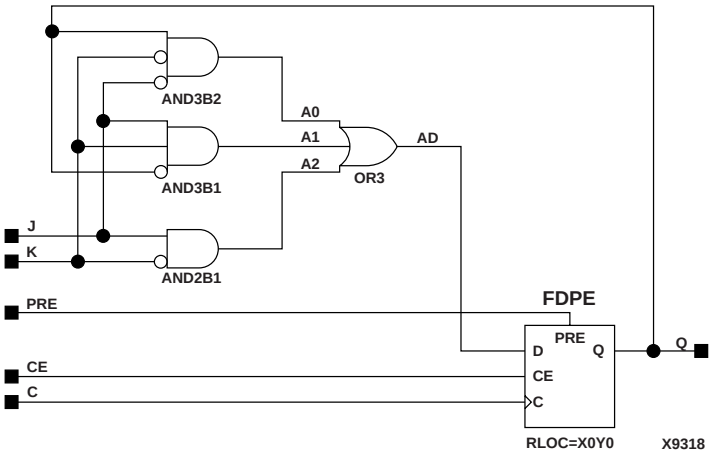


Figure 5-39 FJKPE Implementation Virtex-II, Virtex-II PRO

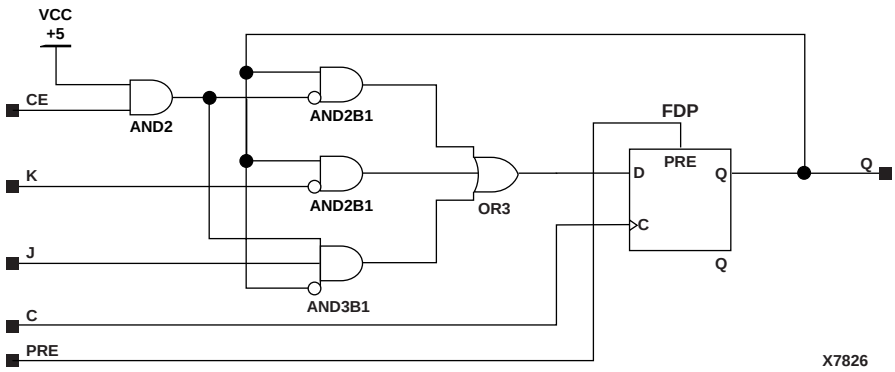
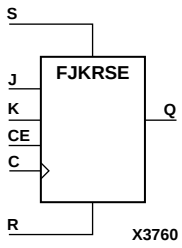


Figure 5-40 FJKPE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FJKRSE

J-K Flip-Flop with Clock Enable and Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FJKRSE is a single J-K-type flip-flop with J, K, synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). When synchronous reset (R) is High, all other inputs are ignored and output Q is reset Low. (Reset has precedence over Set.) When synchronous set (S) is High and R is Low, output Q is set High. When R and S are Low and CE is High, output Q responds to the state of the J and K inputs, according to the following truth table, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs						Outputs
R	S	CE	J	K	C	Q
1	X	X	X	X	↑	0
0	1	X	X	X	↑	1
0	0	0	X	X	X	No Chg
0	0	1	0	0	X	No Chg
0	0	1	0	1	↑	0
0	0	1	1	1	↑	Toggle
0	0	1	1	0	↑	1

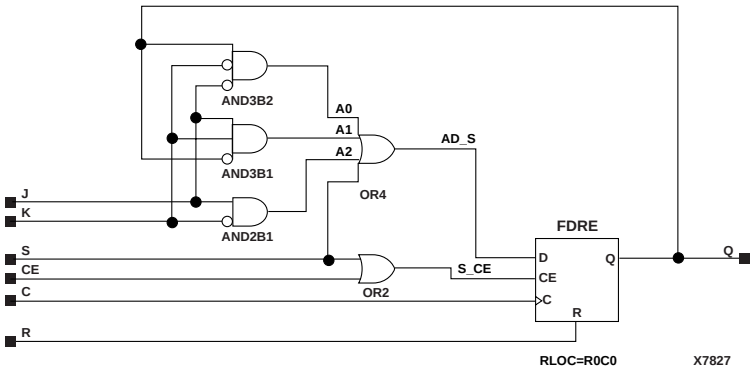


Figure 5-41 FJKRSE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

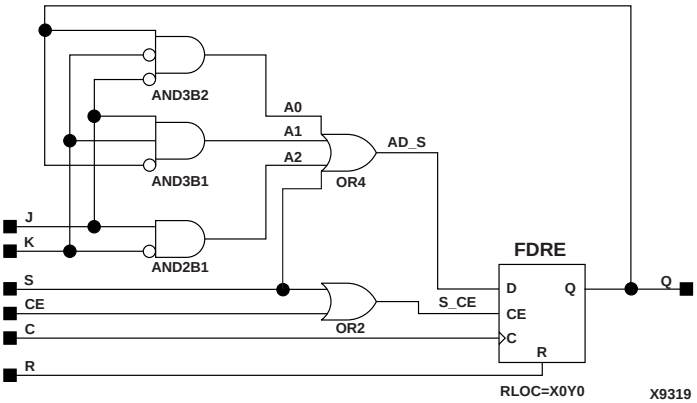


Figure 5-42 FJKRSE Implementation Virtex-II, Virtex-II PRO

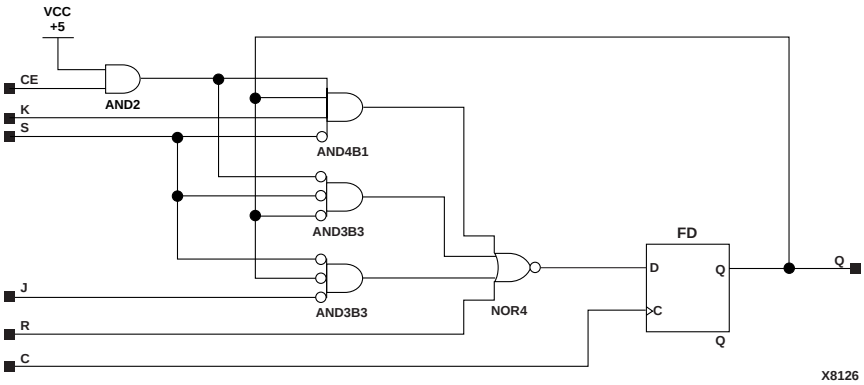
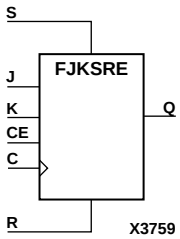


Figure 5-43 FJKRSE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FJKSRE

J-K Flip-Flop with Clock Enable and Synchronous Set and Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FJKSRE is a single J-K-type flip-flop with J, K, synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High, all other inputs are ignored and output Q is set High. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low. When S and R are Low and CE is High, output Q responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs						Outputs
S	R	CE	J	K	C	Q
1	X	X	X	X	↑	1
0	1	X	X	X	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	0	X	No Chg
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

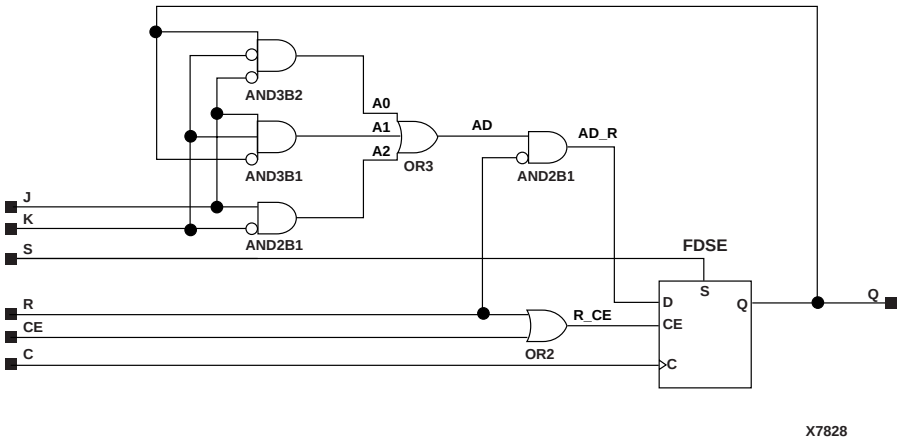


Figure 5-44 FJKSRE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

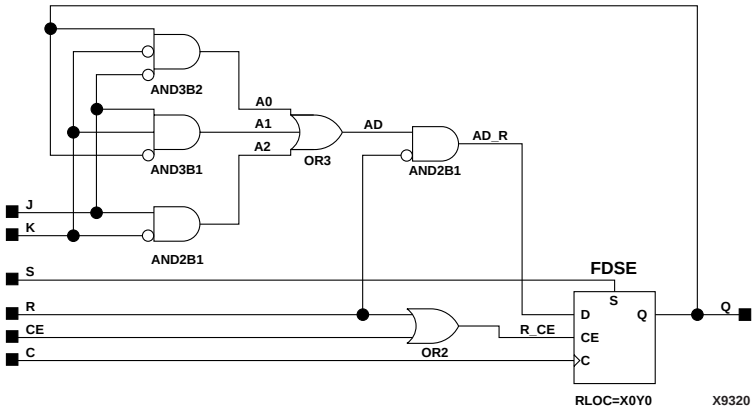


Figure 5-45 FJKSRE Implementation Virtex-II, Virtex-II PRO

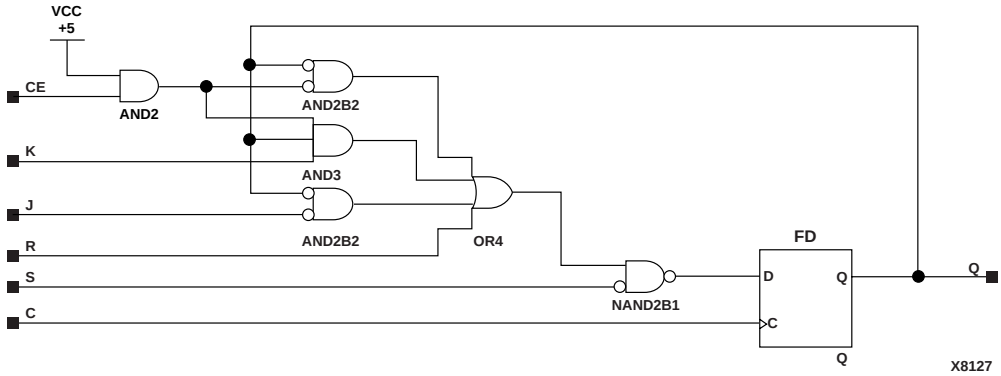
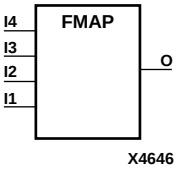


Figure 5-46 FJKSRE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FMAP

F Function Generator Partitioning Control Symbol

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



The FMAP symbol is used to map logic to the function generator of a slice. See the appropriate CAE tool interface user guide for information about specifying this attribute in your schematic design editor.

The MAP=*type* parameter can be used with the FMAP symbol to further define how much latitude you want to give the mapping program. The following table shows MAP option characters and their meanings.

MAP Option Character	Function
P	Pins.
C	Closed — Adding logic to or removing logic from the CLB is not allowed.
L	Locked — Locking CLB pins.
O	Open — Adding logic to or removing logic from the CLB is allowed.
U	Unlocked — No locking on CLB pins.

Possible types of MAP parameters for FMAP are MAP=PUC, MAP=PLC, MAP=PLO, and MAP=PUO. The default parameter is PUO. If one of the “open” parameters is used (PLO or PUO), only the output signals must be specified.

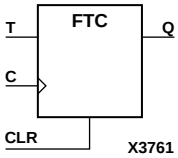
Note Currently, only PUC and PUO are observed. PLC and PLO are translated into PUC and PUO, respectively.

The FMAP symbol can be assigned to specific CLB locations using LOC attributes. See the “LOC” section of the *Constraints Guide* and to the appropriate CAE tool interface user guide for more information on assigning LOC attributes.

FTC

Toggle Flip-Flop with Toggle Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTC is a synchronous, resettable toggle flip-flop. The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the data output (Q) Low. The Q output toggles, or changes state, when the toggle enable (T) input is High and CLR is Low during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CLR	T	C	Q
1	X	X	0
0	0	X	No Chg
0	1	↑	Toggle

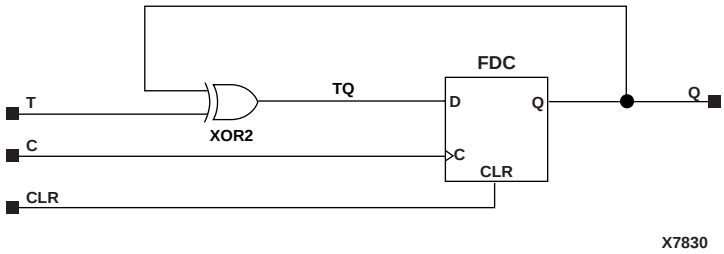


Figure 5-47 FTC Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

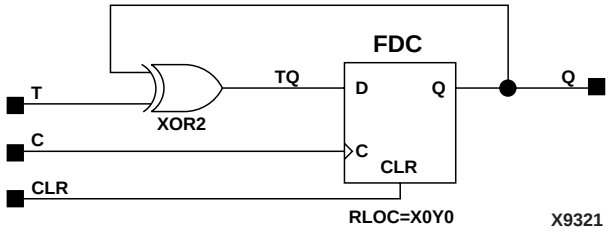


Figure 5-48 FTC Implementation Virtex-II, Virtex-II PRO

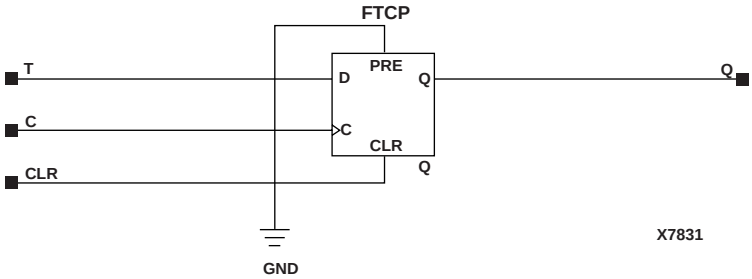
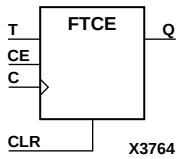


Figure 5-49 FTC Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTCE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTCE is a toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
CLR	CE	T	C	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	0	X	No Chg
0	1	1	↑	Toggle

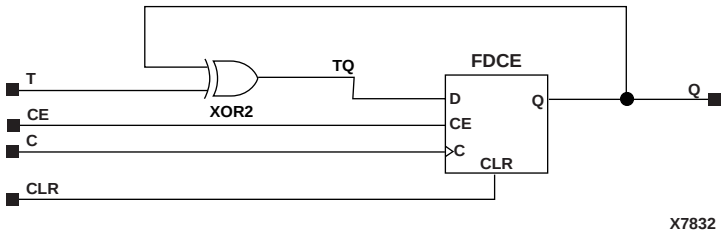


Figure 5-50 FTCE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

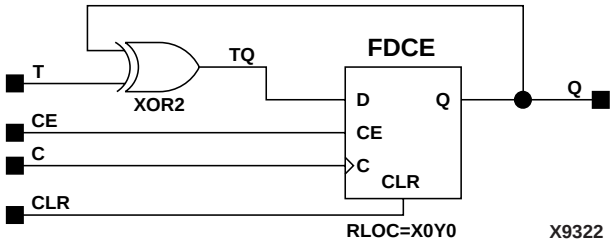


Figure 5-51 FTCE Implementation Virtex-II, Virtex-II PRO

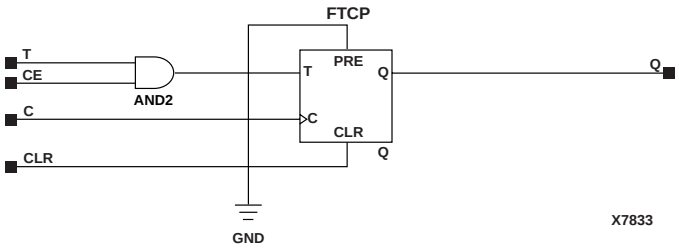
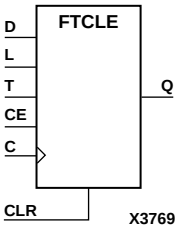


Figure 5-52 FTCE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTCLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTCLE is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs						Outputs
CLR	L	CE	T	D	C	Q
1	X	X	X	X	X	0
0	1	X	X	1	↑	1
0	1	X	X	0	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle

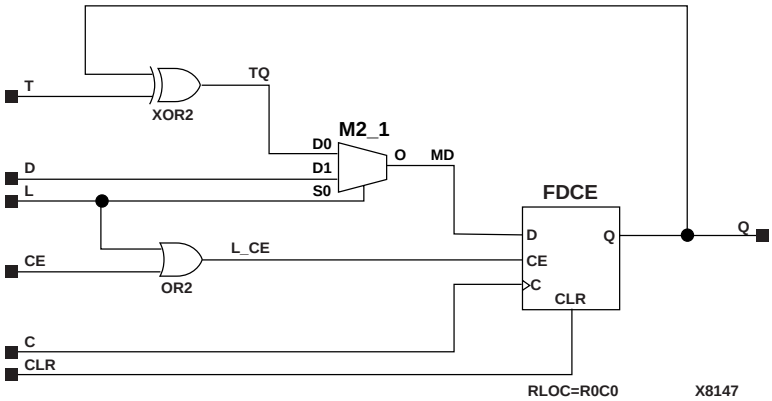


Figure 5-53 FTCLE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

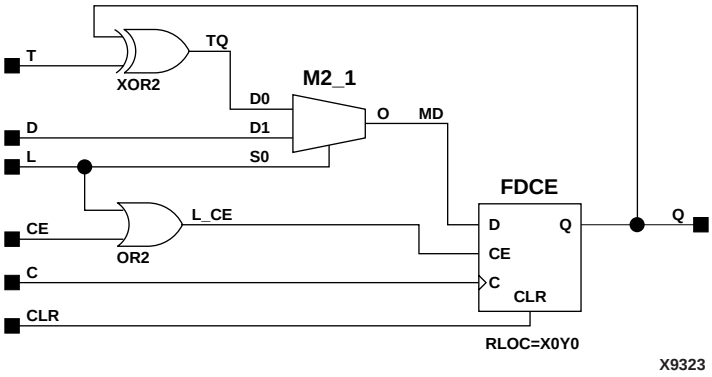


Figure 5-54 FTCLE Implementation Virtex-II, Virtex-II PRO

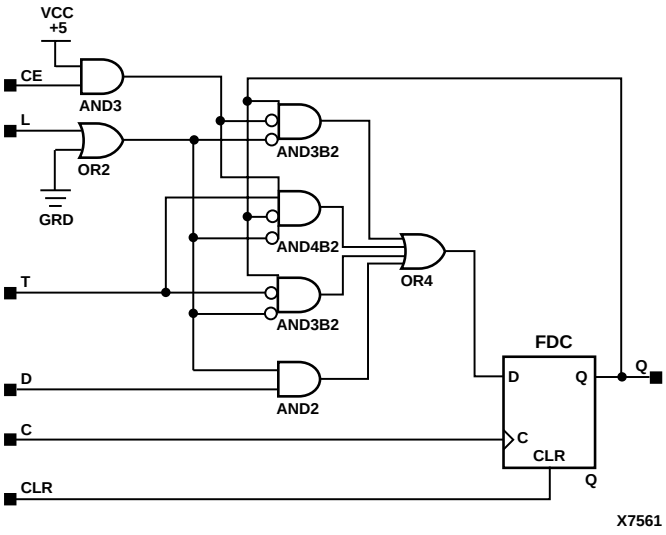
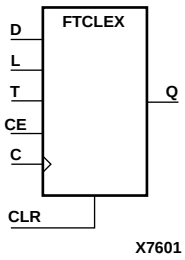


Figure 5-55 FTCLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTCLEX

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



FTCLEX is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs						Outputs
CLR	L	CE	T	D	C	Q
1	X	X	X	X	X	0
0	1	1	X	1	↑	1
0	1	1	X	0	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle

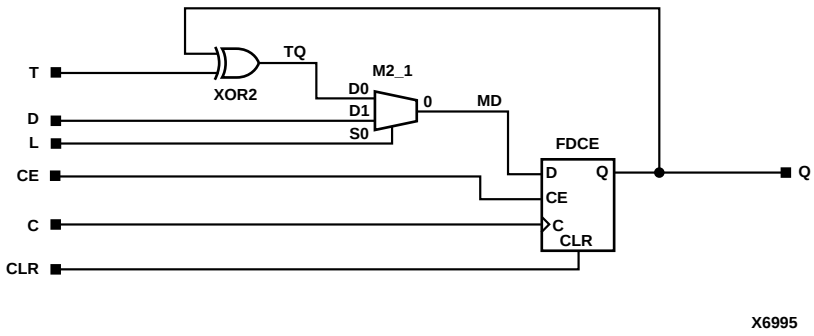


Figure 5-56 FTCLEX Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

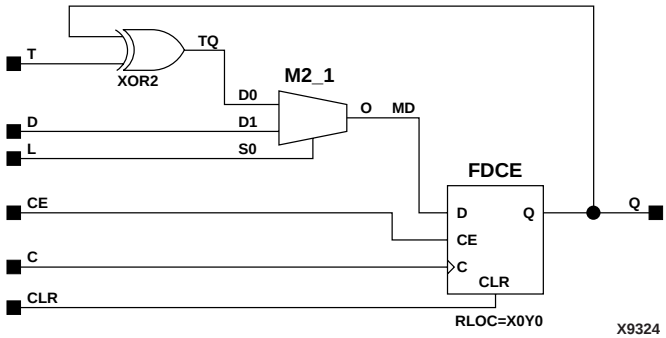
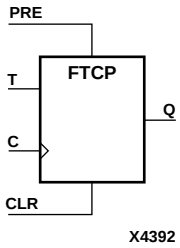


Figure 5-57 FTCLEX Implementation Virtex-II, Virtex-II PRO

FTCP

Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Primitive	Primitive	Primitive



FTCP is a toggle flip-flop with toggle enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) input is High, all other inputs are ignored and Q is set High. When the toggle enable input (T) is High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition.

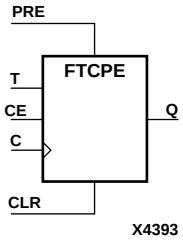
The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
CLR	PRE	T	C	Q
1	0	X	X	0
0	1	X	X	1
0	0	0	X	No Chg
0	0	1	↑	Toggle

FTCPE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro



FTCPE is a toggle flip-flop with toggle and clock enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) input is High, all other inputs are ignored and Q is set High. When the toggle enable input (T) and the clock enable input (CE) are High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. Clock transitions are ignored when CE is Low.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
CLR	PRE	CE	T	C	Q
1	0	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	X	No Chg
0	0	1	1	↑	Toggle

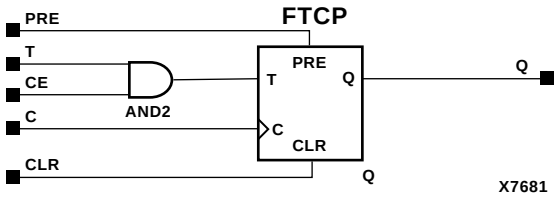
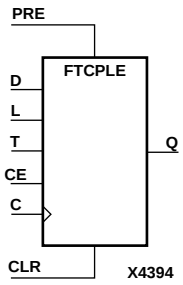


Figure 5-58 FTCPE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTCPLE

Loadable Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro



FTCPLE is a loadable toggle flip-flop with toggle and clock enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) input is High, all other inputs are ignored and Q is set High. The load input (L) loads the data on input D into the flip-flop on the Low-to-High clock transition, regardless of the state of the clock enable (CE). When the toggle enable input (T) and the clock enable input (CE) are High and CLR, PRE, and L are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. Clock transitions are ignored when CE is Low.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs							Outputs
CLR	PRE	L	CE	T	C	D	Q
1	X	X	X	X	X	X	0
0	1	X	X	X	X	X	1
0	0	1	X	X	↑	0	0
0	0	1	X	X	↑	1	1
0	0	0	0	X	X	X	No Chg
0	0	0	1	0	X	X	No Chg
0	0	0	1	1	↑	X	Toggle

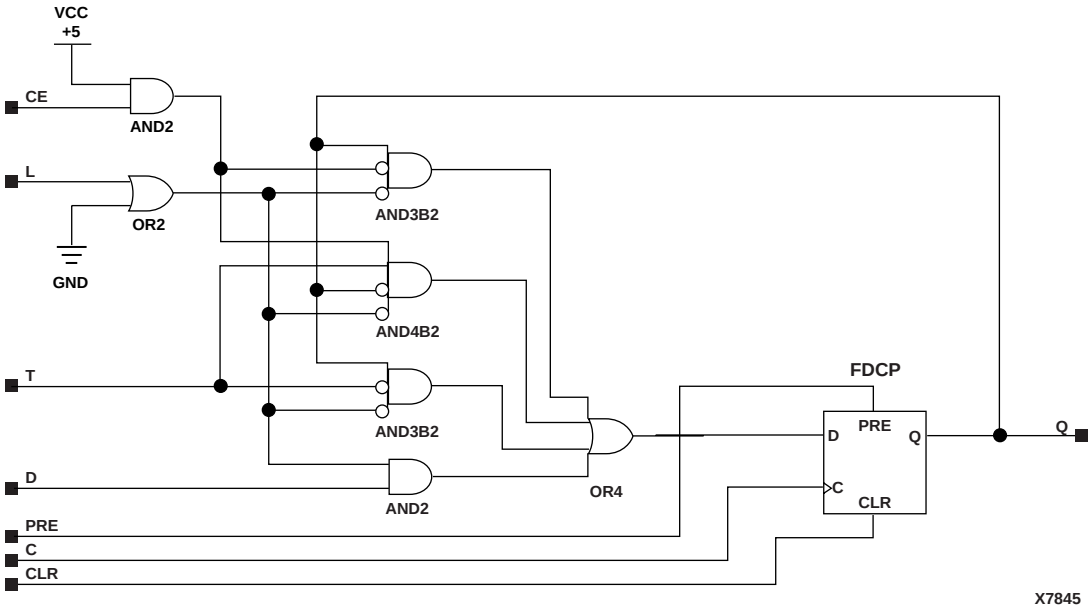
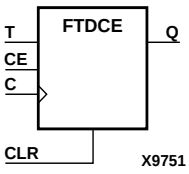


Figure 5-59 FTCPLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTDCE

Dual Edge Triggered Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro



FTDCE is a dual edge triggered toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
CLR	CE	T	C	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	0	X	No Chg
0	1	1	↑	Toggle
0	1	1	↓	Toggle

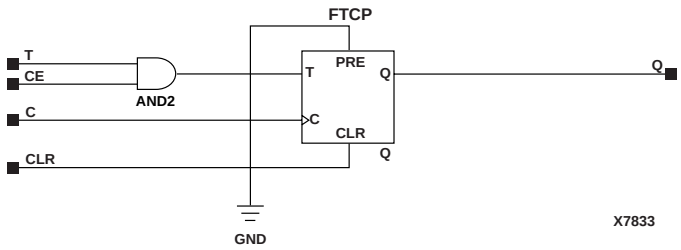
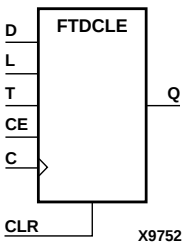


Figure 5-60 FTDCE Implementation CoolRunner-II

FTDCLE

Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FTDCLE is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs
CLR	L	CE	T	D	C	Q
1	X	X	X	X	X	0
0	1	X	X	1	↑	1
0	1	X	X	1	↓	1
0	1	X	X	0	↑	0
0	1	X	X	0	↓	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle
0	0	1	1	X	↓	Toggle

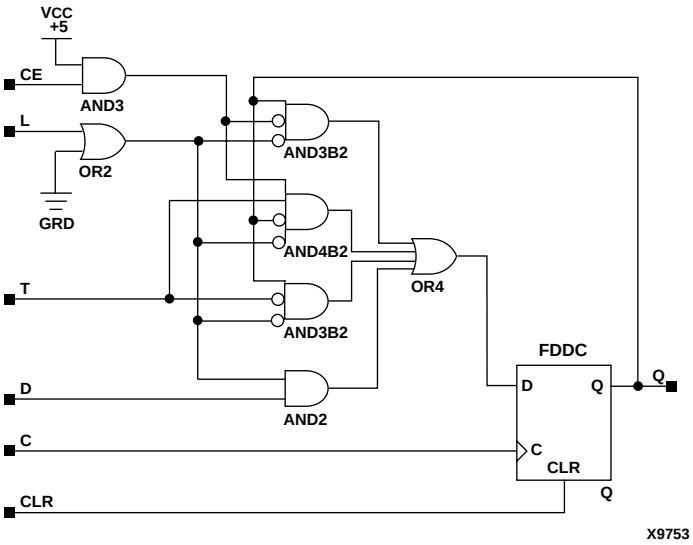
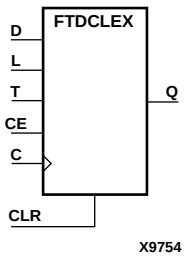


Figure 5-61 FTDCLE Implementation CoolRunner-II

FTDCLEX

Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FTDCLEX is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

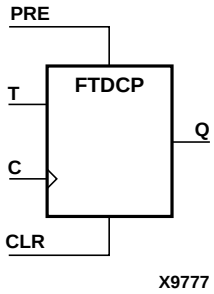
The flip-flop is asynchronously cleared, output Low, when power is applied.

Inputs						Outputs
CLR	L	CE	T	D	C	Q
1	X	X	X	X	X	0
0	1	1	X	1	↑	1
0	1	1	X	1	↓	1
0	1	1	X	0	↑	0
0	1	1	X	0	↓	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle
0	0	1	1	X	↓	Toggle

FTDCP

Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Primitive	Primitive	Primitive



FTDCP is a toggle flip-flop with toggle enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) input is High, all other inputs are ignored and Q is set High. When the toggle enable input (T) is High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
CLR	PRE	T	C	Q
1	0	X	X	0
0	1	X	X	1
0	0	0	X	No Chg
0	0	1	↑	Toggle
0	0	1	↓	Toggle

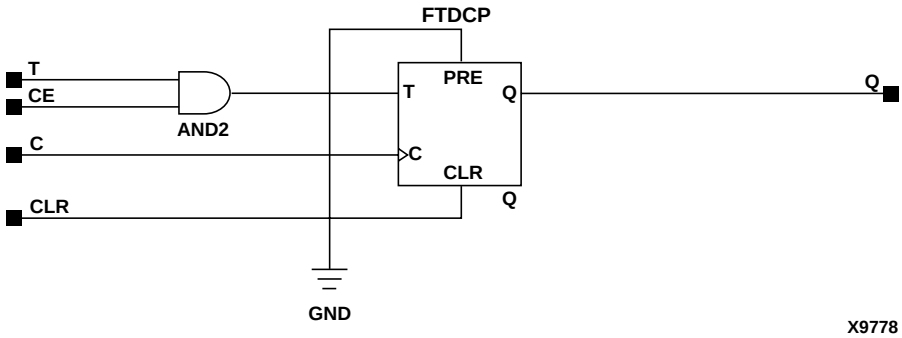
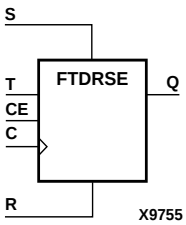


Figure 5-62 FTDCP Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTDRSE

Dual Edge Triggered Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FTDRSE is a dual edge triggered toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is High and R is Low, clock enable input (CE) is overridden and output Q is set High. (Reset has precedence over Set.) When toggle enable input (T) and CE are High and R and S are Low, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock transitions.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
R	S	CE	T	C	Q
1	X	X	X	↑	0
1	X	X	X	↓	0
0	1	X	X	↑	1
0	1	X	X	↓	1
0	0	0	X	X	No Chg
0	0	1	0	X	No Chg
0	0	1	1	↑	Toggle
0	0	1	1	↓	Toggle

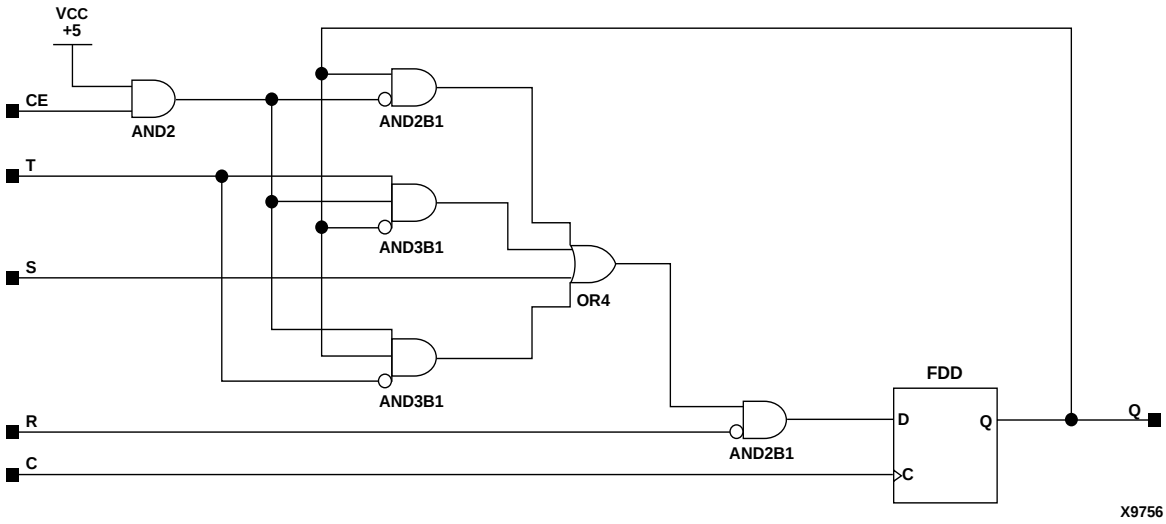
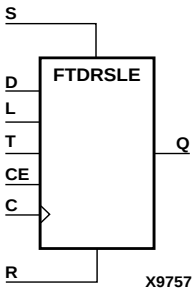


Figure 5-63 FTDRSE Implementation CoolRunner-II

FTDRSLE

Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro



FTDRSLE is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock transitions. When R, S, and L are Low and CE is High, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs							Outputs
R	S	L	CE	T	D	C	Q
1	0	X	X	X	X	↑	0
1	0	X	X	X	X	↓	0
0	1	X	X	X	X	↑	1
0	1	X	X	X	X	↓	1
0	0	1	X	X	1	↑	1
0	0	1	X	X	1	↓	1
0	0	1	X	X	0	↑	0
0	0	1	X	X	0	↓	0
0	0	0	0	X	X	X	No Chg
0	0	0	1	0	X	X	No Chg
0	0	0	1	1	X	↑	Toggle
0	0	0	1	1	X	↓	Toggle

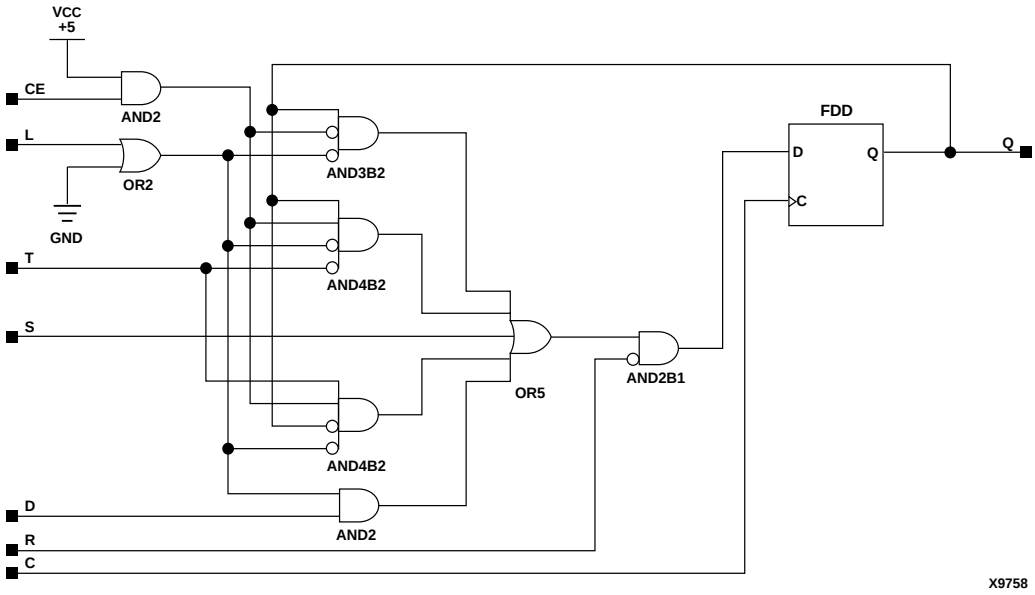
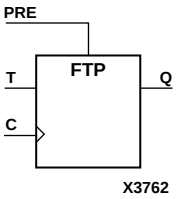


Figure 5-64 FTDRSLE Implementation CoolRunner-II

FTP

Toggle Flip-Flop with Toggle Enable and Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTP is a toggle flip-flop with toggle enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output Q is set High. When toggle-enable input (T) is High and PRE is Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset to output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

The GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, or the STARTUP_VIRTEX symbol.

Inputs			Outputs
PRE	T	C	Q
1	X	X	1
0	0	X	No Chg
0	1	↑	Toggle

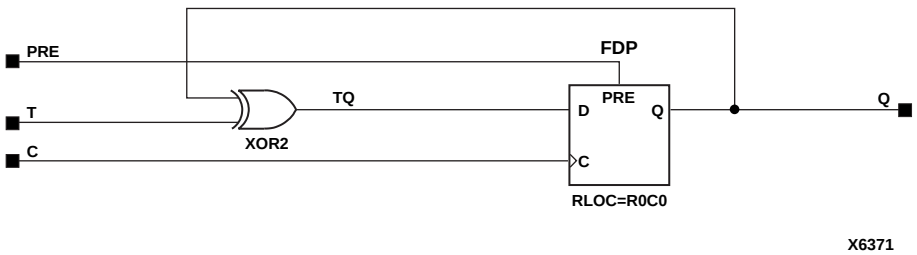


Figure 5-65 FTP Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

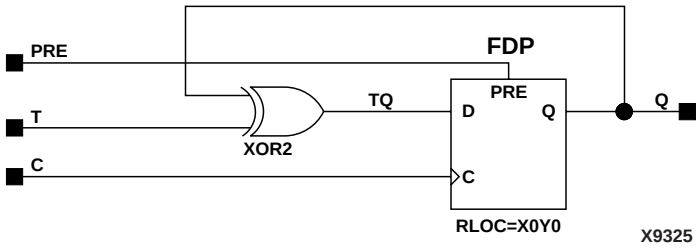


Figure 5-66 FTP Implementation Virtex-II, Virtex-II PRO

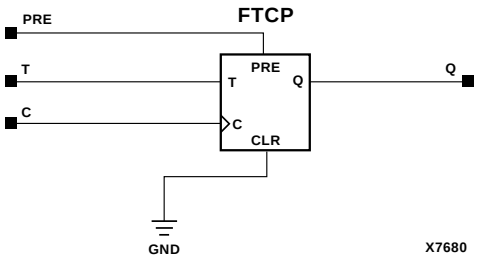
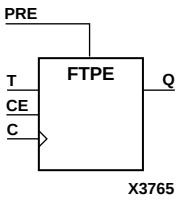


Figure 5-67 FTP Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTPE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTPE is a toggle flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output Q is set High. When the toggle enable input (T) is High, clock enable (CE) is High, and PRE is Low, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset to output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

The GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
PRE	CE	T	C	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	0	X	No Chg
0	1	1	↑	Toggle

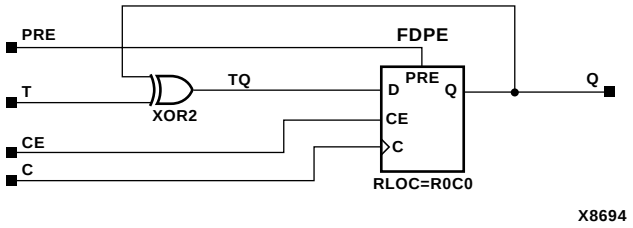


Figure 5-68 FTPE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

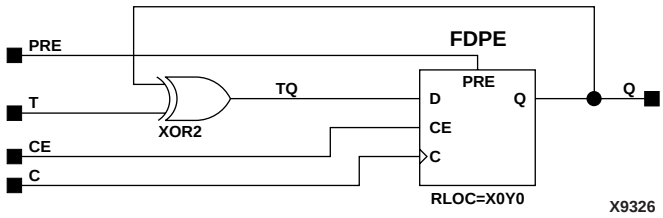


Figure 5-69 FTPE Implementation Virtex-II, Virtex-II PRO

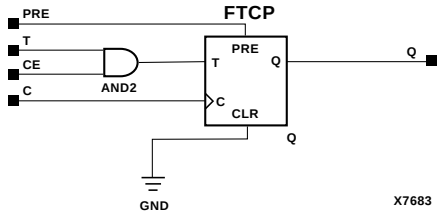
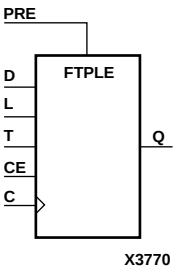


Figure 5-70 FTPE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTPLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTPLE is a toggle/loadable flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset input (PRE) is High, all other inputs are ignored and output Q is set High. When the load enable input (L) is High and PRE is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and CE are High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously preset to output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

The GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs						Outputs
PRE	L	CE	T	D	C	Q
1	X	X	X	X	X	1
0	1	X	X	1	↑	1
0	1	X	X	0	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle

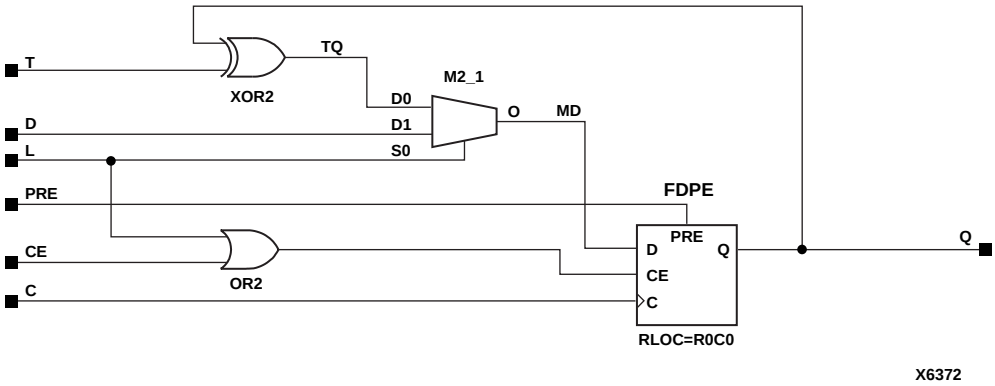


Figure 5-71 FTPLE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

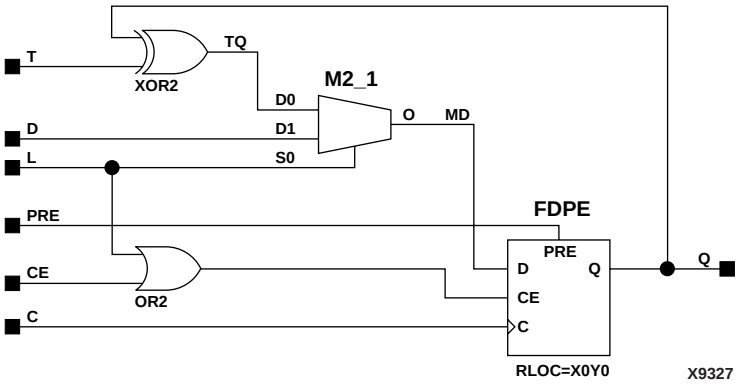


Figure 5-72 FTPLE Implementation Virtex-II, Virtex-II PRO

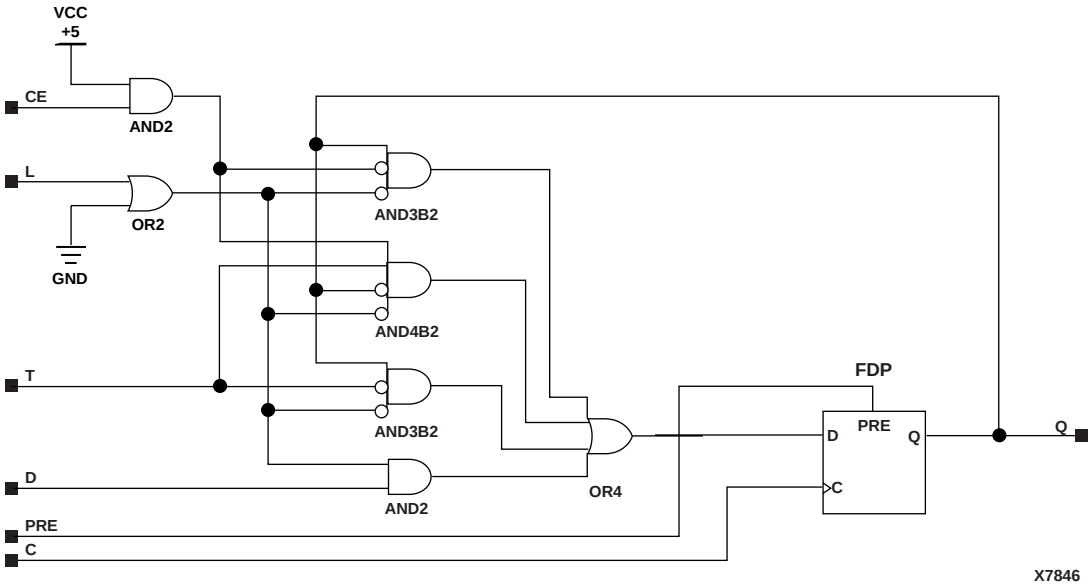
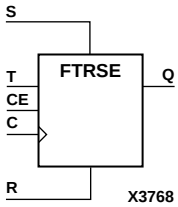


Figure 5-73 FTPLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTRSE

Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTRSE is a toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is High and R is Low, clock enable input (CE) is overridden and output Q is set High. (Reset has precedence over Set.) When toggle enable input (T) and CE are High and R and S are Low, output Q toggles, or changes state, during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs
R	S	CE	T	C	Q
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Chg
0	0	1	0	X	No Chg
0	0	1	1	↑	Toggle

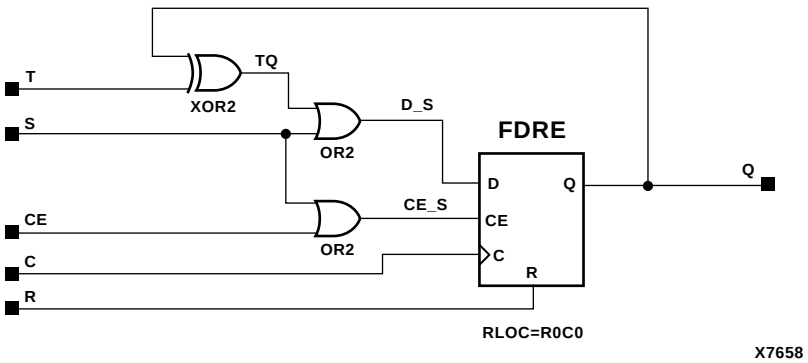


Figure 5-74 FTRSE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

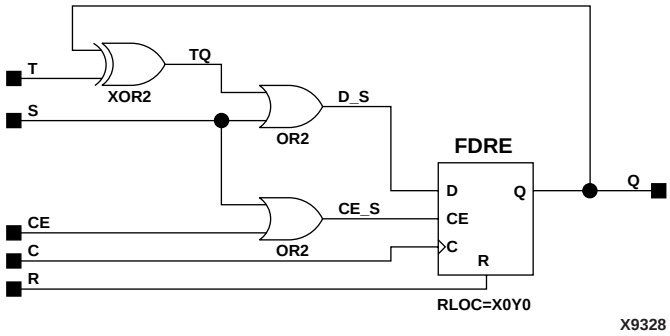


Figure 5-75 FTRSE Implementation Virtex-II, Virtex-II PRO

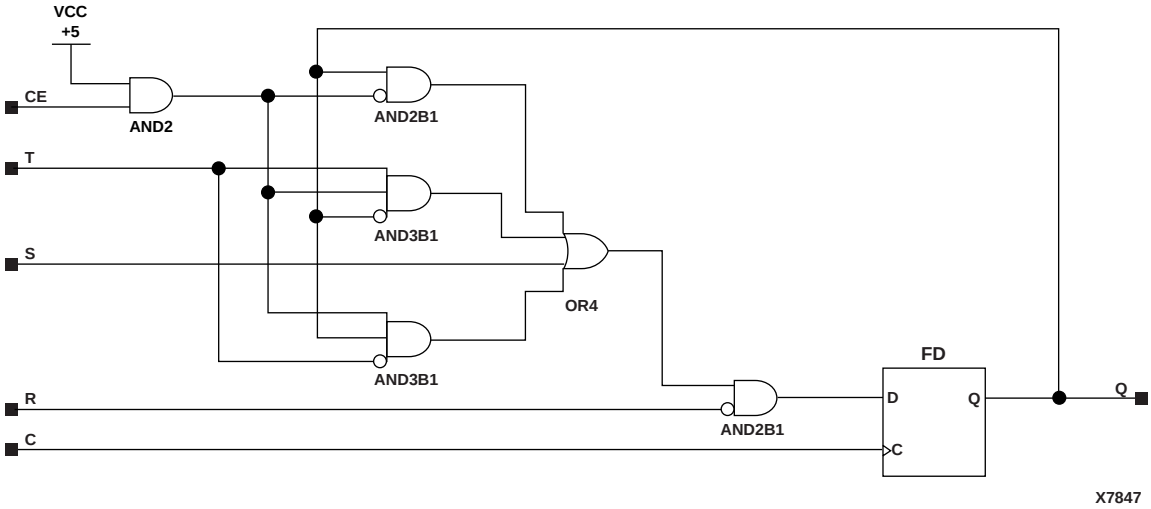
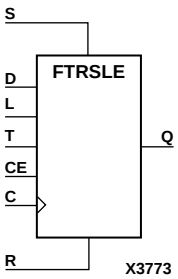


Figure 5-76 FTRSE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTRSLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTRSLE is a toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When R, S, and L are Low and CE is High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs							Outputs
R	S	L	CE	T	D	C	Q
1	0	X	X	X	X	↑	0
0	1	X	X	X	X	↑	1
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Chg
0	0	0	1	0	X	X	No Chg
0	0	0	1	1	X	↑	Toggle

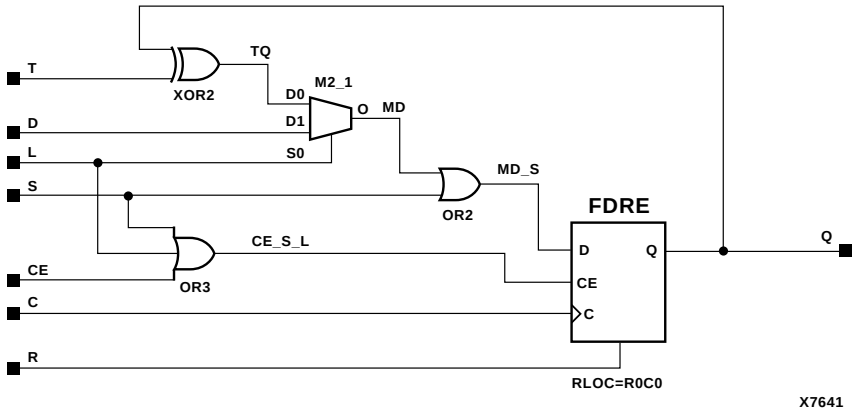


Figure 5-77 FTRSLE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

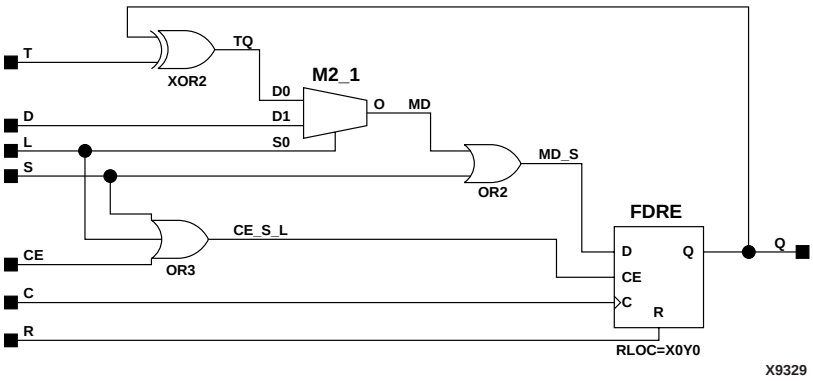


Figure 5-78 FTRSLE Implementation Virtex-II, Virtex-II PRO

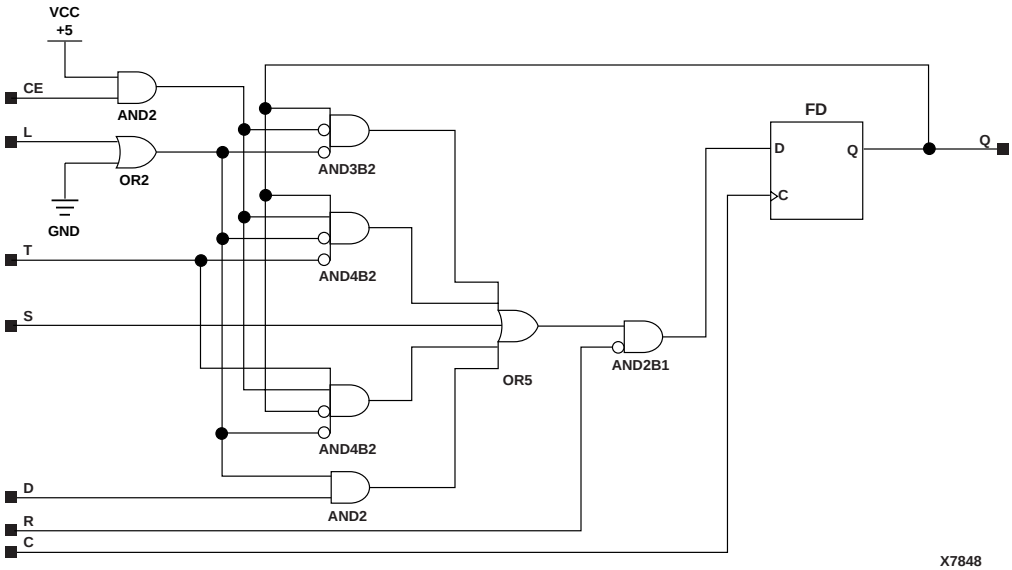
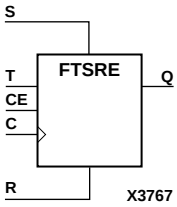


Figure 5-79 FTRSLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTSRE

Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTSRE is a toggle flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input, when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset input (R) is High and S is Low, clock enable input (CE) is overridden and output Q is reset Low. When toggle enable input (T) and CE are High and S and R are Low, output Q toggles, or changes state, during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs					Outputs
S	R	CE	T	C	Q
1	X	X	X	↑	1
0	1	X	X	↑	0
0	0	0	X	X	No Chg
0	0	1	0	X	No Chg
0	0	1	1	↑	Toggle

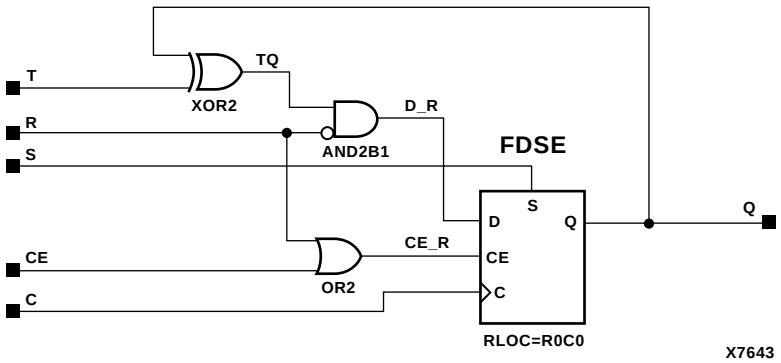


Figure 5-80 FTSRE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

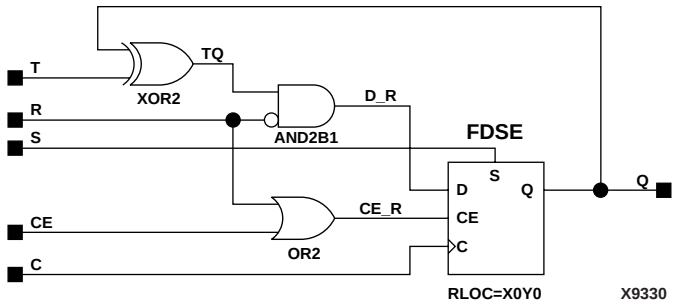


Figure 5-81 FTSRE Implementation Virtex-II, Virtex-II PRO

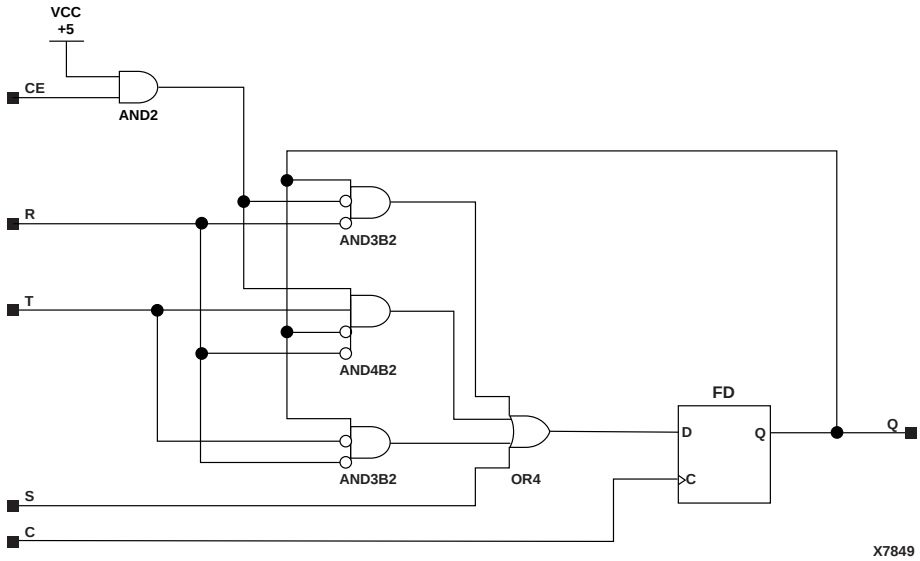
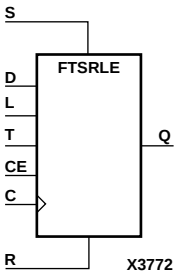


Figure 5-82 FTSRE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

FTSRLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



FTSRLE is a toggle/loadable flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input (S), when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, clock enable input (CE) is overridden and output Q is reset Low. When load enable input (L) is High and S and R are Low, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When the toggle enable input (T) and CE are High and S, R, and L are Low, output Q toggles, or changes state, during the Low-to- High clock transition. When CE is Low, clock transitions are ignored.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the flip-flop is asynchronously preset when a High-level pulse is applied on the PRLD global net.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, the flip-flop is asynchronously cleared, output Low, when global set/reset (GSR) is active.

The GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs							Outputs
S	R	L	CE	T	D	C	Q
1	0	X	X	X	X	↑	1
0	1	X	X	X	X	↑	0
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Chg
0	0	0	1	0	X	X	No Chg
0	0	0	1	1	X	↑	Toggle

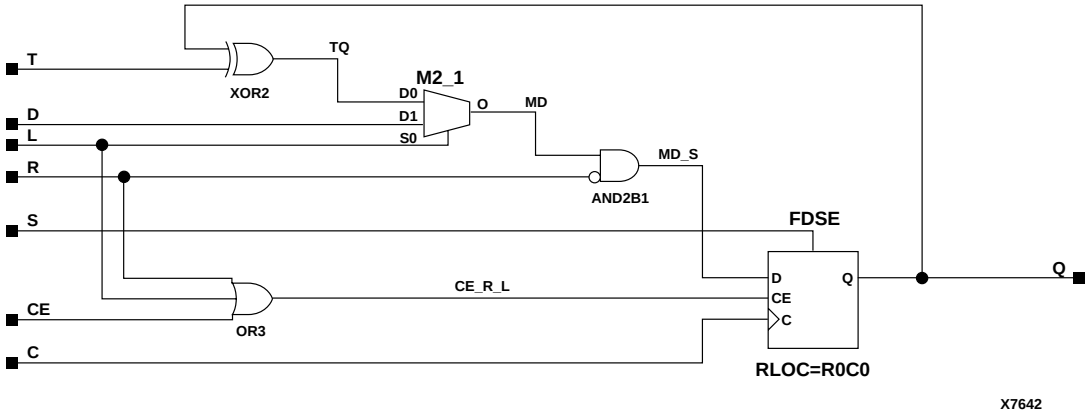


Figure 5-83 FTSRLE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

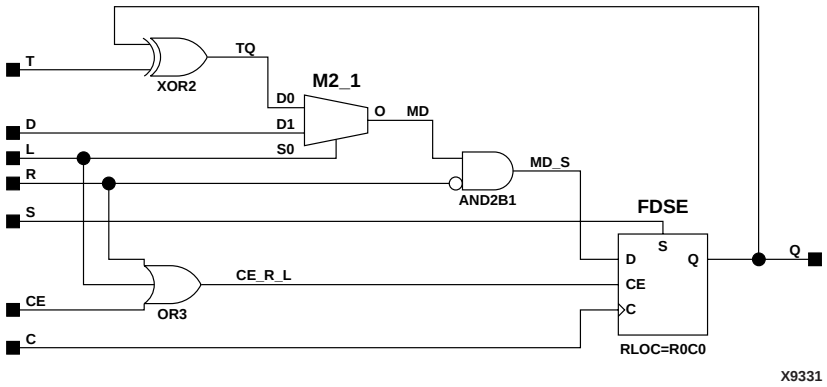


Figure 5-84 FTSRLE Implementation Virtex-II, Virtex-II PRO

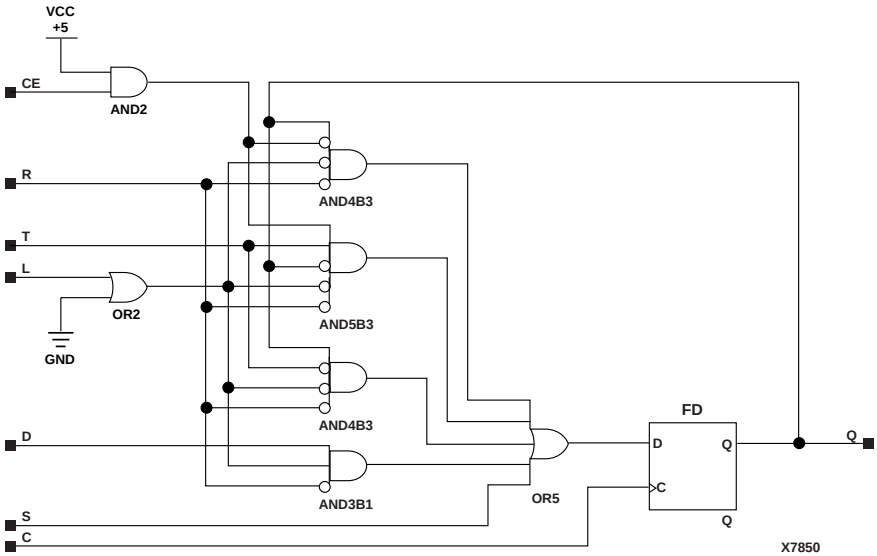


Figure 5-85 FTSRLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

Chapter 6

GND to KEEPER

GND

Ground-Connection Signal Tag

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

X3858

The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

GT_AURORA_*n*

Gigabit Transceiver for High-Speed I/O

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II PRO*	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

*Supported for Virtex-II PRO but not for Virtex-II

This Xilinx protocol gigabit transceiver supports 1, 2, and 4-byte data paths. The letter *n* represents number of bytes of the data path. Valid values are 1, 2 or 4.

You can also set attributes for the primitives. See Table 1-8 of the *Rocket I/O Transceiver User Guide* for a description of these attributes. See Table 1-9 of the *Rocket I/O Transceiver User Guide* for the default attribute values.

The following table lists the input and output ports for all values of *n*. For a description of each of the ports, see Table 1-7 in the *Rocket I/O Transceiver User Guide.*

Inputs	Outputs
CHBONDI [3:0]	CHBONDDONE
CONFIGENABLE	CHBONDO [3:0]
CONFIGIN	CONFIGOUT
ENCHANSYNC	RXBUFSTATUS [1:0]
ENMCOMMAALIGN	RXCHARISCOMMA [0:0] (GT_AURORA_1) RXCHARISCOMMA [1:0] (GT_AURORA_2) RXCHARISCOMMA [3:0] (GT_AURORA_4)
ENPCOMMAALIGN	RXCHARISK [0:0] (GT_AURORA_1) RXCHARISK [1:0] (GT_AURORA_2) RXCHARISK [3:0] (GT_AURORA_4)
LOOPBACK [1:0]	RXCHECKINGCRC
POWERDOWN	RXCLKCORCNT [2:0]
REFCLK	RXCOMMADET
REFCLK2	RXCRCERR
REFCLKSEL	RXDATA [7:0] (GT_AURORA_1) RXDATA [15:0] (GT_AURORA_2) RXDATA [31:0] (GT_AURORA_4)
RXN	RXDISPERR [0:0] (GT_AURORA_1) RXDISPERR [1:0] (GT_AURORA_2) RXDISPERR [3:0] (GT_AURORA_4
RXP	RXLOSSOFSYNC [1:0]
RXPOLARITY	RXNOTINTABLE [0:0] (GT_AURORA_1) RXNOTINTABLE [1:0] (GT_AURORA_2) RXNOTINTABLE [3:0] (GT_AURORA_4)
RXRESET	RXREALIGN
RXUSRCLK	RXRECCLK

Inputs	Outputs
RXUSRCLK2	RXRUNDISP [0:0] (GT_AURORA_1) RXRUNDISP [1:0] (GT_AURORA_2) RXRUNDISP [3:0] (GT_AURORA_4)
TXBYPASS8B10B [0:0] (GT_AURORA_1) TXBYPASS8B10B [1:0] (GT_AURORA_2) TXBYPASS8B10B [3:0] (GT_AURORA_4)	TXBUFERR
TXCHARDISPMODE [0:0] (GT_AURORA_1) TXCHARDISPMODE [1:0] (GT_AURORA_2) TXCHARDISPMODE [3:0] (GT_AURORA_4)	TXKERR [0:0] (GT_AURORA_1) TXKERR [1:0] (GT_AURORA_2) TXKERR [3:0] (GT_AURORA_4)
TXCHARDISPVAL [0:0] (GT_AURORA_1) TXCHARDISPVAL [1:0] (GT_AURORA_2) TXCHARDISPVAL [3:0] (GT_AURORA_4)	TXN
TXCHARISK [0:0] (GT_AURORA_1) TXCHARISK [1:0] (GT_AURORA_2) TXCHARISK [3:0] (GT_AURORA_4)	TXP
TXDATA [7:0] (GT_AURORA_1) TXDATA [15:0](GT_AURORA_2) TXDATA [31:0](GT_AURORA_4)	TXRUNDISP [0:0] (GT_AURORA_1) TXRUNDISP [1:0] (GT_AURORA_2) TXRUNDISP [3:0] (GT_AURORA_4)
TXFORCECRCERR	
TXINHIBIT	
TXPOLARITY	
TXRESET	
TXUSRCLK	
TXUSRCLK2	

GT_CUSTOM

Gigabit Transceiver for High-Speed I/O

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II PRO*	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

*Supported for Virtex-II PRO but not for Virtex-II

This gigabit transceiver is fully customizable. You can set attributes for the primitives. See Table 1-8 of the *Rocket I/O Transceiver User Guide* for a description of these attributes. See Table 1-9 of the *Rocket I/O Transceiver User Guide* for the default attribute values.

The following table lists the input and output ports. For a description of each of the ports, see Table 1-7 in the *Rocket I/O Transceiver User Guide*.

Inputs	Outputs
CHBONDI [3:0]	CHBONDDONE
CONFIGENABLE	CHBONDO [3:0]
CONFIGIN	CONFIGOUT
ENCHANSYNC	RXBUFSTATUS [1:0]
ENMCOMMAALIGN	RXCHARISCOMMA [3:0]
ENPCOMMAALIGN	RXCHARISK [3:0]
LOOPBACK [1:0]	RXCHECKINGCRC
POWERDOWN	RXCLKCORCNT [2:0]
REFCLK	RXCOMMADET
REFCLK2	RXCRCERR
REFCLKSEL	RXDATA [31:0]
RXN	RXDISPERR [3:0]
RXP	RXLOSSOFSYNC [1:0]
RXPOLARITY	RXNOTINTABLE [3:0]
RXRESET	RXREALIGN
RXUSRCLK	RXRECCLK
RXUSRCLK2	RXRUNDISP [3:0]
TXBYPASS8B10B [3:0]	TXBUFERR
TXCHARDISPMODE [3:0]	TXKERR [3:0]
TXCHARDISPVAL [3:0]	TXN
TXCHARISK [3:0]	TXP
TXDATA [31:0]	TXRUNDISP [3:0]
TXFORCECRCERR	
TXINHIBIT	
TXPOLARITY	

Inputs	Outputs
TXRESET	
TXUSRCLK	
TXUSRCLK2	

GT_ETHERNET_*n*

Gigabit Transceiver for High-Speed I/O

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II PRO*	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

*Supported for Virtex-II PRO but not for Virtex-II

This Ethernet gigabit transceiver supports 1, 2, and 4-byte data paths. The letter *n* represents number of bytes of the data path. Valid values are 1, 2 or 4.

You can also set attributes for the primitives. See Table 1-8 of the *Rocket I/O Transceiver User Guide* for a description of these attributes. See Table 1-9 of the *Rocket I/O Transceiver User Guide* for the default attribute values.

The following table lists the input and output ports for all values of *n*. For a description of each of the ports, see Table 1-7 in the *Rocket I/O Transceiver User Guide.*

Inputs	Outputs
CONFIGENABLE	CONFIGOUT
CONFIGIN	RXBUFSTATUS [1:0]
ENMCOMMAALIGN	RXCHARISCOMMA [0:0] (GT_ETHERNET_1) RXCHARISCOMMA [1:0] (GT_ETHERNET_2) RXCHARISCOMMA [3:0] (GT_ETHERNET_4)
ENPCOMMAALIGN	RXCHARISK [0:0] (GT_ETHERNET_1) RXCHARISK [1:0] (GT_ETHERNET_2) RXCHARISK [3:0] (GT_ETHERNET_4)
LOOPBACK [1:0]	RXCHECKINGCRC
POWERDOWN	RXCLKCORCNT [2:0]
REFCLK	RXCOMMADET
REFCLK2	RXCRCERR
REFCLKSEL	RXDATA [7:0] (GT_ETHERNET_1) RXDATA [15:0] (GT_ETHERNET_2) RXDATA [31:0] (GT_ETHERNET_4)
RXN	RXDISPERR [0:0] (GT_ETHERNET_1) RXDISPERR [1:0] (GT_ETHERNET_2) RXDISPERR [3:0] (GT_ETHERNET_4
RXP	RXLOSSOFSYNC [1:0]
RXPOLARITY	RXNOTINTABLE [0:0] (GT_ETHERNET_1) RXNOTINTABLE [1:0] (GT_ETHERNET_2) RXNOTINTABLE [3:0] (GT_ETHERNET_4)
RXRESET	RXREALIGN
RXUSRCLK	RXRECCLK

Inputs	Outputs
RXUSRCLK2	RXRUNDISP [0:0] (GT_ETHERNET_1) RXRUNDISP [1:0] (GT_ETHERNET_2) RXRUNDISP [3:0] (GT_ETHERNET_4)
TXBYPASS8B10B [0:0] (GT_ETHERNET_1) TXBYPASS8B10B [1:0] (GT_ETHERNET_2) TXBYPASS8B10B [3:0] (GT_ETHERNET_4)	TXBUFERR
TXCHARDISPMODE [0:0] (GT_ETHERNET_1) TXCHARDISPMODE [1:0] (GT_ETHERNET_2) TXCHARDISPMODE [3:0] (GT_ETHERNET_4)	TXKERR [0:0] (GT_ETHERNET_1) TXKERR [1:0] (GT_ETHERNET_2) TXKERR [3:0] (GT_ETHERNET_4)
TXCHARDISPVAL [0:0] (GT_ETHERNET_1) TXCHARDISPVAL [1:0] (GT_ETHERNET_2) TXCHARDISPVAL [3:0] (GT_ETHERNET_4)	TXN
TXCHARISK [0:0] (GT_ETHERNET_1) TXCHARISK [1:0] (GT_ETHERNET_2) TXCHARISK [3:0] (GT_ETHERNET_4)	TXP
TXDATA [7:0] (GT_ETHERNET_1) TXDATA [15:0] (GT_ETHERNET_2) TXDATA [31:0] (GT_ETHERNET_4)	TXRUNDISP [0:0] (GT_ETHERNET_1) TXRUNDISP [1:0] (GT_ETHERNET_2) TXRUNDISP [3:0] (GT_ETHERNET_4)
TXFORCECRCERR	
TXINHIBIT	
TXPOLARITY	
TXRESET	
TXUSRCLK	
TXUSRCLK2	

GT_FIBRE_CHAN_*n*

Gigabit Transceiver for High-Speed I/O

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II PRO*	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

*Supported for Virtex-II PRO but not for Virtex-II

This Fibre Channel gigabit transceiver supports 1, 2, and 4-byte data paths. The letter *n* represents number of bytes of the data path. Valid values are 1, 2 or 4.

You can also set attributes for the primitives. See Table 1-8 of the *Rocket I/O Transceiver User Guide* for a description of these attributes. See Table 1-10 of the *Rocket I/O Transceiver User Guide* for the default attribute values.

The following table lists the input and output ports for all values of *n*. For a description of each of the ports, see Table 1-7 in the *Rocket I/O Transceiver User Guide.*

Inputs	Outputs
CONFIGENABLE	CONFIGOUT
CONFIGIN	RXBUFSTATUS [1:0]
ENMCOMMAALIGN	RXCHARISCOMMA [0:0] (GT_FIBRE_CHAN_1) RXCHARISCOMMA [1:0] (GT_FIBRE_CHAN_2) RXCHARISCOMMA [3:0] (GT_FIBRE_CHAN_4)
ENPCOMMAALIGN	RXCHARISK [0:0] (GT_FIBRE_CHAN_1) RXCHARISK [1:0] (GT_FIBRE_CHAN_2) RXCHARISK [3:0] (GT_FIBRE_CHAN_4)
LOOPBACK [1:0]	RXCHECKINGCRC
POWERDOWN	RXCLKCORCNT [2:0]
REFCLK	RXCOMMADET
REFCLK2	RXCRCERR
REFCLKSEL	RXDATA [7:0] (GT_FIBRE_CHAN_1) RXDATA [15:0] (GT_FIBRE_CHAN_2) RXDATA [31:0] (GT_FIBRE_CHAN_4)
RXN	RXDISPERR [0:0] (GT_FIBRE_CHAN_1) RXDISPERR [1:0] (GT_FIBRE_CHAN_2) RXDISPERR [3:0] (GT_FIBRE_CHAN_4
RXP	RXLOSSOFSYNC [1:0]
RXPOLARITY	RXNOTINTABLE [0:0] (GT_FIBRE_CHAN_1) RXNOTINTABLE [1:0] (GT_FIBRE_CHAN_2) RXNOTINTABLE [3:0] (GT_FIBRE_CHAN_4)
RXRESET	RXREALIGN
RXUSRCLK	RXRECCLK
RXUSRCLK2	RXRUNDISP [0:0] (GT_FIBRE_CHAN_1) RXRUNDISP [1:0] (GT_FIBRE_CHAN_2) RXRUNDISP [3:0] (GT_FIBRE_CHAN_4)

Inputs	Outputs
TXBYPASS8B10B [0:0] (GT_FIBRE_CHAN_1) TXBYPASS8B10B [1:0] (GT_FIBRE_CHAN_2) TXBYPASS8B10B [3:0] (GT_FIBRE_CHAN_4)	TXBUFERR
TXCHARDISPMODE [0:0] (GT_FIBRE_CHAN_1) TXCHARDISPMODE [1:0] (GT_FIBRE_CHAN_2) TXCHARDISPMODE [3:0] (GT_FIBRE_CHAN_4)	TXKERR [0:0] (GT_FIBRE_CHAN_1) TXKERR [1:0] (GT_FIBRE_CHAN_2) TXKERR [3:0] (GT_FIBRE_CHAN_4)
TXCHARDISPVAL [0:0] (GT_FIBRE_CHAN_1) TXCHARDISPVAL [1:0] (GT_FIBRE_CHAN_2) TXCHARDISPVAL [3:0] (GT_FIBRE_CHAN_4)	TXN
TXCHARISK [0:0] (GT_FIBRE_CHAN_1) TXCHARISK [1:0] (GT_FIBRE_CHAN_2) TXCHARISK [3:0] (GT_FIBRE_CHAN_4)	TXP
TXDATA [7:0] (GT_FIBRE_CHAN_1) TXDATA [15:0] (GT_FIBRE_CHAN_2) TXDATA [31:0] (GT_FIBRE_CHAN_4)	TXRUNDISP [0:0] (GT_FIBRE_CHAN_1) TXRUNDISP [1:0] (GT_FIBRE_CHAN_2) TXRUNDISP [3:0] (GT_FIBRE_CHAN_4)
TXFORCECRCERR	
TXINHIBIT	
TXPOLARITY	
TXRESET	
TXUSRCLK	
TXUSRCLK2	

GT_INFINIBAND_*n*

Gigabit Transceiver for High-Speed I/O

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II PRO*	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

*Supported for Virtex-II PRO but not for Virtex-II

This Infiniband gigabit transceiver supports 1, 2, and 4-byte data paths. The letter *n* represents number of bytes of the data path. Valid values are 1, 2 or 4.

You can also set attributes for the primitives. See Table 1-8 of the *Rocket I/O Transceiver User Guide* for a description of these attributes. See Table 1-10 of the *Rocket I/O Transceiver User Guide* for the default attribute values.

The following table lists the input and output ports for all values of *n*. For a description of each of the ports, see Table 1-7 in the *Rocket I/O Transceiver User Guide.*

Inputs	Outputs
CHBONDI [3:0]	CHBONDDONE
CONFIGENABLE	CHBONDO [3:0]
CONFIGIN	CONFIGOUT
ENCHANSYNC	RXBUFSTATUS [1:0]
ENMCOMMAALIGN	RXCHARISCOMMA [0:0] (GT_INFINIBAND_1) RXCHARISCOMMA [1:0] (GT_INFINIBAND_2) RXCHARISCOMMA [3:0] (GT_INFINIBAND_4)
ENPCOMMAALIGN	RXCHARISK [0:0] (GT_INFINIBAND_1) RXCHARISK [1:0] (GT_INFINIBAND_2) RXCHARISK [3:0] (GT_INFINIBAND_4)
LOOPBACK [1:0]	RXCHECKINGCRC
POWERDOWN	RXCLKCORCNT [2:0]
REFCLK	RXCOMMADET
REFCLK2	RXCRCERR
REFCLKSEL	RXDATA [7:0] (GT_INFINIBAND_1) RXDATA [15:0] (GT_INFINIBAND_2) RXDATA [31:0] (GT_INFINIBAND_4)
RXN	RXDISPERR [0:0] (GT_INFINIBAND_1) RXDISPERR [1:0] (GT_INFINIBAND_2) RXDISPERR [3:0] (GT_INFINIBAND_4
RXP	RXLOSSOFSYNC [1:0]
RXPOLARITY	RXNOTINTABLE [0:0] (GT_INFINIBAND_1) RXNOTINTABLE [1:0] (GT_INFINIBAND_2) RXNOTINTABLE [3:0] (GT_INFINIBAND_4)
RXRESET	RXREALIGN
RXUSRCLK	RXRECCLK

Inputs	Outputs
RXUSRCLK2	RXRUNDISP [0:0] (GT_INFINIBAND_1) RXRUNDISP [1:0] (GT_INFINIBAND_2) RXRUNDISP [3:0] (GT_INFINIBAND_4)
TXBYPASS8B10B [0:0] (GT_INFINIBAND_1) TXBYPASS8B10B [1:0] (GT_INFINIBAND_2) TXBYPASS8B10B [3:0] (GT_INFINIBAND_4)	TXBUFERR
TXCHARDISPMODE [0:0] (GT_INFINIBAND_1) TXCHARDISPMODE [1:0] (GT_INFINIBAND_2) TXCHARDISPMODE [3:0] (GT_INFINIBAND_4)	TXKERR [0:0] (GT_INFINIBAND_1) TXKERR [1:0] (GT_INFINIBAND_2) TXKERR [3:0] (GT_INFINIBAND_4)
TXCHARDISPVAL [0:0] (GT_INFINIBAND_1) TXCHARDISPVAL [1:0] (GT_INFINIBAND_2) TXCHARDISPVAL [3:0] (GT_INFINIBAND_4)	TXN
TXCHARISK [0:0] (GT_INFINIBAND_1) TXCHARISK [1:0] (GT_INFINIBAND_2) TXCHARISK [3:0] (GT_INFINIBAND_4)	TXP
TXDATA [7:0] (GT_INFINIBAND_1) TXDATA [15:0] (GT_INFINIBAND_2) TXDATA [31:0] (GT_INFINIBAND_4)	TXRUNDISP [0:0] (GT_INFINIBAND_1) TXRUNDISP [1:0] (GT_INFINIBAND_2) TXRUNDISP [3:0] (GT_INFINIBAND_4)
TXFORCECRCERR	
TXINHIBIT	
TXPOLARITY	
TXRESET	
TXUSRCLK	
TXUSRCLK2	

GT_XAUI_*n*

10-Gigabit Transceiver for High-Speed I/O

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II PRO*	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

*Supported for Virtex-II PRO but not for Virtex-II

This 10-gigabit Ethernet transceiver supports 1, 2, and 4-byte data paths. The letter *n* represents number of bytes of the data path. Valid values are 1, 2 or 4.

You can also set attributes for the primitives. See Table 1-8 of the *Rocket I/O Transceiver User Guide* for a description of these attributes. See Table 1-10 of the *Rocket I/O Transceiver User Guide* for the default attribute values.

The following table lists the input and output ports for all values of *n*. For a description of each of the ports, see Table 1-7 in the *Rocket I/O Transceiver User Guide.*

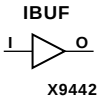
Inputs	Outputs
CHBONDI [3:0]	CHBONDDONE
CONFIGENABLE	CHBONDO [3:0]
CONFIGIN	CONFIGOUT
ENCHANSYNC	RXBUFSTATUS [1:0]
ENMCOMMAALIGN	RXCHARISCOMMA [0:0] (GT_XAUI_1) RXCHARISCOMMA [1:0] (GT_XAUI_2) RXCHARISCOMMA [3:0] (GT_XAUI_4)
ENPCOMMAALIGN	RXCHARISK [0:0] (GT_XAUI_1) RXCHARISK [1:0] (GT_XAUI_2) RXCHARISK [3:0] (GT_XAUI_4)
LOOPBACK [1:0]	RXCHECKINGCRC
POWERDOWN	RXCLKCORCNT [2:0]
REFCLK	RXCOMMADET
REFCLK2	RXCRCERR
REFCLKSEL	RXDATA [7:0] (GT_XAUI_1) RXDATA [15:0] (GT_XAUI_2) RXDATA [31:0] (GT_XAUI_4)
RXN	RXDISPERR [0:0] (GT_XAUI_1) RXDISPERR [1:0] (GT_XAUI_2) RXDISPERR [3:0] (GT_XAUI_4
RXP	RXLOSSOFSYNC [1:0]
RXPOLARITY	RXNOTINTABLE [0:0] (GT_XAUI_1) RXNOTINTABLE [1:0] (GT_XAUI_2) RXNOTINTABLE [3:0] (GT_XAUI_4)
RXRESET	RXREALIGN
RXUSRCLK	RXRECCLK

Inputs	Outputs
RXUSRCLK2	RXRUNDISP [0:0] (GT_XAUI_1) RXRUNDISP [1:0] (GT_XAUI_2) RXRUNDISP [3:0] (GT_XAUI_4)
TXBYPASS8B10B [0:0] (GT_XAUI_1) TXBYPASS8B10B [1:0] (GT_XAUI_2) TXBYPASS8B10B [3:0] (GT_XAUI_4)	TXBUFERR
TXCHARDISPMODE [0:0] (GT_XAUI_1) TXCHARDISPMODE [1:0] (GT_XAUI_2) TXCHARDISPMODE [3:0] (GT_XAUI_4)	TXKERR [0:0] (GT_XAUI_1) TXKERR [1:0] (GT_XAUI_2) TXKERR [3:0] (GT_XAUI_4)
TXCHARDISPVAL [0:0] (GT_XAUI_1) TXCHARDISPVAL [1:0] (GT_XAUI_2) TXCHARDISPVAL [3:0] (GT_XAUI_4)	TXN
TXCHARISK [0:0] (GT_XAUI_1) TXCHARISK [1:0] (GT_XAUI_2) TXCHARISK [3:0] (GT_XAUI_4)	TXP
TXDATA [7:0] (GT_XAUI_1) TXDATA [15:0] (GT_XAUI_2) TXDATA [31:0] (GT_XAUI_4)	TXRUNDISP [0:0] (GT_XAUI_1) TXRUNDISP [1:0] (GT_XAUI_2) TXRUNDISP [3:0] (GT_XAUI_4)
TXFORCECRCERR	
TXINHIBIT	
TXPOLARITY	
TXRESET	
TXUSRCLK	
TXUSRCLK2	

IBUF, 4, 8, 16

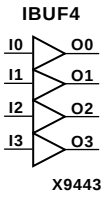
Single- and Multiple-Input Buffers

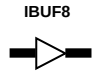
Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
IBUF	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IBUF4, IBUF8, IBUF16	Macro	Macro	Macro	Macro	Macro	Macro

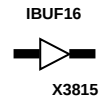


IBUF, IBUF4, IBUF8, and IBUF16 are single- and multiple-input buffers. An IBUF isolates the internal circuit from the signals coming into a chip. IBUFs are contained in input/output blocks (IOBs). IBUF inputs (I) are connected to an IPAD or an IOPAD. IBUF outputs (O) are connected to the internal circuit.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, see the "IBUF_selectIO" section for information on IBUF variants with selectable I/O interfaces. IBUF, 4, 8, and 16 use the LVTTL I/O standard.







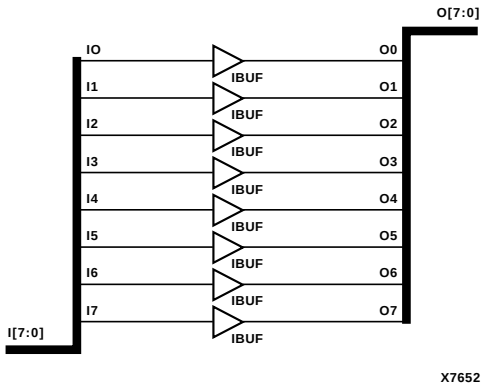


Figure 6-1 IBUF8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-II E, Virtex, Virtex-E

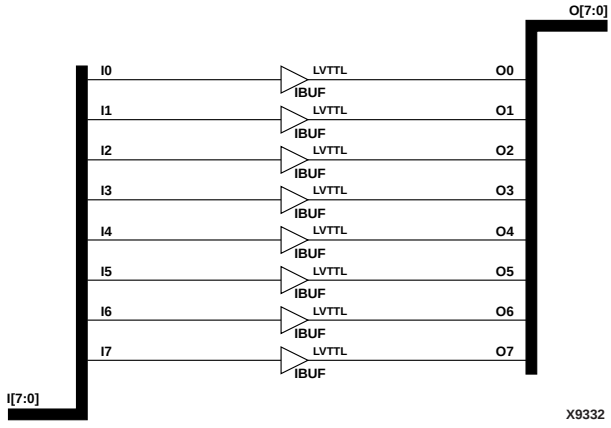
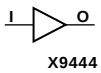


Figure 6-2 IBUF8 Implementation Virtex-II, Virtex-II PRO

IBUF_*selectIO*

Single Input Buffer with Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



For Spartan-II, Spartan-IIE, Virtex, and Virtex-E, IBUF and its selectIO variants (listed in the "Components" column in Table 6-1) are single input buffers whose I/O interface corresponds to a specific I/O standard. The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. For example, IBUF_SSTL3_II is a single input buffer that uses the SSTL3_II I/O-signaling standard. You can attach an IOSTANDARD attribute to an IBUF instance instead of using an IBUF_*selectIO* component. Check marks (√) in the "Spartan-II, Spartan-IIE, Virtex" and "Virtex-E" columns indicate the components and IOSTANDARD attribute values available for those architectures.

An IBUF isolates the internal circuit from the signals coming into a chip. For Spartan-II, Spartan-IIE, Virtex, and Virtex-E, the dedicated GCLKIOB pad is input only. IBUF inputs (I) are connected to an IPAD or IOPAD. IBUF outputs (O) are connected to the internal circuit.

The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffers. See the "SelectI/O Usage Rules" section below for information on using these components and IOSTANDARD attributes.

Table 6-1 Spartan-II, Spartan-IIE, Virtex, and Virtex-E IBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II, Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Input VCCO	VREF
IBUF	√	√	(defaults to LVTTL)	3.3	N/A
IBUF_AGP	√	√	AGP	N/A	1.32
IBUF_CTT	√	√	CTT	N/A	1.50
IBUF_GTL	√	√	GTL	N/A	0.80
IBUF_GTLP	√	√	GTLP	N/A	1.00
IBUF_HSTL_I	√	√	HSTL_I	N/A	0.75
IBUF_HSTL_III	√	√	HSTL_III	1.5	0.90
IBUF_HSTL_IV	√	√	HSTL_IV	N/A	0.90
IBUF_LVCMOS2	√		LVCMOS2	2.5	N/A
IBUF_LVCMOS15			LVCMOS15	1.5	N/A
IBUF_LVCMOS18		√	LVCMOS18	1.8	N/A
IBUF_LVCMOS25		√	LVCMOS25	2.5	N/A
IBUF_LVCMOS33		√	LVCMOS33	3.3	N/A
IBUF_LVDS		√	LVDS	N/A	N/A
IBUF_LVPECL		√	LVPECL	N/A	N/A
IBUF_LVTTL	√	√	LVTTL	N/A	N/A

Table 6-1 Spartan-II, Spartan-IIE, Virtex, and Virtex-E IBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II, Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Input VCCO	VREF
IBUF_PCI33_3	√	√	PCI33_3	3.3	N / A
IBUF_PCI33_5	√		PCI33_5	N / A	N / A
IBUF_PCI66_3	√	√	PCI66_3	3.3	N / A
IBUF_SSTL2_I	√	√	SSTL2_I	N / A	1.25
IBUF_SSTL2_II	√	√	SSTL2_II	N / A	1.25
IBUF_SSTL3_I	√	√	SSTL3_I	N / A	1.50
IBUF_SSTL3_II	√	√	SSTL3_II	N / A	1.50

The Virtex-II and Virtex-II PRO library includes some IBUF_*selectIO* components for compatibility with older, existing designs and other architectures. For new Virtex-II and Virtex-II PRO designs, however, the recommended method for using IBUF selectI/O buffers is to attach an IOSTANDARD attribute to an IBUF component. For example, attach IOSTANDARD=GTLP to an IBUF instead of using the IBUF_GTLP component for new Virtex-II and Virtex-II PRO designs. The IOSTANDARD attributes that can be attached to an IBUF component are listed in the "IOSTANDARD (Attribute Value)" column in Table 6-2. See the "SelectI/O Usage Rules" section for information on using these IOSTANDARD attributes.

Table 6-2 Virtex-II, Virtex-II PRO IBUF_*selectIO* IOSTANDARD Attributes

Component[a]	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Input VCCO	VREF	Terminate Type (Virtex-II only)
IBUF	√	AGP*	N / A	1.32	None
		*does not apply to Virtex-II PRO			
IBUF	√	GTL	N / A	0.80	None
IBUF	√	GTL_DCI	1.2	0.80	Single
IBUF	√	GTLP	N / A	1.00	None
IBUF	√	GTLP_DCI	1.5	1.00	Single
IBUF	√	HSTL_I	N / A	0.75	None
IBUF	√	HSTL_I_18	1.8	0.75	None
IBUF	√	HSTL_I_DCI	1.5	0.75	Split
IBUF	√	HSTL_I_DCI_18	1.8	0.75	Split
IBUF	√	HSTL_II	N / A	0.75	None
IBUF	√	HSTL_II_18	1.8	0.75	None
IBUF	√	HSTL_II_DCI	1.5	0.75	Split
IBUF	√	HSTL_II_DCI_18	1.8	0.75	Split
IBUF	√	HSTL_III	1.5	0.90	None
IBUF	√	HSTL_III_18	1.8	0.90	None
IBUF	√	HSTL_III_DCI	1.5	0.90	Split
IBUF	√	HSTL_III_DCI_18	1.8	0.90	Split

Table 6-2 Virtex-II, Virtex-II PRO IBUF_*selectIO* IOSTANDARD Attributes

Component[a]	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Input VCCO	VREF	Terminate Type (Virtex-II only)
IBUF	√	HSTL_IV	N/A	0.90	None
IBUF	√	HSTL_IV_18	1.8	0.90	None
IBUF	√	HSTL_IV_DCI	1.5	0.90	Split
IBUF	√	HSTL_IV_DCI_18	1.8	0.90	Split
IBUF	√	LVCMOS15	1.5	N/A	None
IBUF	√	LVCMOS18	1.8	N/A	None
IBUF	√	LVCMOS2	2.0	N/A	None
IBUF	√	LVCMOS25	2.5	N/A	None
IBUF	√	LVCMOS33	3.3	N/A	None
IBUF	√	LVDCI_15	N/A	N/A	Driver
IBUF	√	LVDCI_18	N/A	N/A	Driver
IBUF	√	LVDCI_25	N/A	N/A	Driver
IBUF	√	LVDCI_33	N/A	N/A	Driver
IBUF	√	LVDCI_DV2_15	N/A	N/A	Driver
IBUF	√	LVDCI_DV2_18	N/A	N/A	Driver
IBUF	√	LVDCI_DV2_25	N/A	N/A	Driver
IBUF	√	LVDCI_DV2_33	N/A	N/A	Driver
IBUF	√	LVTTL (default)	3.3	N/A	None
IBUF	√	LVTTL_33	3.3	N/A	None
IBUF	√	PCI33_3	3.3	N/A	None
IBUF	√	PCI66_3	3.3	N/A	None
IBUF	√	PCIX	3.3	N/A	None
IBUF	√	SSTL2_I	N/A	1.25	None
IBUF	√	SSTL2_I_DCI	2.5	1.25	Split
IBUF	√	SSTL2_II	N/A	1.25	None
IBUF	√	SSTL2_II_DCI	2.5	1.25	Split
IBUF	√	SSTL3_I	N/A	1.50	None
IBUF	√	SSTL3_I_DCI	3.3	1.25	Split
IBUF	√	SSTL3_II	N/A	1.50	None
IBUF	√	SSTL3_II_DCI	3.3	1.25	Split

[a]Attach an IOSTANDARD attribute to an IBUF and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the input for the I/O standard associated with that value.

SelectI/O Usage Rules

The Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO architectures include a versatile SelectI/O interface to multiple voltage and drive standards. To select an I/O standard, you must choose the appropriate component from the library or add an IOSTANDARD attribute to the appropriate buffer component. For example, for an input buffer that uses the GTL standard, you would choose the IBUF_GTL component or choose the IBUF component and attach the IOSTANDARD=GTL attribute to it.

See the following sections for information on the various input/output buffer components and attributes available to implement the desired standar: "IBUF_selectIO", "IBUFG, IBUFG_selectIO", "IOBUF, IOBUF_selectIO", "OBUFT_selectIO", and "OBUFT_selectIO" sections.

The hardware implementation of the various I/O standards requires that certain usage rules be followed. Each I/O standard has voltage source requirements for input reference (VREF), output drive (VCCO), or both. In addition, Virtex-II and Virtex-II PRO have terminate type requirements. Each Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO device has eight banks (two on each edge). Each bank has voltage sources shared by all I/O in the bank. Therefore, in a particular bank, the voltage source (for either input or output) must be of the same type.

For Spartan-II, Spartan-IIE, Virtex, and VirtexE, see the "Virtex, Virtex-E, Spartan-II, and Spartan-IIE Banking Rules" section. Virtex-E follows the same banking rules as Virtex with a few additions. See "Additional Banking Rules for Virtex-E" section for the additional Virtex-E rules. Virtex-II and Virtex-II PRO have their own set of banking rules, see the "Virtex-II, Virtex-II PRO Banking Rules" section for Virtex-II and Virtex-II PRO rules.

Virtex, Virtex-E, Spartan-II, and Spartan-IIE Banking Rules

The hardware implementation of the various I/O standards requires that certain usage rules be followed. As shown in the following table, each I/O standard has voltage source requirements for input reference (VREF), output drive (VCCO), or both. Each Spartan-II, Spartan-IIE, Virtex, and Virtex-E, device has eight banks (two on each edge). Each bank has voltage sources shared by all I/O in the bank. Therefore, in a particular bank, the voltage source (for either input or output) must be of the same type. The Input Banking (VREF) Rules section and the Output Banking (VCCO) Rules section below summarize the SelectI/O component usage rules based on the hardware implementation.

Table 6-3 I/O Standards Supported in Virtex, Virtex-E, Spartan-II, and Spartan-IIE

I/O Standard	Application	Description	Output VCCO	Input VCCO	VREF
AGP	Graphics	Advanced graphics port	3.3	N/A	1.32
CTT	Memory	Center tap terminated	3.3	N/A	1.50
LVTTL	General Purpose	Low voltage transistor-transistor logic	3.3	3.3	N/A
LVCMOS2	General Purpose	Low voltage complementary metal-oxide semiconductor	2.5	2.5	N/A
PCI33_3	PCI	Peripheral component interface (33MHz 3.3V)	3.3	3.3	N/A
PCI33_5	PCI	Peripheral component interface (33MHZ 5.0V)	3.3	N/A	N/A
PCI66_3	PCI	Peripheral component interface (66MHz 3.3V)	3.3	3.3	N/A
GTL	Backplane	Gunning transceiver logic interface (to processors or backplane driver)	N/A	N/A	0.80
GTL+ (GTLP)	Backplane	Gunning transceiver logic interface Plus	N/A	N/A	1.00
HSTL_I	Hitachi SRAM	High Speed transceiver logic	1.5	N/A	0.75

Table 6-3 I/O Standards Supported in Virtex, Virtex-E, Spartan-II, and Spartan-IIE

I/O Standard	Application	Description	Output VCCO	Input VCCO	VREF
HSTL_III	Hitachi SRAM	High Speed transceiver logic	1.5	N/A	0.90
HSTL_IV	Hitachi SRAM	High Speed transceiver logic	1.5	N/A	0.75
SSTL2_I	Synchronous DRAM	Stub-series terminated logic interface for SDRAM	2.5	N/A	1.10
SSTL2_II	Synchronous DRAM	Stub-series terminated logic interface for SDRAM	2.5	N/A	1.10
SSTL3_I	Synchronous DRAM	Stub-series terminated logic interface for SDRAM	3.3	N/A	0.90
SSTL3_II	Synchronous DRAM	Stub-series terminated logic interface for SDRAM	3.3	N/A	1.50

Input Banking (VREF) Rules

The low-voltage I/O standards that have a differential amplifier input require a voltage reference input (VREF). The VREF voltage source is provided as an external signal to the chip that is banked internal to the chip.

- Any input buffer component that does not require a VREF source (LVTTL, LVCMOS2, PCI*) can be placed in any bank.
- All input buffer components that require a VREF source (GTL*, HSTL*, SSTL*, CTT, AGP) must be of the same I/O standard in a particular bank. For example, IBUF_SSTL2_I and IBUFG_SSTL2_I are compatible since they are the same I/O standard (SSTL2_I).
- If the bank contains any input buffer component that requires a VREF source, the following conditions apply.
  - One or more VREF sources must be connected to the bank via an IOB.
  - The number of VREF sources is dependent on the device and package.
  - The locations of the VREF sources are fixed for each device/package.
  - All VREF sources must be used in that bank.
- If the bank contains no input buffer component that requires a VREF source, the IOBs for VREF sources can be used for general I/O.
- Output buffer components of any type can be placed in the bank.

Output Banking (VCCO) Rules

Because Virtex, Virtex-E, Spartan-II, and Spartan-IIE have multiple low-voltage standards and also needs to be 5V tolerant, some control is required over the distribution of VCCO, the drive source voltage for output pins. To provide for maximum flexibility, the output pins are banked. In comparison to the VREF sources described above, the VCCO voltage sources are dedicated pins on the device and do not consume valuable IOBs.

- Any output buffer component that does not require a VCCO source (GTL, GTL+) can be placed in any bank.

- To be placed in a particular bank, all output buffer components that require VCCO must have the same supply voltage (VCCO). For example, OBUF_SSTL3_I and OBUF_PCI33_3 are compatible in the same output bank since VCCO=3.3 for both.
- Input buffer components of any type can be placed in the bank.
- The configuration pins on a Virtex, Virtex-E, Spartan-II, and Spartan-IIE device are on the right side of the chip. When configuring the device through a serial PROM, the user is required to use a VCCO of 3.3V in the two banks on the right hand side of the chip. If the user is not configuring the device through a serial PROM, the VCCO requirement is dependent upon the configuration source.

Banking Rules for OBUFT_*selectIO* with KEEPER

If a KEEPER symbol is attached to an OBUFT_*selectIO* component (3-state output buffer) for an I/O standard that requires a VREF (for example, OBUFT_GTL, OBUFT_SSTL3_I), then the OBUFT_*selectIO* component follows the same rules as an IOBUF_*selectIO* component for the same standard. It must follow both the input banking and output banking rules. The KEEPER element requires that the VREF be properly driven.

Additional Banking Rules for Virtex-E

The Virtex-E architecture requires the same banking rules as described in the "Virtex, Virtex-E, Spartan-II, and Spartan-IIE Banking Rules" section. In addition for Virtex-E, certain input standards are incompatible with certain output standards. Therefore, the following additional rules apply:

- LVTTL and PCI 3.3V inputs cannot be placed in a bank where VCCO is 3.3V.
- LVCMOS2 inputs cannot be placed in a bank where VCCO is 2.5V.
- If a design contains a combination of LVTTL or PCI 3.3V inputs along with outputs that require a VCCO other than 3.3V, all IOBs must be locked.

Table 6-4 Additional I/O Standards Supported in Virtex-E

I/O Standard	Application	Description	Output VCCO	Input VCCO	VREF
Single Ended:					
LVCMOS15	General Purpose	Low voltage complementary metal-oxide semiconductor	1.5	1.5	N/A
LVCMOS18	General Purpose	Low voltage complementary metal-oxide semiconductor	1.8	1.8	N/A
LVCMOS25	General Purpose	Low voltage complementary metal-oxide semiconductor	2.5	2.5	N/A
LVCMOS33	General Purpose	Low voltage complementary metal-oxide semiconductor	3.3	3.3	N/A
GTL+ (GTLP)	Backplane	Gunning transceiver logic interface Plus	N/A	N/A	1.00
HSTL_I	Hitachi SRAM	High Speed transceiver logic, Class I	1.5	N/A	0.75
HSTL_III	Hitachi SRAM	High Speed transceiver logic, Class III	1.5	N/A	0.90

Table 6-4 Additional I/O Standards Supported in Virtex-E

I/O Standard	Application	Description	Output VCCO	Input VCCO	VREF
HSTL_IV	Hitachi SRAM	High Speed transceiver logic, Class IV	1.5	N / A	0.75
SSTL2_I	Synchronous DRAM	Stub-series terminated logic interface for SDRAM, Class I	2.5	N / A	1.10
SSTL2_II	Synchronous DRAM	Stub-series terminated logic interface for SDRAM, Class II	2.5	N / A	1.10
SSTL3_I	Synchronous DRAM	Stub-series terminated logic interface for SDRAM, Class I	3.3	N / A	0.90
SSTL3_II	Synchronous DRAM	Stub-series terminated logic interface for SDRAM, class II	3.3	N / A	1.50
Differential Signaling:					
LVDS	Point-to-point or multi-drop backplanes, high noise immunity	Low voltage differential signal	2.5	2.5	N / A
LVPECL	High performance clocking, backplanes, differential 100MHz+ clocking, optical transceiver, high speed networking and mixed-signal interfacing	Low voltage positive emitter couple logic	2.5	2.5	N / A

Virtex-II, Virtex-II PRO Banking Rules

The hardware implementation of the various I/O standards requires that certain usage rules be followed. Virtex-II and Virtex-II PRO devices have eight banks (two on each edge), numbered from 0 through 7. Each bank has voltage sources shared by all I/O in the bank.

As shown in Table 6-5, for the I/O standards supported in Virtex-II and Virtex-II PRO, each I/O standard has voltage source requirements for input reference (VREF), output drive (VCCO), and Terminate Type.

Table 6-5 I/O Standards Supported In Virtex-II and Virtex-II PRO

I/O Standard	Application	Description	Output VCCO	Input VCCO	VREF	Terminate Type
Single-Ended:						
AGP	Graphics	Advanced graphics port	3.3	N / A	1.32	None
GTL	Memory	Gunning transceiver logic interface (to processors or backplace driver)	N / A	N / A	0.80	None
GTL_DCI	Memory	Gunning transceiver logic interface with on-chip Digital Controlled Impedance	1.2	1.2	0.80	Single
GTL+ (GTLP)	Memory	Gunning transceiver logic interface Plus	N / A	N / A	1.00	None

Table 6-5 I/O Standards Supported In Virtex-II and Virtex-II PRO

I/O Standard	Application	Description	Output VCCO	Input VCCO	VREF	Terminate Type
GTLP_DCI	Memory	Gunning transceiver logic interface with on-chip Digital Controlled Impedance	1.5	1.5	1.00	Single
HSTL_I	Hitachi SRAM	High Speed transceiver logic	1.5	N / A	0.75	None
HSTL_I__DCI	Hitachi SRAM	High Speed transceiver logic interface with on-chip Digital Controlled Impedance	1.5	1.5	0.75	Split
HSTL_II	Hitachi SRAM	High Speed transceiver logic	1.5	N / A	0.75	None
HSTL_II__DCI	Hitachi SRAM	High Speed transceiver logic interface with on-chip Digital Controlled Impedance	1.5	1.5	0.75	Split
HSTL_III	Hitachi SRAM	High Speed transceiver logic	1.5	1.5	0.90	None
HSTL_III__DCI	Hitachi SRAM	High Speed transceiver logic interface with on-chip Digital Controlled Impedance	1.5	1.5	0.90	Split
HSTL_IV	Hitachi SRAM	High Speed transceiver logic	1.5	N / A	0.90	None
HSTL_IV__DCI	Hitachi SRAM	High Speed transceiver logic interface with on-chip Digital Controlled Impedance	1.5	1.5	0.90	Split
LVCMOS15[a]	General Purpose	Low voltage complementary metal-oxide semiconductor	1.5	1.5	N / A	None
LVCMOS18[a]	General Purpose	Low voltage complementary metal-oxide semiconductor	1.8	1.8	N / A	None
LVCMOS25[a]	General Purpose	Low voltage complementary metal-oxide semiconductor	2.5	2.5	N / A	None
LVCMOS33[a]	General Purpose	Low voltage complementary metal-oxide semiconductor	3.3	3.3	N / A	None
LVDCI_15	General Purpose	Low voltage complementary metal-oxide semiconductor with on-chip Digital Controlled Impedance	1.5	N / A	N / A	Driver
LVDCI_18	General Purpose	Low voltage complementary metal-oxide semiconductor with on-chip Digital Controlled Impedance	1.8	N / A	N / A	Driver
LVDCI_25	General Purpose	Low voltage complementary metal-oxide semiconductor with on-chip Digital Controlled Impedance	2.5	N / A	N / A	Driver
LVDCI_33	General Purpose	Low voltage complementary metal-oxide semiconductor with on-chip Digital Controlled Impedance	3.3	N / A	N / A	Driver
LVDCI_DV2_15	General Purpose	Low voltage complementary metal-oxide semiconductor with on-chip Digital Controlled Impedance	1.5	N / A	N / A	Driver

Table 6-5 I/O Standards Supported In Virtex-II and Virtex-II PRO

I/O Standard	Application	Description	Output VCCO	Input VCCO	VREF	Terminate Type
LVDCI_DV2_18	General Purpose	Low voltage complementary metal-oxide semiconductor with on-chip Digital Controlled Impedance	1.8	N / A	N / A	Driver
LVDCI_DV2_25	General Purpose	Low voltage complementary metal-oxide semiconductor with on-chip Digital Controlled Impedance	2.5	N / A	N / A	Driver
LVDCI_DV2_33	General Purpose	Low voltage complementary metal-oxide semiconductor with on-chip Digital Controlled Impedance	3.3	N / A	N / A	Driver
LVTTL[a]	General Purpose	Low voltage transistor-transistor logic	3.3	3.3	N / A	None
LVTTL_33[a]	General Purpose	Low voltage transistor-transistor logic	3.3	3.3	N / A	None
PCI33_3	PCI	Peripheral component interface (33MHz 3.3V)	3.3	3.3	N / A	None
PCI66_3	PCI	Peripheral component interface (66MHz 3.3V)	3.3	3.3	N / A	None
PCIX	PCI	Peripheral component interface	3.3	3.3	N / A	None
SSTL2_I	Synchronous DRAM	Stub-series terminated logic interface for SDRAM	2.5	N / A	1.25	None
SSTL2_I_DCI	Synchronous DRAM	Stub-series terminated logic interface for SDRAM with on-chip Digital Controlled Impedance	2.5	2.5	1.25	Split
SSTL2_II	Synchronous DRAM	Stub-series terminated logic interface for SDRAM	2.5	N / A	1.25	None
SSTL2_II_DCI	Synchronous DRAM	Stub-series terminated logic interface for SDRAM with on-chip Digital Controlled Impedance	2.5	2.5	1.25	Split
SSTL3_I	Synchronous DRAM	Stub-series terminated logic interface for SDRAM	3.3	N / A	1.50	None
SSTL3_I_DCI	Synchronous DRAM	Stub-series terminated logic interface for SDRAM with on-chip Digital Controlled Impedance	3.3	3.3	1.5	Split
SSTL3_II	Synchronous DRAM	Stub-series terminated logic interface for SDRAM	3.3	N / A	1.50	None
SSTL3_II_DCI	Synchronous DRAM	Stub-series terminated logic interface for SDRAM with on-chip Digital Controlled Impedance	3.3	3.3	1.5	Split

Table 6-5 I/O Standards Supported In Virtex-II and Virtex-II PRO

I/O Standard	Application	Description	Output VCCO	Input VCCO	VREF	Terminate Type
Differential Signaling:						
BLVDS_25	Bus LVDS backplanes, high noise immunity, bus architecture back-planes	Bidirectional low voltage differential signal	2.5	2.5	N/A	None
LDT_25	Point-to-point multi-drop backplanes, high noise immunity	Lightning Data Transport	2.5	2.5	N/A	None
LVDS_25	Point-to-point multi-drop backplanes, high noise immunity	Low voltage differential signal	2.5	N/A	N/A	None
LVDS_33	Point-to-point and multi-drop backplanes, high noise immunity	Low voltage differential signal	3.3	N/A	N/A	None
LVDSEXT_25	Point-to-point multi-drop backplanes, high noise immunity	Extended low voltage differ-ential signal	2.5	N/A	N/A	None
LVDSEXT_33	Point-to-point multi-drop backplanes, high noise immunity	Extended low voltage differ-ential signal	3.3	N/A	N/A	None
LVPECL_33	High performance clocking, backplanes, differential 100 MHz+ clocking, optical trans-ceiver, high speed networking and mixed signal interfacing	Low voltage positive emitter couple logic	3.3	N/A	N/A	None
ULVDS_25	Point-to-point multi-drop backplanes, high noise immunity	Ultra low voltage differential signal	2.5	N/A	N/A	None

Notes:
[a]LVTTL, LVCMOS15, LVCMOS18, LVCMOS25, and LVCOMS33 also require DRIVE and SLEW (FAST or Slow) attributes.

The following rules apply for using the various IO standards with Virtex-II or Virtex-II PRO :

- In any particular Virtex-II or Virtex-II PRO I/O bank, the voltage sources (both input and output) must be compatible. That is, they must have either the same voltage or an undefined (N/A) voltage.
- VREF, VCCO input, and VCCO output must be compatible within an I/O bank.
- In addition, to VREF and VCCO compatibility, the terminate type I/O standards must be compatible within the bank.

  For terminate type compatibility, the following rules apply:

  - Only one I/O buffer with terminate type of SINGLE can be in a particular bank.
  - Only one I/O buffer with terminate type of SPLIT can be in a particular bank.

- Multiple I/O buffers with NONE and DRIVER terminate types can be in a particular bank.
- SPLIT and SINGLE can co-exist in the same bank.
- NONE and DRIVER types can co-exist with SPLIT and SINGLE types.

- The right edge of a Virtex-II or Virtex-II PRO device is set for 3.3V. Therefore, on the right edge of the device, VCCO output and VCCO input must be 3.3V or N/A.
- To place an I/O buffer that requires a VREF in a bank, the reserved VREF sites in that bank must be empty.
- To place an I/O buffer that has a terminate type of SINGLE, SPLIT, or DRIVER in a bank, the reserved VR sites in that bank must be empty.

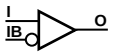
The following table summarizes the values that you need to check for compatibility for each combination of I/O buffer programming (input, output, or bidirectional buffer). For example, the table shows that if you configure an output buffer as LVCMOS25, which has an output voltage of 2.5V, and an input buffer as LVCMOS15, which as an input voltage of 1.5V, the Out/In Voltage is checked. Because they have different voltages, this combination would not be allowed in a particular I/O bank.

IOB Programming Combinations		VREF	Output VCCO	Input VCCO	Out/In Voltage
Input	Input	Check		Check	
Input	Output				Check
Input	Bidirectional	Check		Check	Check
Output	Input				Check
Output	Output		Check		
Output	Bidirectional		Check		Check
Bidirectional	Input	Check		Check	Check
Bidirectional	Output		Check		Check
Bidirectional	Bidirectional	Check	Check	Check	Check

IBUFDS

Differential Signaling Input Buffer with Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



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IBUFDS is an input buffer that supports low-voltage, differential signaling. In IBUFDS, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET and MYNETB).

Inputs		Outputs
I	IB	O
0	0	X
0	1	0
1	0	1
1	1	X

The IOSTANDARD attribute values listed in the following table can be applied to an IBUFDS component to provide selectIO interface capability.

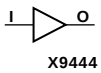
Component	IOSTANDARD (Attribute Value)	Input VCCO	VREF	Terminate Type
IBUFDS[a]	BLVDS_25	2.5	N/A	None
IBUFDS[a]	LDT_25	2.5	N/A	None
IBUFDS[a]	LVDS_25 (default)	N/A	N/A	None
IBUFDS[a]	LVDS_33 *	N/A	N/A	None
	*does not apply to Virtex-II PRO			
IBUFDS[a]	LVDSEXT_25	N/A	N/A	None
IBUFDS[a]	LVDSEXT_33*	N/A	N/A	None
	*does not apply to Virtex-II PRO			
IBUFDS[a]	LVPECL_33*	N/A	N/A	None
	*does not apply to Virtex-II PRO			
IBUFDS[a]	ULVDS_25	N/A	N/A	None

[a]A separate SelectI/O component is not provided. Attach an IOSTANDARD attribute to an IBUFDS and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the inputs for the I/O standard associated with that value.

IBUFG, IBUFG_*selectIO*

Dedicated Input Buffer with Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, IBUFG and its selectIO variants (listed in the "Components" column in the table below) are dedicated input buffers for connecting to the clock buffer BUFG or CLKDLL. The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. For example, IBUFG_SSTL3_II is a single input buffer that uses the SSTL3_II I/O-signaling standard. You can attach an IOSTANDARD attribute to an IBUFG instance instead of using an IBUFG_*selectIO* component. Check marks (√) in the "Spartan-II, Spartan-IIE, Virtex" and "Virtex-E" columns indicate the components and IOSTANDARD attribute values available for those architectures.

The Xilinx implementation software converts each BUFG to an appropriate type of global buffer for the target PLD device. The IBUFG output can be connected to the CLKIN input of a CLKDLL or to the input of a BUFG. IBUFG can be routed to user logic and does not have to be routed to a DLL. The IBUFG can only be driven by an IPAD.

The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffers. See the "SelectI/O Usage Rules" section included in the IBUF_*selectIO* section for information on using these components and the IOSTANDARD attributes.

Table 6-6 Spartan-II, Spartan-IIE, Virtex, and Virtex-E IBUFG_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Input VCCO	VREF
IBUFG	√	√	(defaults to LVTTL)	3.3	N/A
IBUFG_AGP	√	√	AGP	N/A	1.32
IBUFG_CTT	√	√	CTT	N/A	1.50
IBUFG_GTL	√	√	GTL	N/A	0.80
IBUFG_GTLP	√	√	GTLP	N/A	1.00
IBUFG_HSTL_I	√	√	HSTL_I	N/A	0.75
IBUFG_HSTL_III	√	√	HSTL_III	1.5	0.90
IBUFG_HSTL_IV	√	√	HSTL_IV	N/A	0.90
IBUFG_LVCMOS2	√		LVCMOS2	2.5	N/A
IBUFG_LVCMOS15		√	LVCMOS15	1.5	N/A
IBUFG_LVCMOS18		√	LVCMOS18	1.8	N/A
IBUFG_LVCMOS25		√	LVCMOS25	2.5	N/A
IBUFG_LVCMOS33		√	LVCMOS33	3.3	N/A
IBUFG_LVDS		√	LVDS	N/A	N/A

Table 6-6 Spartan-II, Spartan-IIE, Virtex, and Virtex-E IBUFG_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Input VCCO	VREF
IBUFG_LVPECL		√	LVPECL	N/A	N/A
IBUFG_PCI33_3	√	√	PCI33_3	3.3	N/A
IBUFG_PCI33_5	√	√	PCI33_5	N/A	N/A
IBUFG_PCI66_3	√	√	PCI66_3	3.3	N/A
IBUFG_SSTL2_I	√	√	SSTL2_I	N/A	1.25
IBUFG_SSTL2_II	√	√	SSTL2_II	N/A	1.25
IBUFG_SSTL3_I	√	√	SSTL3_I	N/A	1.50
IBUFG_SSTL3_II	√	√	SSTL3_II	N/A	1.50

The Virtex-II and Virtex-II PRO library includes some IBUFG_*selectIO* components for compatibility with older, existing designs and other architectures. For new Virtex-II and Virtex-II PRO designs, however, the recommended method for using IBUFG selectI/O buffers is to attach an IOSTANDARD attribute to an IBUFG component. For example, attach IOSTANDARD=GTLP to an IBUFG instead of using the IBUFG_GTLP component for new Virtex-II and Virtex-II PRO designs. The IOSTANDARD attributes that can be attached to an IBUFG component are listed in the "IOSTANDARD (Attribute Value)" column in Table 6-7<$elemparanum. See the "SelectI/O Usage Rules" section for information on using these IOSTANDARD attributes.

Table 6-7 Virtex-II, Virtex-II PRO IBUFG_*selectIO* IOSTANDARD Attributes

Component[a]	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Input VCCO	VREF	Terminate Type
IBUFG	√	AGP*	N/A	1.32	None
		*does not apply to Virtex-II PRO			
IBUFG	√	GTL	N/A	0.80	None
IBUFG	√	GTL_DCI	1.2	0.80	Single
IBUFG	√	GTLP	N/A	1.00	None
IBUFG	√	GTLP_DCI	1.5	1.00	Single
IBUFG	√	HSTL_I	N/A	0.75	None
IBUFG	√	HSTL_I_18	1.8	0.75	None
IBUFG	√	HSTL_I_DCI	1.5	0.75	Split
IBUFG	√	HSTL_I_DCI_18	1.8	0.75	Split
IBUFG	√	HSTL_II	N/A	0.75	None
IBUFG	√	HSTL_II_18	1.8	0.75	None
IBUFG	√	HSTL_II_DCI	1.5	0.75	Split
IBUFG	√	HSTL_II_DCI_18	1.8	0.75	Split
IBUFG	√	HSTL_III	1.5	0.90	None
IBUFG	√	HSTL_III_18	1.8	0.90	None
IBUFG	√	HSTL_III_DCI	1.5	0.90	Split

Table 6-7 Virtex-II, Virtex-II PRO IBUFG_*selectIO* IOSTANDARD Attributes

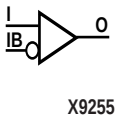
Component[a]	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Input VCCO	VREF	Terminate Type
IBUFG	√	HSTL_III_DCI_18	1.8	0.90	Split
IBUFG	√	HSTL_IV	N/A	0.90	None
IBUFG	√	HSTL_IV_18	1.8	0.90	None
IBUFG	√	HSTL_IV_DCI	1.5	0.90	Split
IBUFG	√	HSTL_IV_DCI_18	1.8	0.90	Split
IBUFG	√	LVCMOS15	1.5	N/A	None
IBUFG	√	LVCMOS18	1.8	N/A	None
IBUFG	√	LVCMOS2	2.0	N/A	None
IBUFG	√	LVCMOS25	2.5	N/A	None
IBUFG	√	LVCMOS33	3.3	N/A	None
IBUFG	√	LVDCI_15	N/A	N/A	Driver
IBUFG	√	LVDCI_18	N/A	N/A	Driver
IBUFG	√	LVDCI_25	N/A	N/A	Driver
IBUFG	√	LVDCI_33	N/A	N/A	Driver
IBUFG	√	LVDCI_DV2_15	N/A	N/A	Driver
IBUFG	√	LVDCI_DV2_18	N/A	N/A	Driver
IBUFG	√	LVDCI_DV2_25	N/A	N/A	Driver
IBUFG	√	LVDCI_DV2_33	N/A	N/A	Driver
IBUFG	√	LVTTL (default)	3.3	N/A	None
IBUFG	√	LVTTL_33	3.3	N/A	None
IBUFG	√	PCI33_3	3.3	N/A	None
IBUFG	√	PCI66_3	3.3	N/A	None
IBUFG	√	PCIX	3.3	N/A	None
IBUFG	√	SSTL2_I	N/A	1.25	None
IBUFG	√	SSTL2_I_DCI	2.5	1.25	Split
IBUFG	√	SSTL2_II	N/A	1.25	None
IBUFG	√	SSTL2_II_DCI	2.5	1.25	Split
IBUFG	√	SSTL3_I	N/A	1.50	None
IBUFG	√	SSTL3_I_DCI	3.3	1.25	Split
IBUFG	√	SSTL3_II	N/A	1.50	None
IBUFG	√	SSTL3_II_DCI	3.3	1.25	Split

[a]Attach an IOSTANDARD attribute to an IBUFG and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the input for the I/O standard associated with that value.

IBUFGDS

Dedicated Differential Signaling Input Buffer with Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



X9255

IBUFGDS is a dedicated differential signaling input buffer for connection to the clock buffer (BUFG) or DCM. In IBUFGDS, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET and MYNETB).

Inputs		Outputs
I	IB	O
0	0	X
0	1	0
1	0	1
1	1	X

The IOSTANDARD attribute values listed in the following table can be applied to an IBUFGDS component to provide selectIO interface capability. See the *Xilinx Constraints Guide* for information using these attributes.

Component	IOSTANDARD (Attribute Value)	Input VCCO	VREF	Terminate Type
IBUFGDS[a]	BLVDS_25	N/A	N/A	None
IBUFGDS[a]	LDT_25	N/A	N/A	None
IBUFGDS[a]	LVDS_25 (default)	N/A	N/A	None
IBUFGDS[a]	LVDS_33 *	N/A	N/A	None
	*does not apply to Virtex-II PRO			
IBUFGDS[a]	LVDSEXT_25	N/A	N/A	None
IBUFGDS[a]	LVDSEXT_33*	N/A	N/A	None
	*does not apply to Virtex-II PRO			
IBUFGDS[a]	LVPECL_33*	N/A	N/A	None
	*does not apply to Virtex-II PRO			

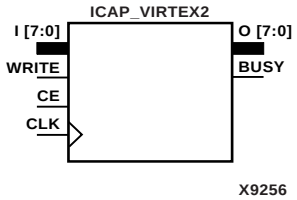
Component	IOSTANDARD (Attribute Value)	Input VCCO	VREF	Terminate Type
IBUFGDS[a]	ULVDS_25*	N/A	N/A	None

[a]A separate SelectI/O component is not provided. Attach an IOSTANDARD attribute to an IBUFGDS and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the inputs for the I/O standard associated with that value.

ICAP_VIRTEX2

User Interface to Virtex-II and Virtex-II PRO Internal Configuration Access Port

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	Primitive	N / A	N / A	N / A

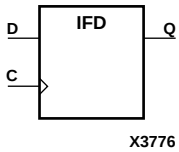


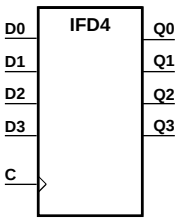
ICAP_VIRTEX2 provides user access to the Virtex-II and Virtex-II PRO internal configuration access port (ICAP).

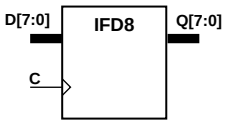
IFD, 4, 8, 16

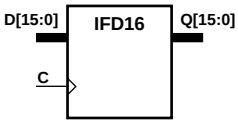
Single- and Multiple-Input D Flip-Flops

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
IFD	Macro	Macro	Macro	Macro	Macro	Macro
IFD4, IFD8, IFD16	Macro	Macro	Macro	Macro	Macro	Macro









The IFD D-type flip-flop is contained in an input / output block (IOB), except for XC9500 / XV / XL, CoolRunner XPLA3. The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

The flip-flops are asynchronously cleared with Low outputs when power is applied.

For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	C	Q
0	↑	0
1	↑	1

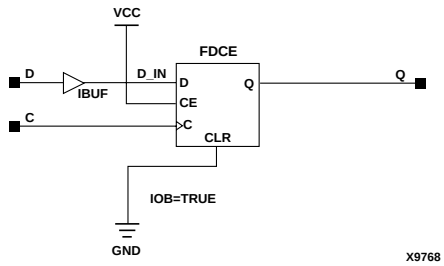


Figure 6-3 IFD Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

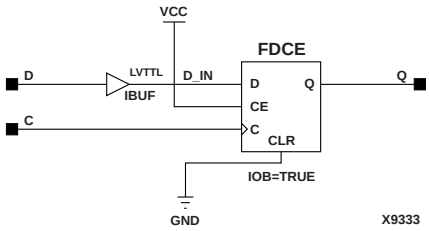


Figure 6-4 IFD Implementation Virtex-II, Virtex-II PRO

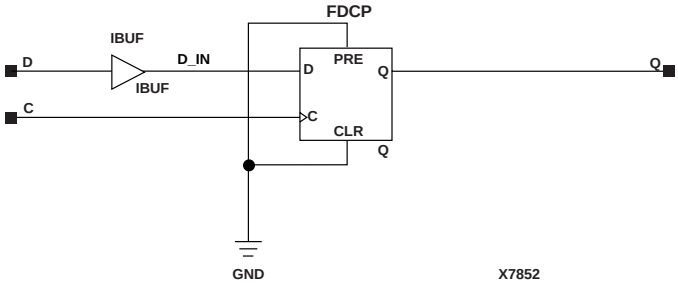


Figure 6-5 IFD Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

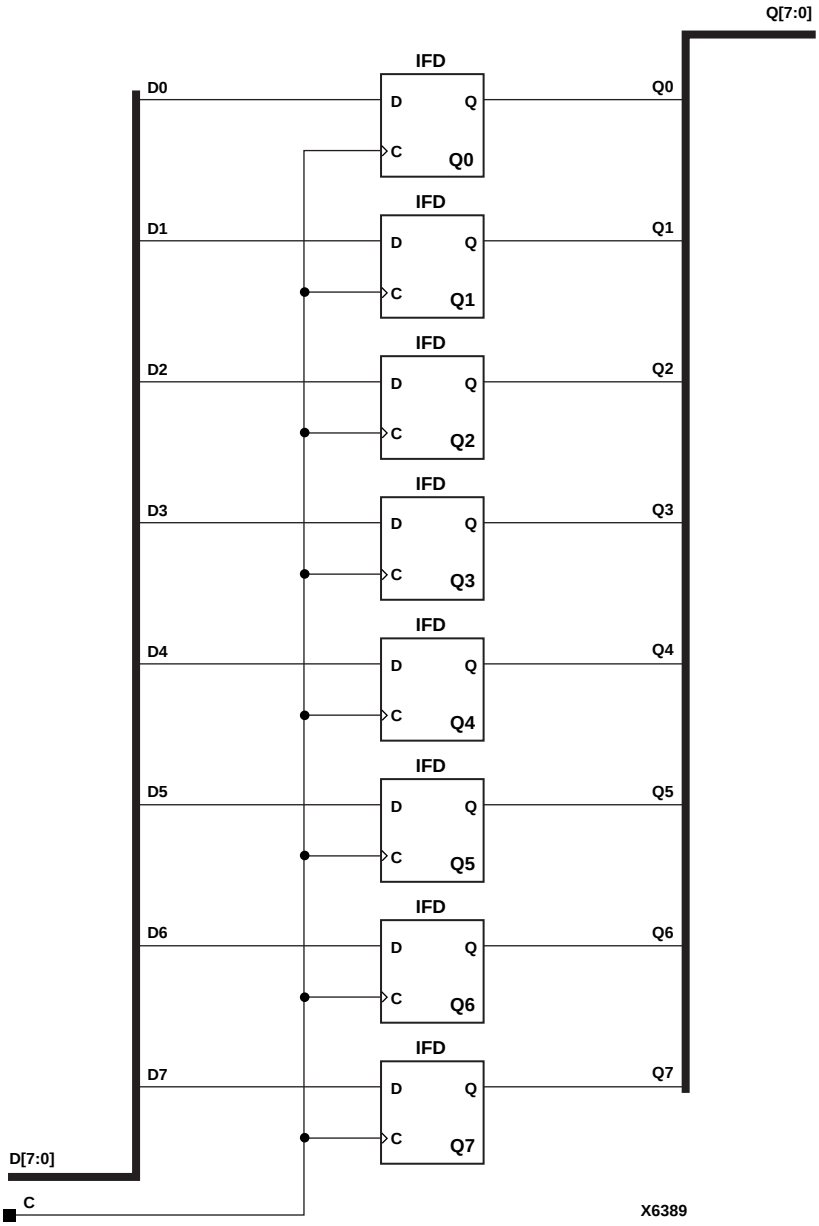
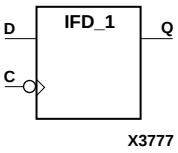


Figure 6-6 IFD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

IFD_1

Input D Flip-Flop with Inverted Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



The IFD_1 D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

The flip-flop is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	C	Q
0	↓	0
1	↓	1

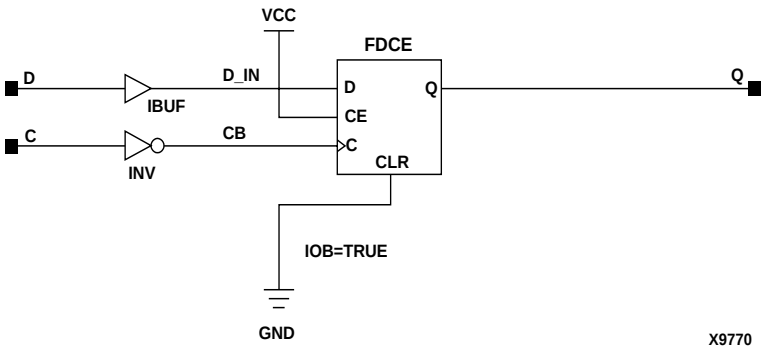


Figure 6-7 IFD_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

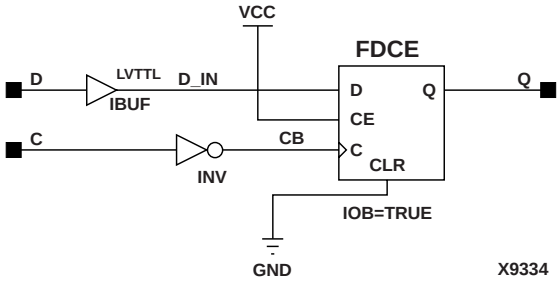
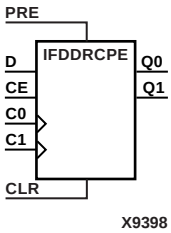


Figure 6-8 IFD_1 Implementation Virtex-II, Virtex-II PRO

IFDDRCPE

Dual Data Rate Input D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	Primitive	N / A	N / A	N / A



IFDDRCPE is a dual data rate (DDR) input D flip-flop with clock enable (CE) and asynchronous preset (PRE) and clear (CLR). It consists of one input buffer and two identical flip-flops (FDCPE).

When the asynchronous PRE is High and CLR is Low, both the Q0 and Q1 outputs are set High. When CLR is High, both outputs are reset Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High. The data is loaded into the Q0 output on the Low-to-High C0 clock transition. The data is loaded into the Q1 output on the Low-to-High C1 clock transition.

The flip-flops are asynchronously cleared with Low outputs when power is applied.

The INIT attribute does not apply to IFDDRCPE components.

Inputs						Outputs	
C0	C1	CE	D	CLR	PRE	Q0	Q1
X	X	X	X	1	0	0	0
X	X	X	X	0	1	1	1
X	X	X	X	1	1	0	0
X	X	0	X	0	0	No Chg	No Chg
↑	X	1	D	0	0	D	No Chg
X	↑	1	D	0	0	No Chg	D

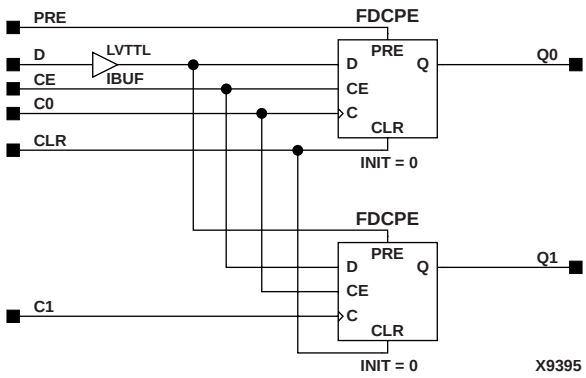
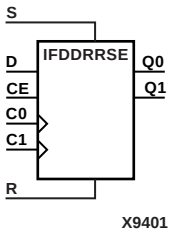


Figure 6-9 IFDDRCPE Implementation Virtex-II, Virtex-II PRO

IFDDRRSE

Dual Data Rate Input D Flip-Flop with Synchronous Reset and Set and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	Primitive	N / A	N / A	N / A



IFDDRRSE is a dual data rate (DDR) input D flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE). It consists of one input buffer and two identical flip-flops (FDRSE).

For the C0 input and Q0 output, reset (R) has precedence. The R input, when High, resets the Q0 output Low during the Low-to-High C0 clock transition. When S is High and R is Low, the Q0 output is set High during the Low-to-High C0 clock transition. For the C1 input and Q1 output, set (S) has precedence.

The flip-flop is asynchronously cleared, output Low, when power is applied.

The INIT attribute does not apply to IFDDRRSE components.

Inputs						Outputs	
C0	C1	CE	D	R	S	Q0	Q1
↑	X	X	X	1	0	0	No Chg
↑	X	X	X	0	1	1	No Chg
↑	X	X	X	1	1	0	No Chg
X	↑	X	X	1	0	No Chg	0
X	↑	X	X	0	1	No Chg	1
X	↑	X	X	1	1	No Chg	0
X	X	0	X	0	0	No Chg	No Chg
↑	X	1	D	0	0	D	No Chg
X	↑	1	D	0	0	No Chg	D

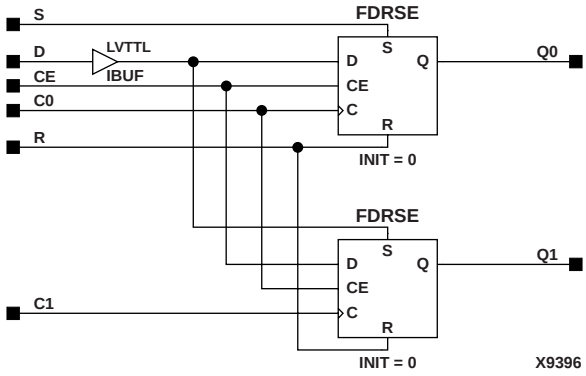
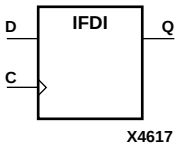


Figure 6-10 IFDDRRSE Implementation Virtex-II, Virtex-II PRO

IFDI

Input D Flip-Flop (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



The IFDI D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

The flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	C	Q
0	↑	0
1	↑	1

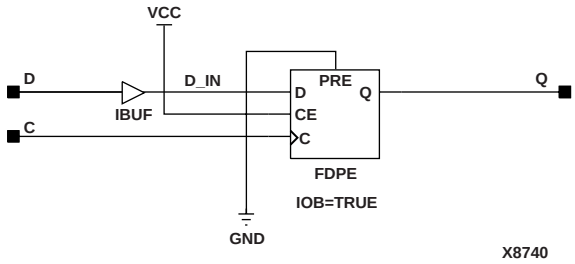


Figure 6-11 IFDI Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

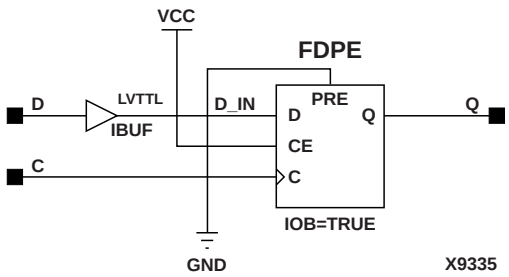
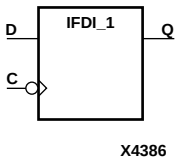


Figure 6-12 IFDI Implementation Virtex-II, Virtex-II PRO

IFDI_1

Input D Flip-Flop with Inverted Clock (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



The IFDI_1 D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

The flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	C	Q
0	↓	0
1	↓	1

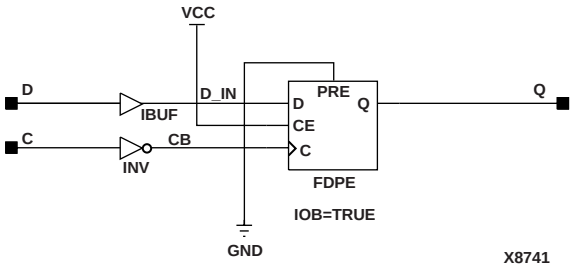


Figure 6-13 IFDI_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

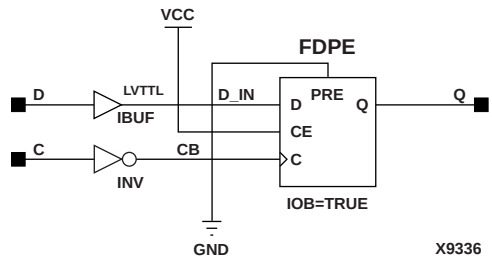
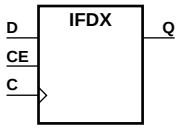


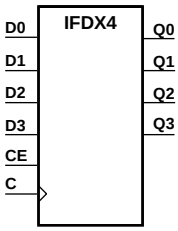
Figure 6-14 IFDI_1 Implementation Virtex-II, Virtex-II PRO

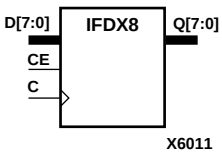
IFDX, 4, 8, 16

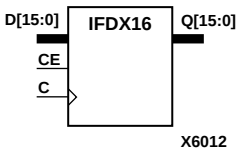
Single- and Multiple-Input D Flip-Flops with Clock Enable

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
IFDX	Macro	Macro	Macro	N/A	N/A	N/A
IFDX4, IFDX8, IFDX16	Macro	Macro	Macro	N/A	N/A	N/A









The IFDX D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

The flip-flops are asynchronously cleared with Low outputs when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CE	Dn	C	Qn
1	Dn	↑	dn
0	X	X	No Chg

dn = state of referenced input (Dn) one setup time prior to active clock transition

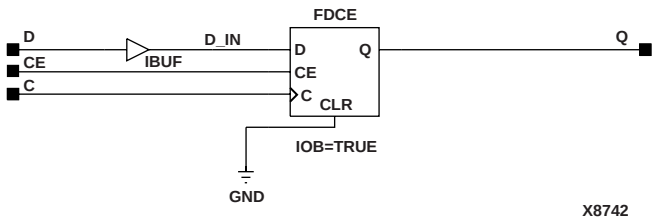


Figure 6-15 IFDX Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

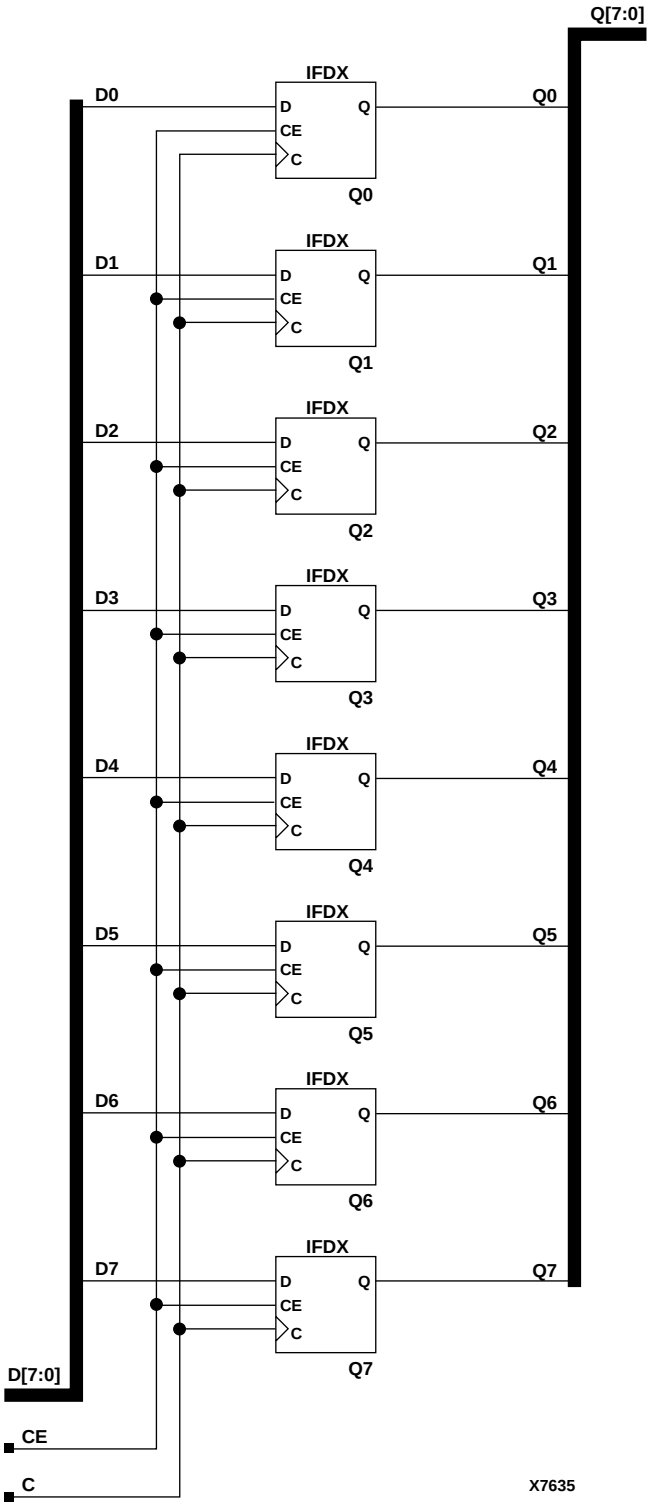
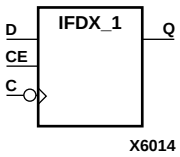


Figure 6-16 IFDX8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

IFDX_1

Input D Flip-Flop with Inverted Clock and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N / A	N / A	N / A



The IFDX_1 D-type flip-flop is contained in an input / output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously cleared with Low output, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

For more information on IFDX_1, see the "ILDX, 4, 8, 16" section.

Inputs			Outputs
CE	D	C	Q
1	D	↓	d
0	X	X	No Chg

d = state of D input one setup time prior to active clock transition

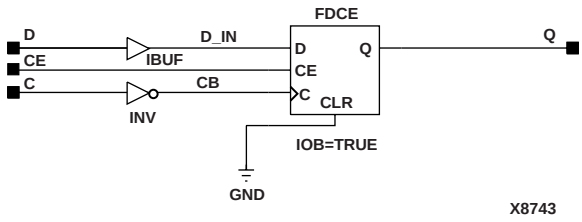


Figure 6-17 IFDX_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

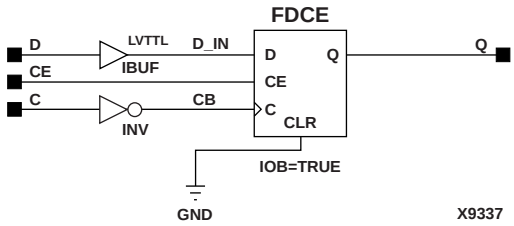
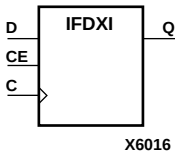


Figure 6-18 IFDX_1 Implementation Virtex-II, Virtex-II PRO

IFDXI

Input D Flip-Flop with Clock Enable (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



The IFDXI D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously preset with High output, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

For information on legal IFDXI, IFDXI_1, ILDXI, and ILDXI_1 combinations, see the "ILDXI" section.

Inputs			Outputs
CE	D	C	Q
1	D	↑	d
0	X	X	No Chg

d = state of D input one setup time prior to active clock transition

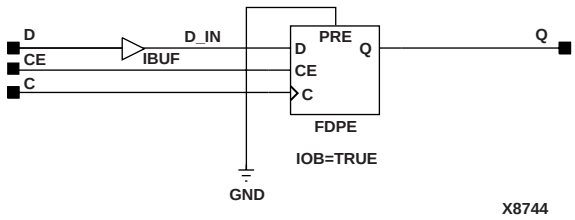


Figure 6-19 IFDXI Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

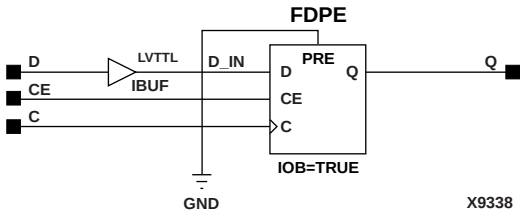
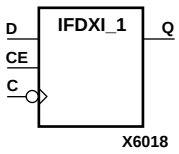


Figure 6-20 IFDXI Implementation Virtex-II, Virtex-II PRO

IFDXI_1

Input D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



The IFDXI_1 D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously preset with High output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

For information on legal IFDXI, IFDXI_1, ILDXI, and ILDXI_1 combinations, see the "ILDXI" section.

Inputs			Outputs
CE	D	C	Q
1	D	↓	d
0	X	X	No Chg

d = state of D input one setup time prior to active clock transition

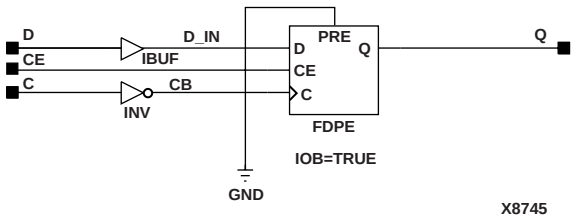


Figure 6-21 IFDXI_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

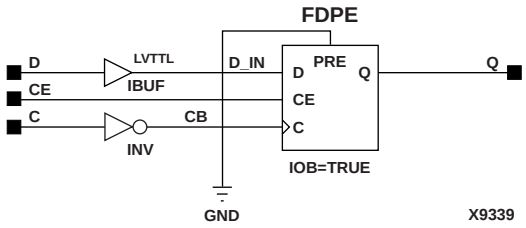
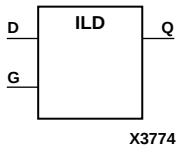


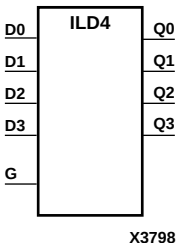
Figure 6-22 IFDXI_1 Implementation Virtex-II, Virtex-II PRO

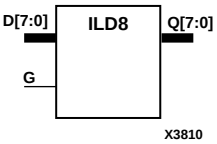
ILD, 4, 8, 16

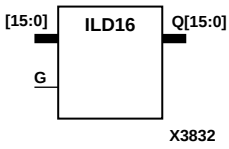
Transparent Input Data Latches

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
ILD	Macro	Macro	Macro	Macro	Macro	Macro
ILD4, ILD8, ILD16	Macro	Macro	Macro	Macro	Macro	Macro









ILD, ILD4, ILD8, and ILD16 are single or multiple transparent data latches, which can be used to hold transient data entering a chip. The ILD latch is contained in an input / output block (IOB), except for XC9500 / XV / XL. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

The latch is asynchronously cleared with Low output when power is applied.

For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
G	D	Q
1	1	1
1	0	0
0	X	d

d = state of referenced input one setup time prior to active G transition

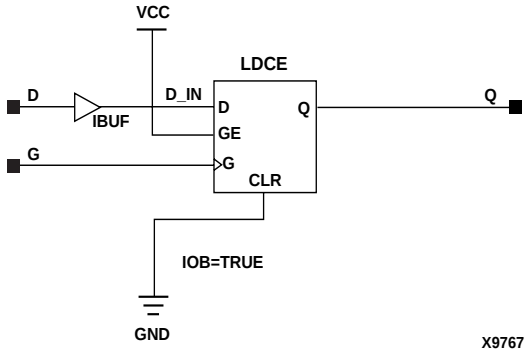


Figure 6-23 ILD Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

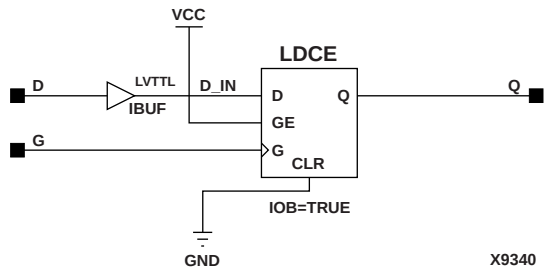


Figure 6-24 ILD Implementation Virtex-II, Virtex-II PRO

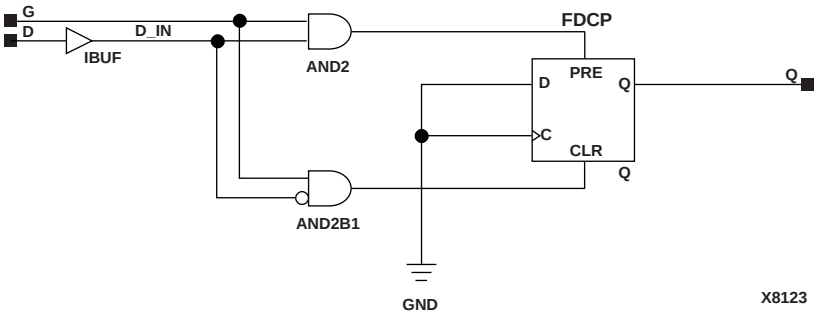


Figure 6-25 ILD Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

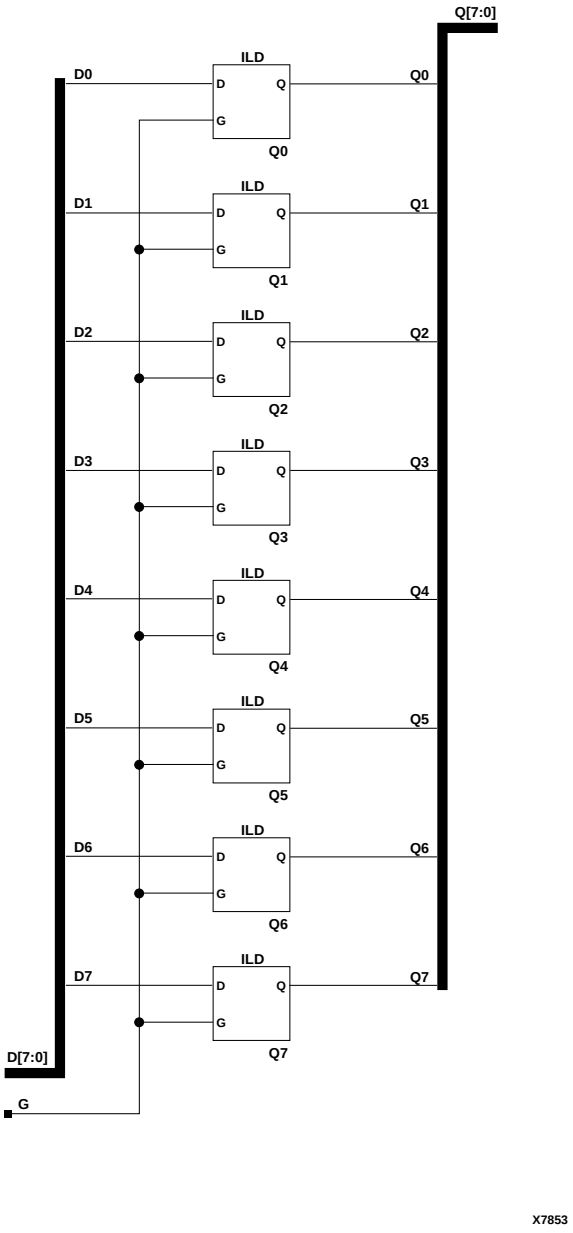
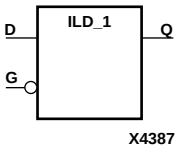


Figure 6-26 ILD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

ILD_1

Transparent Input Data Latch with Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



ILD_1 is a transparent data latch, which can be used to hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
G	D	Q
0	1	1
0	0	0
1	X	d

d = state of referenced input one setup time prior to Low-to-High gate transition

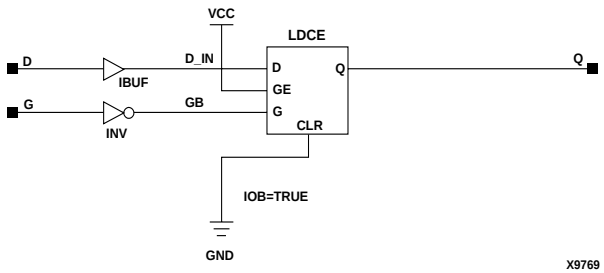


Figure 6-27 ILD_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

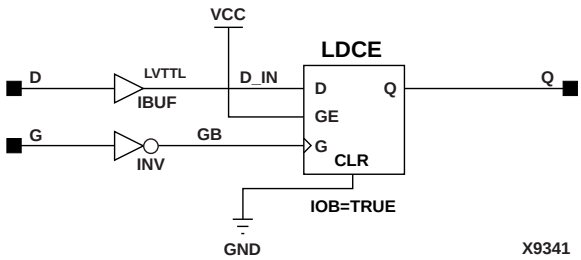
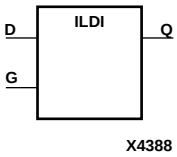


Figure 6-28 ILD_1 Implementation Virtex-II, Virtex-II PRO

ILDI

Transparent Input Data Latch (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



ILDI is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

The latch is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

ILDIs and IFDIs

The ILDI is actually the input flip-flop master latch. It is possible to access two different outputs from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDI) corresponds to a falling edge-triggered flip-flop (IFDI_1). Similarly, a transparent Low latch (ILDI_1) corresponds to a rising edge-triggered flip-flop (IFDI).

Inputs		Outputs
G	D	Q
1	1	1
1	0	0
0	X	d

d = state of referenced input one setup time prior to High-to-Low gate transition

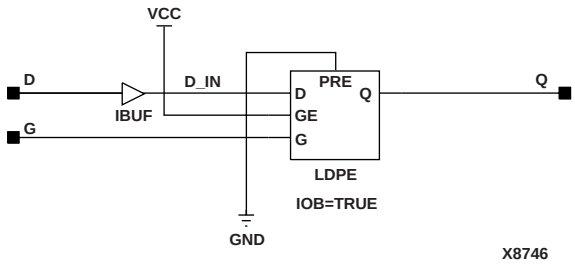


Figure 6-29 ILDI Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

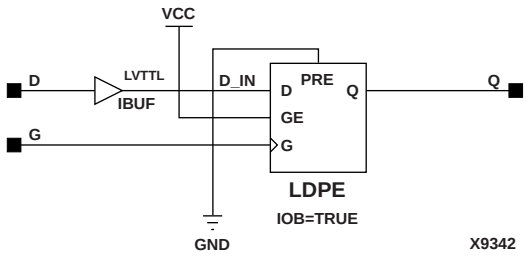
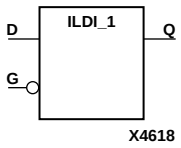


Figure 6-30 ILDI Implementation Virtex-II, Virtex-II PRO

ILDI_1

Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



ILDI_1 is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

For information on ILDI_1, see the "ILDI" section.

Inputs		Outputs
G	D	Q
0	1	1
0	0	0
1	X	d

d = state of input one setup time prior to High-to-Low gate transition

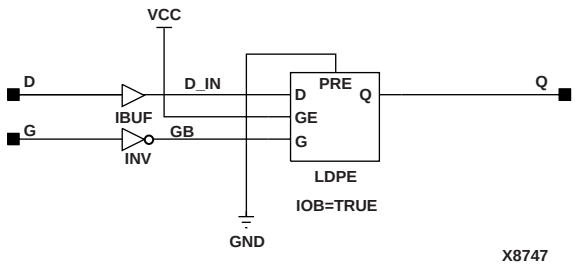


Figure 6-31 ILDI_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

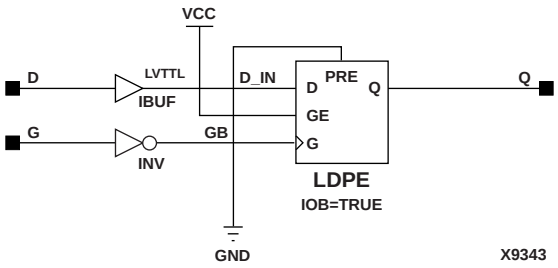
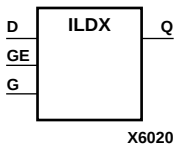


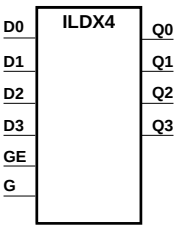
Figure 6-32 ILDI_1 Implementation Virtex-II, Virtex-II PRO

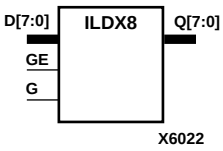
ILDX, 4, 8, 16

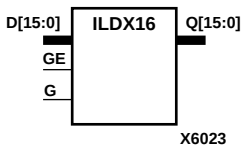
Transparent Input Data Latches

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
ILDX	Macro	Macro	Macro	N/A	N/A	N/A
ILDX4, ILDX8, ILDX16	Macro	Macro	Macro	N/A	N/A	N/A









ILDX, ILDX4, ILDX8, and ILDX16 are single or multiple transparent data latches, which can be used to hold transient data entering a chip. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF).

The latch is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

ILDXs and IFDXs

The ILDX is actually the input flip-flop master latch. Two different outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDX) corresponds to a falling edge-triggered flip-flop (IFDX_1). Similarly, a transparent Low latch (ILDX_1) corresponds to a rising edge-triggered flip-flop (IFDX).

Inputs			Outputs
GE	G	D	Q
0	X	X	No Chg
1	0	X	No Chg
1	1	1	1
1	1	0	0
1	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

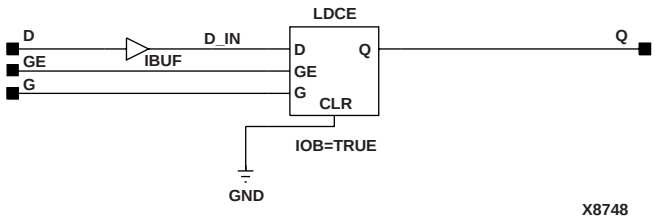


Figure 6-33 ILDX Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

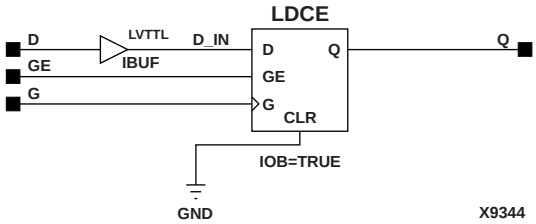


Figure 6-34 ILDX Implementation Virtex-II, Virtex-II PRO

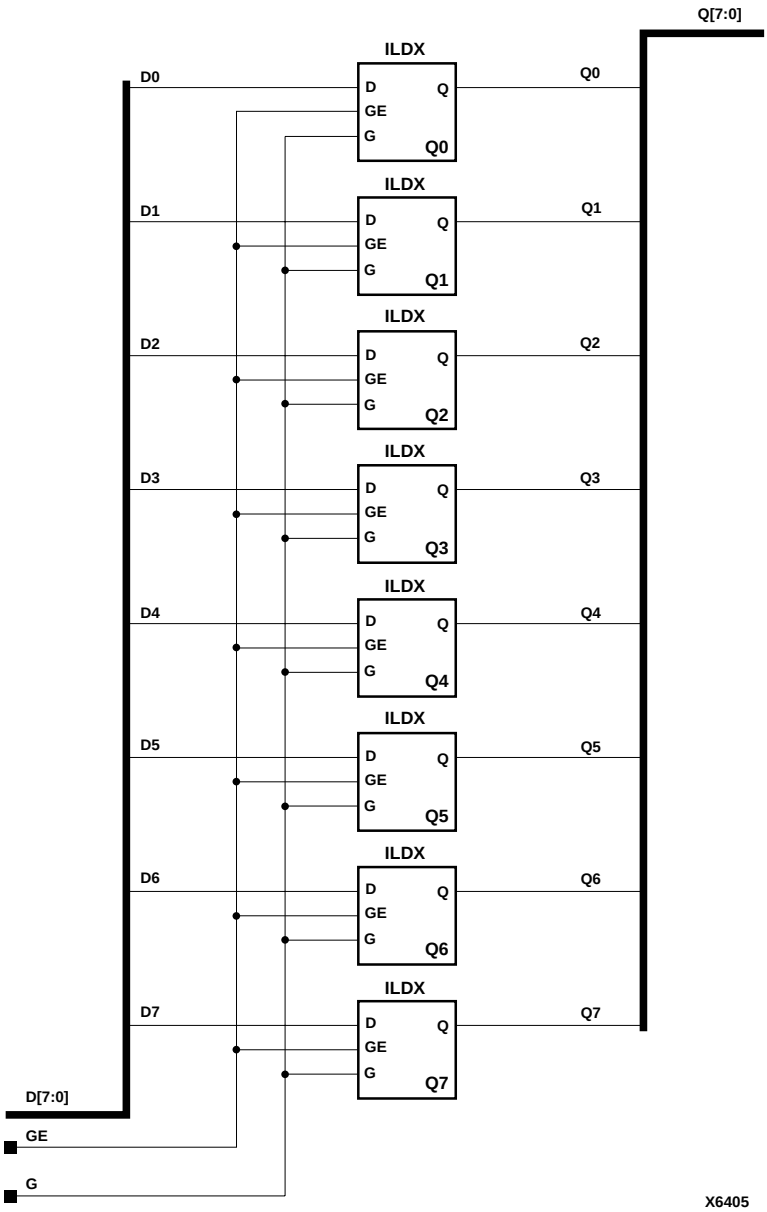
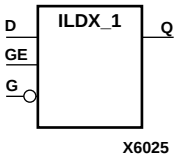


Figure 6-35 ILDX8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

ILDX_1

Transparent Input Data Latch with Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



ILDX_1 is a transparent data latch, which can be used to hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously cleared with Low output, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

For more information on ILDX_1, see the "ILDX, 4, 8, 16" section.

Inputs			Outputs
GE	G	D	Q
0	X	X	No Chg
1	1	X	No Chg
1	0	1	1
1	0	0	0
1	↑	D	d

d = state of input one setup time prior to Low-to-High gate transition

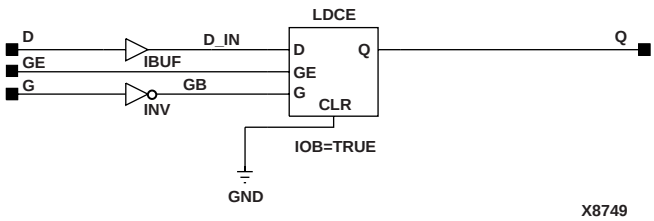


Figure 6-36 ILDX_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

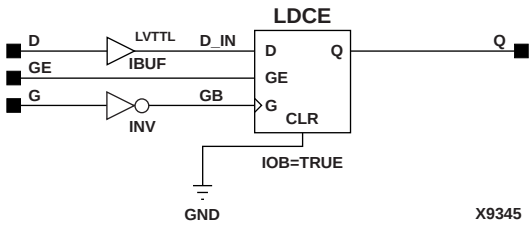
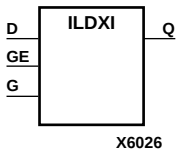


Figure 6-37 ILDX_1 Implementation Virtex-II, Virtex-II PRO

ILDXI

Transparent Input Data Latch (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



ILDXI is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

The latch is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

ILDXIs and IFDXIs

The ILDXI is actually the input flip-flop master latch. Two different outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDXI) corresponds to a falling edge-triggered flip-flop (IFDXI_1). Similarly, a transparent Low latch (ILDXI_1) corresponds to a rising edge-triggered flip-flop (IFDXI). See the following figure for legal IFDXI, IFDXI_1, ILDXI, and ILDXI_1 combinations.

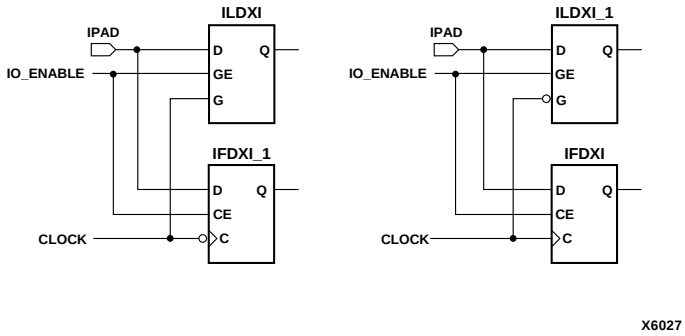


Figure 6-38 Legal Combinations of IFDXI and ILDXI for a Single IOB

Inputs			Outputs
GE	G	D	Q
0	X	X	No Chg
1	0	X	No Chg
1	1	1	1
1	1	0	0

Inputs			Outputs
GE	**G**	**D**	**Q**
1	↓	D	d

d = state of referenced input one setup time prior to High-to-Low gate transition

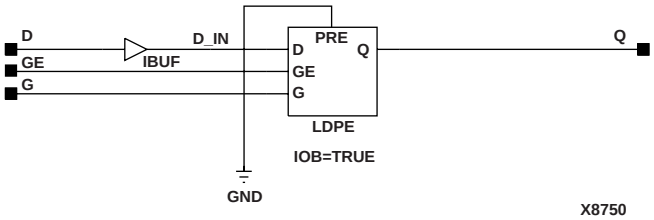


Figure 6-39 ILDXI Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

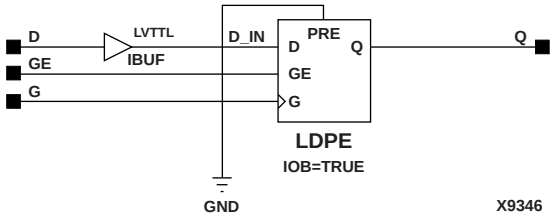
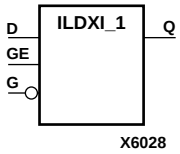


Figure 6-40 ILDXI Implementation Virtex-II, Virtex-II PRO

ILDXI_1

Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



ILDXI_1 is a transparent data latch, which can hold transient data entering a chip. The latch is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

For information on legal IFDXI, IFDXI_1, ILDXI, and ILDXI_1 combinations, see the "ILDXI" section.

Inputs			Outputs
GE	G	D	Q
0	X	X	No Chg
1	1	X	No Chg
1	0	1	1
1	0	0	0
1	↑	D	d

d = state of referenced input one setup time prior to Low-to-High gate transition

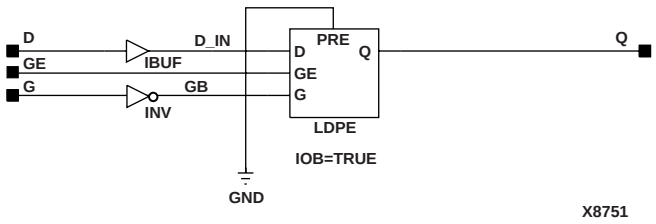


Figure 6-41 ILDXI_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

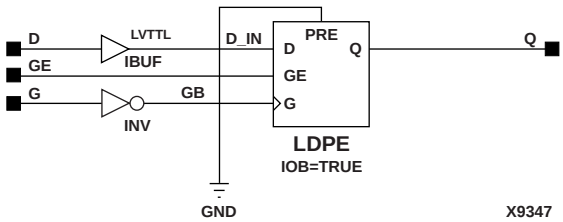
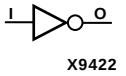


Figure 6-42 ILDXI_1 Implementation Virtex-II, Virtex-II PRO

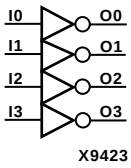
INV, 4, 8, 16

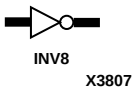
Single and Multiple Inverters

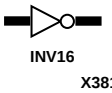
Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
INV	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
INV4, INV8, INV16	Macro	Macro	Macro	Macro	Macro	Macro



INV, INV4, INV8, and INV16 are single and multiple inverters that identify signal inversions in a schematic.







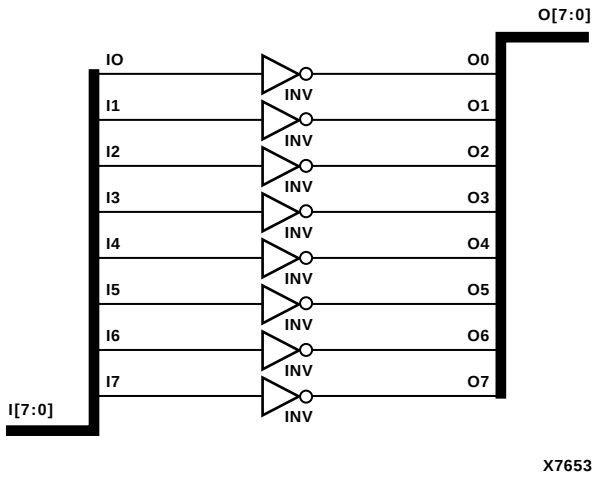
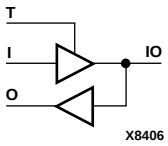


Figure 6-43 INV8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

IOBUF, IOBUF_*selectIO*

Bi-Directional Buffer with Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, IOBUF and its *selectIO* variants (listed in the "Components" column in the table below) are bi-directional buffers whose I/O interface corresponds to a specific I/O standard.The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. The S, F, and 2, 4, 6, 8, 12, 16, 24 extensions specify the slew rate (SLOW or FAST) and the drive power (2, 4, 6, 8, 12, 16, 24 mA) for the LVTTL standard variants. For example, IOBUF_F_2 is a bi-directional buffer that uses the LVTTL I/O-signaling standard with a FAST slew and 2mA of drive power. You can attach an IOSTANDARD attribute to an IOBUF instance instead of using an IOBUF_*selectIO* component. Check marks (√) in the "Spartan-II, Spartan-IIE, Virtex" and "Virtex-E" columns indicate the components and IOSTANDARD attribute values available for each architecture.

IOBUF components that use the LVTTL, LVCMOS15, LVCMOS18, LVCMOS25, LVCMOS33 signaling standards have selectable drive and slew rates using the DRIVE and FAST or SLOW constraints. The defaults are DRIVE=12 mA and SLOW slew.

IOBUFs are composites of IBUF and OBUFT elements. The O output is X (unknown) when IO (input/output) is Z. IOBUFs can be implemented as interconnections of their component elements.

The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffers. See the "SelectI/O Usage Rules" under the IBUF_*selectIO* section for information on using these components and IOSTANDARD attributes.

Table 6-8 Spartan-II, Spartan-IIE, Virtex, and Virtex-E IOBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II, Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Output VCCO	Input VCCO	VREF
IOBUF	√	√	defaults to LVTTL [b]	3.3	3.3	N/A
IOBUF_S_2	√	√	LVTTL [b]	3.3	3.3	N/A
IOBUF_S_4	√	√	LVTTL [b]	3.3	3.3	N/A
IOBUF_S_6	√	√	LVTTL [b]	3.3	3.3	N/A
IOBUF_S_8	√	√	LVTTL [b]	3.3	3.3	N/A
IOBUF_S_12	√	√	LVTTL [b]	3.3	3.3	N/A
IOBUF_S_16	√	√	LVTTL [b]	3.3	3.3	N/A
IOBUF_S_24	√	√	LVTTL [b]	3.3	3.3	N/A
IOBUF_F_2	√	√	LVTTL [b]	3.3	3.3	N/A

Table 6-8 Spartan-II, Spartan-IIE, Virtex, and Virtex-E IOBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II, Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Output VCCO	Input VCCO	VREF
IOBUF_F_4	√	√	LVTTL [b]	3.3	3.3	N / A
IOBUF_F_6	√	√	LVTTL [b]	3.3	3.3	N / A
IOBUF_F_8	√	√	LVTTL [b]	3.3	3.3	N / A
IOBUF_F_12	√	√	LVTTL [b]	3.3	3.3	N / A
IOBUF_F_16	√	√	LVTTL [b]	3.3	3.3	N / A
IOBUF_F_24	√	√	LVTTL [b]	3.3	3.3	N / A
IOBUF_AGP	√	√	AGP	3.3	N / A	1.32
IOBUF_CTT	√	√	CTT	3.3	N / A	1.50
IOBUF_GTL	√	√	GTL	N / A	N / A	0.80
IOBUF_HSTL_I	√	√	HSTL_I	1.5	N / A	0.75
IOBUF_HSTL_III	√	√	HSTL_III	1.5	1.5	0.90
IOBUF_HSTL_IV	√	√	HSTL_IV	1.5	N / A	0.90
IOBUF_LVCMOS2	√		LVCMOS2	2.5	2.5	N / A
IOBUF_LVCMOS18		√	LVCMOS18 [b]	1.8	1.8	N / A
IOBUF_LVDS		√	LVDS	2.5	N / A	N / A
IOBUF_LVPECL		√	LVPECL	3.3	N / A	N / A
IOBUF_PCI33_3	√	√	PCI33_3	3.3	3.3	N / A
IOBUF_PCI33_5	√	√	PCI33_5	3.3	N / A	N / A
IOBUF_PCI66_3, PCIX66_3	√	√	PCI66_3, PCIX66_3	3.3	3.3	N / A
IOBUF_SSTL2_I	√	√	SSTL2_I	2.5	N / A	1.25
IOBUF_SSTL2_II	√	√	SSTL2_II	2.5	N / A	1.25
IOBUF_SSTL3_I	√	√	SSTL3_I	3.3	N / A	1.50
IOBUF_SSTL3_II	√	√	SSTL3_II	3.3	N / A	1.50

[b] The LVTTL, LVCMOS15, and LVCMOS18 attributes also require a slew value (FAST or SLOW) and DRIVE value. See the FAST, SLOW, and DRIVE attribute descriptions in the *Xilinx Constraints Guide* for valid values for each architecture.

The Virtex-II and Virtex-II PRO library includes some IOBUF_*selectIO* components for compatibility with older, existing designs and other architectures. For new Virtex-II and Virtex-II PRO designs, however, the recommended method for using IOBUF selectI/O buffers is to attach an IOSTANDARD attribute to an IOBUF component. For example, attach IOSTANDARD=GTLP to an IOBUF instead of using the IOBUF_GTLP component for new Virtex-II and Virtex-II PRO designs. The IOSTANDARD attributes that can be attached to an IOBUF component are listed in the "IOSTANDARD (Attribute Value)" column in <$elemparanum. See the "SelectI/O Usage Rules" section for information on using these IOSTANDARD attributes.

For Virtex-II and Virtex-II PRO, the IOSTANDARD attribute values listed in the following table can be applied to an IOBUFDS component to provide SelectI/O interface capability for the inputs. The O output uses the LVTTL standard.

Table 6-9 Virtex-II, Virtex-II PRO IOBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Input VCCO	VREF	Terminate Type
IOBUF[a]	√	AGP*	3.3	N / A	1.32	None
		*does not apply to Virtex-II PRO				
IOBUF[a]	√	F_12	3.3	3.3	N / A	None
IOBUF[a]	√	F_16	3.3	3.3	N / A	None
IOBUF[a]	√	F_2	3.3	3.3	N / A	None
IOBUF[a]	√	F_24	3.3	3.3	N / A	None
IOBUF[a]	√	F_4	3.3	3.3	N / A	None
IOBUF[a]	√	F_6	3.3	3.3	N / A	None
IOBUF[a]	√	F_8	3.3	3.3	N / A	None
IOBUF[a]	√	GTL	N / A	N / A	0.80	None
IOBUF[a]	√	GTL_DCI	1.2	1.2	0.80	Single
IOBUF[a]	√	GTLP	N / A	N / A	1.00	None
IOBUF[a]	√	GTLP_DCI	1.5	1.5	1.00	Single
IOBUF[a]	√	HSTL_I	1.5	1.5	0.75	Split
IOBUF[a]	√	HSTL_I_18	1.8	1.5	0.75	Split
IOBUF[a]	√	HSTL_II	1.5	N / A	0.75	None
IOBUF[a]	√	HSTL_II_18	1.8	1.5	0.75	Split
IOBUF[a]	√	HSTL_II_DCI	1.5	1.5	0.75	Split
IOBUF[a]	√	HSTL_II_DCI_18	1.8	1.5	0.75	Split
IOBUF[a]	√	HSTL_III	1.5	N / A	0.75	None
IOBUF[a]	√	HSTL_III_18	1.8	N / A	0.75	None
IOBUF[a]	√	HSTL_IV	1.5	N / A	0.90	None
IOBUF[a]	√	HSTL_IV_18	1.8	N / A	0.90	None
IOBUF[a]	√	HSTL_IV_DCI	1.5	1.5	0.90	Split
IOBUF[a]	√	HSTL_IV_DCI_18	1.8	1.5	0.90	Split
IOBUF [a]	√	LVCMOS15 [b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS2[b]	2.5	2.5	N / A	None
IOBUF [a]	√	LVCMOS15_F_12 [b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_F_16[b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_F_2 [b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_F_4[b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_F_6[b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_F_8[b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_S_12 [b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_S_16[b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_S_2 [b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_S_4[b]	1.5	1.5	N / A	None
IOBUF [a]	√	LVCMOS15_S_6[b]	1.5	1.5	N / A	None

Table 6-9 Virtex-II, Virtex-II PRO IOBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Input VCCO	VREF	Terminate Type
IOBUF [a]	√	LVCMOS15_S_8[b]	1.5	1.5	N/A	None
IOBUF[a]	√	LVCMOS18 [b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _F_12[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _F_16[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _F_2[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _F_4[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _F_6[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _F_8[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _S_12[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _S_16[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _S_2[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _S_4[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _S_6[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS18 _S_8[b]	1.8	1.8	N/A	None
IOBUF[a]	√	LVCMOS2 [b]	2.0	2.0	N/A	None
IOBUF[a]	√	LVCMOS25 [b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _F_12[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _F_16[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _F_2[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _F_24[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _F_4[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _F_6[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _F_8[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _S_12[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _S_16[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _S_2[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _S_24[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _S_4[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _S_6[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS25 _S_8[b]	2.5	2.5	N/A	None
IOBUF[a]	√	LVCMOS33 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _F_12[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _F_16[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _F_2[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _F_24[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _F_4[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _F_6[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _F_8[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _S_12[b]	3.3	3.3	N/A	None

Table 6-9 Virtex-II, Virtex-II PRO IOBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Input VCCO	VREF	Terminate Type
IOBUF[a]	√	LVCMOS33 _S_16[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _S_2[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _S_24[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _S_4[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _S_6[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVCMOS33 _S_8[b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVDCI_15	1.5	N/A	N/A	Driver
IOBUF[a]	√	LVDCI_18	1.8	N/A	N/A	Driver
IOBUF[a]	√	LVDCI_25	2.5	N/A	N/A	Driver
IOBUF[a]	√	LVDCI_33	3.3	N/A	N/A	Driver
IOBUF[a]	√	LVDCI_DV2_15	1.5	N/A	N/A	Driver
IOBUF[a]	√	LVDCI_DV2_18	1.8	N/A	N/A	Driver
IOBUF[a]	√	LVDCI_DV2_25	2.5	N/A	N/A	Driver
IOBUF[a]	√	LVDCI_DV2_33	3.3	N/A	N/A	Driver
IOBUF[a]	√	LVTTL (default) [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_33 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_F_12 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_F_16 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_F_2 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_F_24 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_F_4 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_F_6 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_F_8 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_S_12 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_S_16 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_S_2 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_S_24 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_S_4 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_S_6 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	LVTTL_S_8 [b]	3.3	3.3	N/A	None
IOBUF[a]	√	PCI33_3	3.3	3.3	N/A	None
IOBUF[a]	√	PCI66_3	3.3	3.3	N/A	None
IOBUF[a]	√	PCIX	3.3	3.3	N/A	None
IOBUF[a]	√	SSTL2_II_DCI	2.5	2.5	1.25	Split
IOBUF[a]	√	SSTL3_II_DCI	2.5	3.3	1.25	Split
IOBUF[a]	√	SSTL2_I	2.5	N/A	1.25	None
IOBUF[a]	√	SSTL2_II	2.5	N/A	1.25	None
IOBUF[a]	√	SSTL3_I	3.3	N/A	1.50	None
IOBUF[a]	√	SSTL3_II	3.3	N/A	1.50	None

Table 6-9 Virtex-II, Virtex-II PRO IOBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Input VCCO	VREF	Terminate Type
IOBUF[a]	√	S_12	3.3	3.3	N/A	None
IOBUF[a]	√	S_16	3.3	3.3	N/A	None
IOBUF[a]	√	S_2	3.3	3.3	N/A	None
IOBUF[a]	√	S_24	3.3	3.3	N/A	None
IOBUF[a]	√	S_4	3.3	3.3	N/A	None
IOBUF[a]	√	S_6	3.3	3.3	N/A	None
IOBUF[a]	√	S_8	3.3	3.3	N/A	None

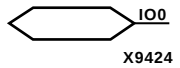
[a]Attach an IOSTANDARD attribute to an IOBUF and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the input for the I/O standard associated with that value.

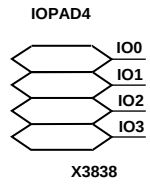
[b] The LVTTL, LVCMOS15, LVCMOS18, LVCMOS25, LVCMOS33 attributes also require a slew value (FAST or SLOW) and DRIVE value. See the FAST, SLOW, and DRIVE attribute descriptions in the *Xilinx Constraints Guide* for valid values for Virtex-II.

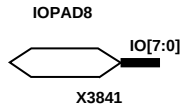
IOPAD, 4, 8, 16

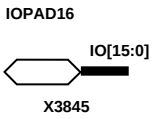
Single- and Multiple-Input/Output Pads

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
IOPAD	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IOPAD4, IOPAD8, IOPAD16	Macro	Macro	Macro	Macro	Macro	Macro









IOPAD, IOPAD4, IOPAD8, and IOPAD16 are single and multiple input/output pads. The IOPAD is a connection point from a device pin, used as a bidirectional signal, to a PLD device. The IOPAD is connected internally to an input/output block (IOB), which is configured by the software as a bidirectional block. Bidirectional blocks can consist of any combinations of a 3-state output buffer (such as OBUFT or OFDE) and any available input buffer (such as IBUF or IFD). See the appropriate CAE tool interface user guide for details on assigning pin location and identification.

Note The LOC attribute cannot be used on IOPAD multiples.

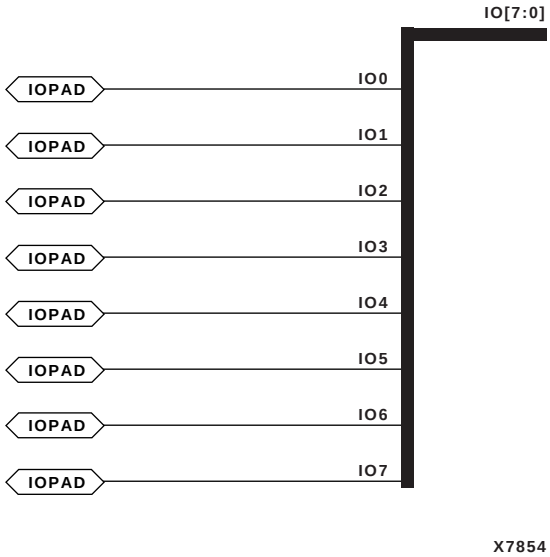
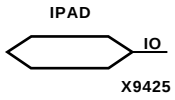


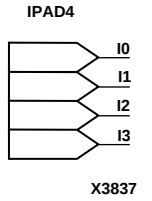
Figure 6-44 IOPAD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

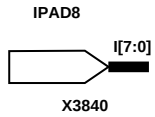
IPAD, 4, 8, 16

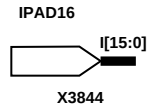
Single- and Multiple-Input Pads

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
IPAD	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IPAD4, IPAD8, IPAD16	Macro	Macro	Macro	Macro	Macro	Macro









IPAD, IPAD4, IPAD8, and IPAD16 are single and multiple input pads. The IPAD is a connection point from a device pin used for an input signal to the PLD device. It is connected internally to an input/output block (IOB), which is configured by the software as an IBUF, IFD, or ILD. See the appropriate CAE tool interface user guide for details on assigning pin location and identification.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, pads must be used to drive IBUF and IBUFG inputs. An IPAD can be inferred by NGDBUILD if one is missing on an IBUF or IBUFG input.

Note The LOC attribute cannot be used on IPAD multiples.

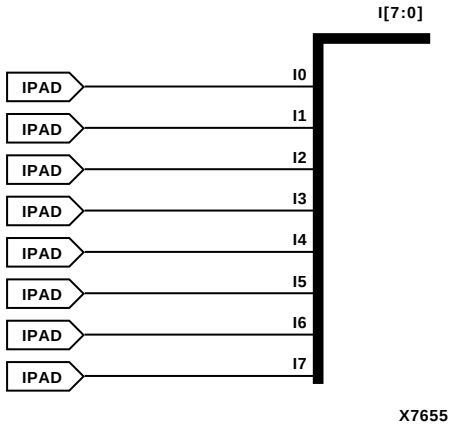


Figure 6-45 IPAD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

JTAGPPC

JTAG Primitive for the Power PC

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO*	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

* Not supported for Virtex-II. Only supported for Virtex-II PRO.

The JTAGPPC block allows connection from the JTAG logic in the PPC405 core to the JTAG logic of the Virtex-II PRO device. The connections are made through programmable routing and so the connection only exists after configuration. Following is an example instantiation of the JTAGPPC block in Verilog:

```
JTAGPPC IJTAGPPC(.TDOTSPPC(TDO_TS_PPC),
.TDOPPC(TDO_PPC),.TMS(TMS_PPC),
.TDIPPC(TDI_PPC), .TCK(TCK_PPC));

PPC405 IPPC405 (
 ...
.JTGC405TCK   (TCK_PPC),
.JTGC405TDI   (TDI_PPC),
.JTGC405TMS   (TMS_PPC),
.C405JTGTDO   (TDO_PPC),
.C405JTGTDOEN (TDO_TS_PPC),
...
)
```

When the block is instantiated in this fashion, the instruction registers of the PPC405 and the Virtex-II PRO device are linked in series.

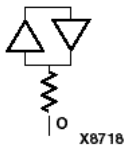
The following table lists the input and output pins for JTAGPPC.

Inputs	Outputs
TDOPPC	TCK
TDOTPPC	TDIPPC
	TMS

KEEPER

KEEPER Symbol

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



KEEPER is a weak keeper element used to retain the value of the net connected to its bidirectional O pin. For example, if a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the net.

For additional information on using a KEEPER element with SelectI/O components, see the "SelectI/O Usage Rules" in the "IBUF_*selectIO*" section

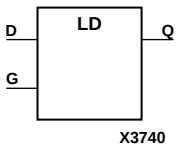
Chapter 7

LD to NOR12, 16

LD

Transparent Data Latch

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Primitive	Primitive



LD is a transparent data latch. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
G	D	Q
1	0	0
1	1	1
0	X	No Chg
↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

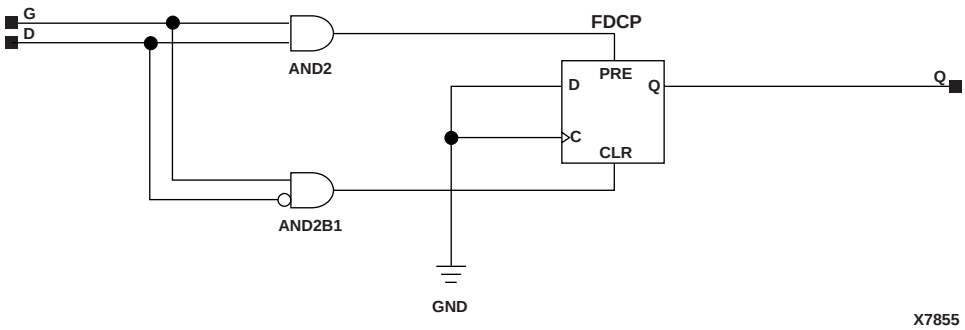
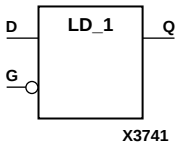


Figure 7-1 LD Implementation XC9500/XV/XL

LD_1

Transparent Data Latch with Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LD_1 is a transparent data latch with an inverted gate. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

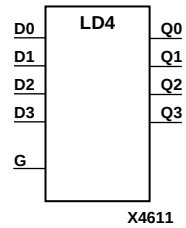
Inputs		Outputs
G	D	Q
0	0	0
0	1	1
1	X	No Chg
↑	D	d

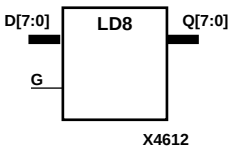
d = state of input one setup time prior to Low-to-High gate transition

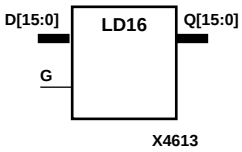
LD4, 8, 16

Multiple Transparent Data Latches

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







LD4, LD8, and LD16 have, respectively, 4, 8, and 16 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously cleared, output Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

See the "LD" section for information on single transparent data latches.

Inputs		Outputs
G	D	Q
1	0	0
1	1	1
0	X	No Chg
↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

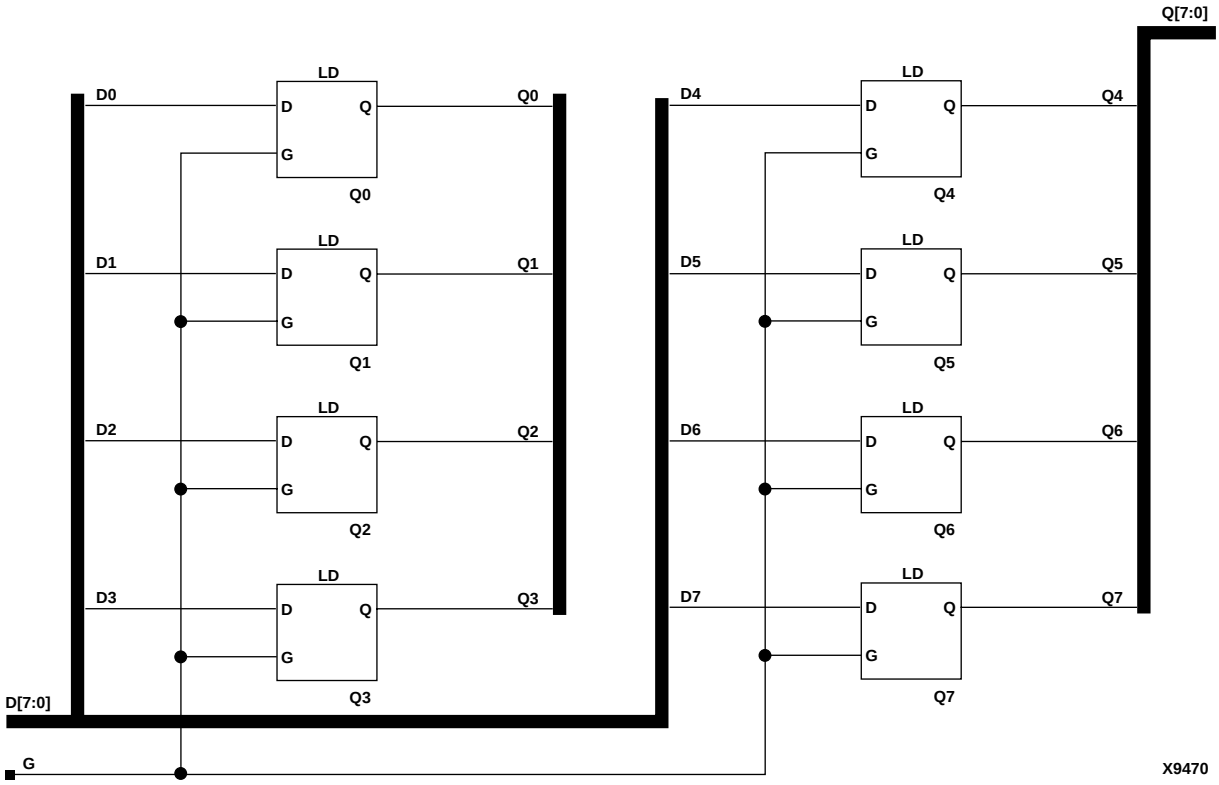
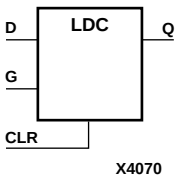


Figure 7-2 LD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

LDC

Transparent Data Latch with Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Primitive	Primitive



LDC is a transparent data latch with asynchronous clear. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate enable (G) input is High and CLR is Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains low.

The latch is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

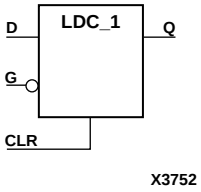
Inputs			Outputs
CLR	G	D	Q
1	X	X	0
0	1	0	0
0	1	1	1
0	0	X	No Chg
0	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

LDC_1

Transparent Data Latch with Asynchronous Clear and Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDC_1 is a transparent data latch with asynchronous clear and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs (D and G) and resets the data (Q) output Low. Q reflects the data (D) input while the gate enable (G) input and CLR are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

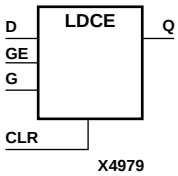
Inputs			Outputs
CLR	G	D	Q
1	X	X	0
0	0	0	0
0	0	1	1
0	1	X	No Chg
0	↑	D	d

d = state of input one setup time prior to Low-to-High gate transition

LDCE

Transparent Data Latch with Asynchronous Clear and Gate Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDCE is a transparent data latch with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR is Low. If GE is Low, data on D cannot be latched. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remains low.

The latch is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

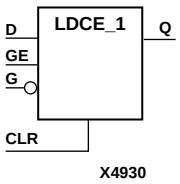
Inputs				Outputs
CLR	GE	G	D	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	1	0	0
0	1	1	1	1
0	1	0	X	No Chg
0	1	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

LDCE_1

Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDCE_1 is a transparent data latch with asynchronous clear, gate enable, and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and CLR are Low and gate enable (GE) is High. If GE is Low, the data on D cannot be latched. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High or GE remains Low.

The latch is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

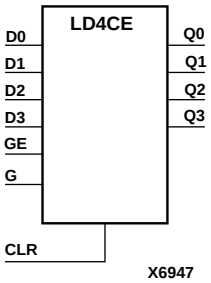
Inputs				Outputs
CLR	GE	G	D	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	0	0	0
0	1	0	1	1
0	1	1	X	No Chg
0	1	↑	D	d

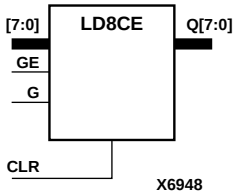
d = state of input one setup time prior to Low-to-High gate transition

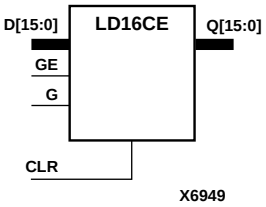
LD4CE, LD8CE, LD16CE

Transparent Data Latches with Asynchronous Clear and Gate Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A







LD4CE, LD8CE, and LD16CE have, respectively, 4, 8, and 16 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. Q reflects the data (D) inputs while the gate (G) input is High, gate enable (GE) is High, and CLR is Low. If GE is Low, data on D cannot be latched. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as GE remains Low.

The latch is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs
CLR	GE	G	Dn	Qn
1	X	X	X	0
0	0	X	X	No Chg
0	1	1	1	1
0	1	1	0	0
0	1	0	X	No Chg
0	1	↓	Dn	dn

Dn = referenced input, for example, D0, D1, D2

Qn = referenced output, for example, Q0, Q1, Q2

dn = referenced input state, one setup time prior to High-to-Low gate transition

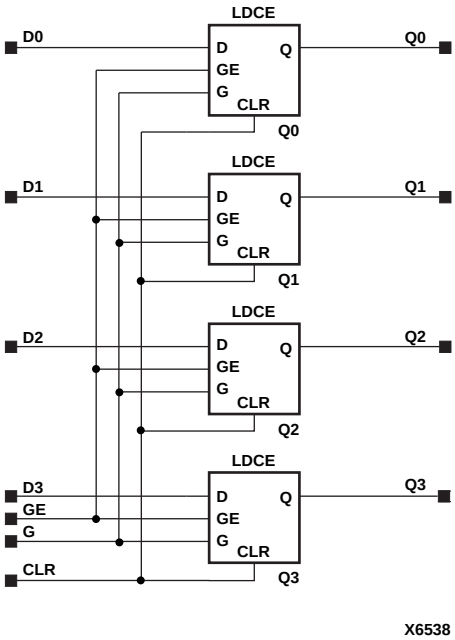


Figure 7-3 LD4CE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

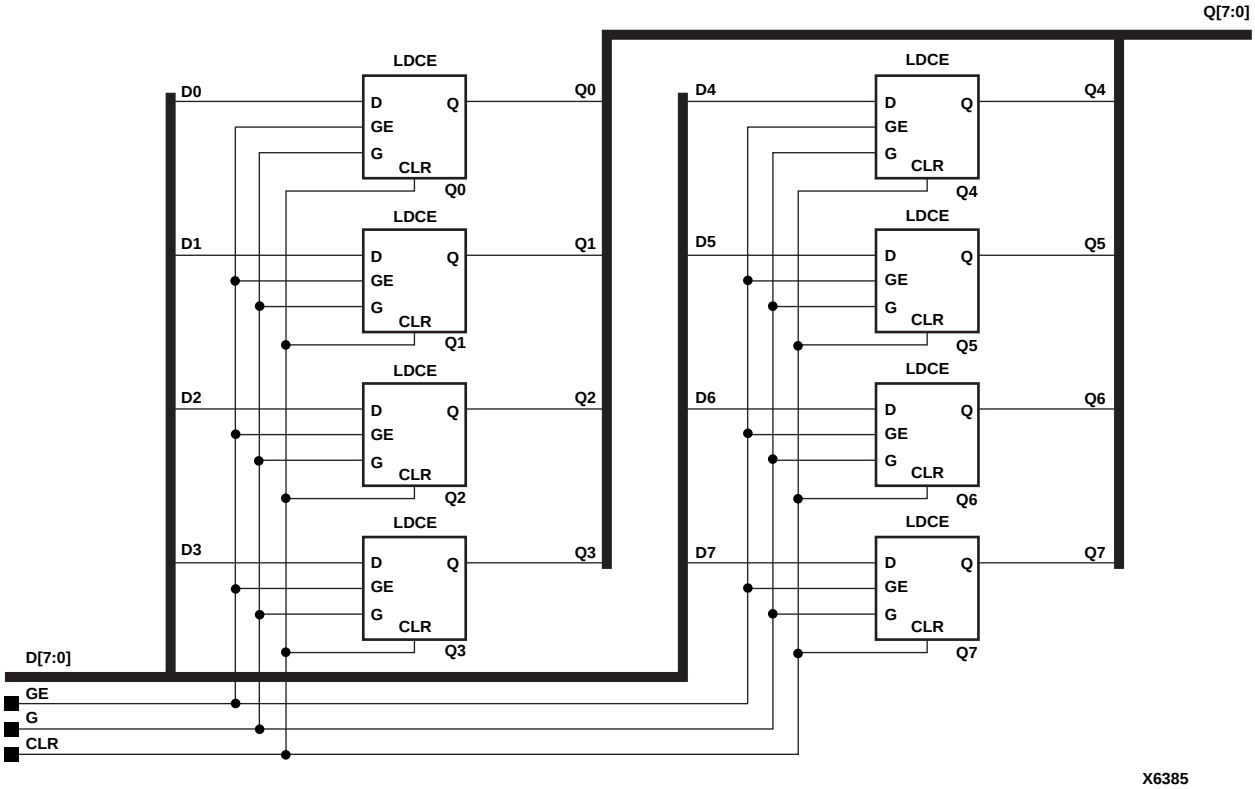
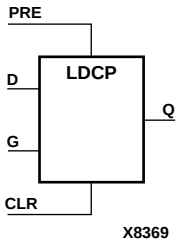


Figure 7-4 LD8CE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

LDCP

Transparent Data Latch with Asynchronous Clear and Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Primitive	Primitive



LDCP is a transparent data latch with data (D), asynchronous clear (CLR) and preset (PRE) inputs. When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is low, it presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input is High and CLR and PRE are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

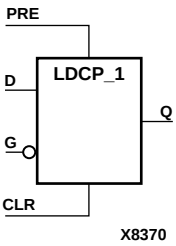
Inputs				Outputs
CLR	PRE	G	D	Q
1	X	X	X	0
0	1	X	X	1
0	0	1	1	1
0	0	1	0	0
0	0	0	X	No Chg
0	0	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

LDCP_1

Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDCP_1 is a transparent data latch with data (D), asynchronous clear (CLR) and preset (PRE) inputs. When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is Low, it presets the data (Q) output High. Q reflects the data (D) input while gate (G) input, CLR, and PRE are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

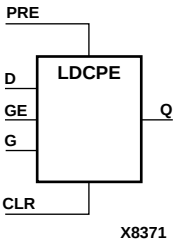
Inputs				Outputs
CLR	PRE	G	D	Q
1	X	X	X	0
0	1	X	X	1
0	0	0	1	1
0	0	0	0	0
0	0	1	X	No Chg
0	0	↑	D	d

d = state of input one setup time prior to Low-to-High gate transition

LDCPE

Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDCPE is a transparent data latch with data (D), asynchronous clear (CLR), asynchronous preset (PRE), and gate enable (GE). When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is Low, it presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR and PRE are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remains Low.

The latch is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

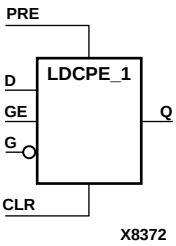
Inputs					Outputs
CLR	PRE	GE	G	D	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	1	0	0
0	0	1	1	1	1
0	0	1	0	X	No Chg
0	0	1	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

LDCPE_1

Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDCPE_1 is a transparent data latch with data (D), asynchronous clear (CLR), asynchronous preset (PRE), and gate enable (GE). When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is Low, it presets the data (Q) output High. Q reflects the data (D) input while gate enable (GE) is High and gate (G), CLR, and PRE are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G is High or GE is Low.

The latch is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

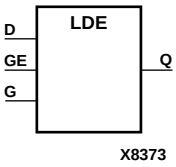
Inputs					Outputs
CLR	PRE	GE	G	D	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	X	No Chg
0	0	1	↑	D	d

d = state of input one setup time prior to Low-to-High gate transition

LDE

Transparent Data Latch with Gate Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDE is a transparent data latch with data (D) and gate enable (GE) inputs. Output Q reflects the data (D) while the gate (G) input and gate enable (GE) are High. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remains Low.

The latch is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

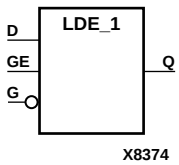
Inputs			Outputs
GE	G	D	Q
0	X	X	No Chg
1	1	0	0
1	1	1	1
1	0	X	No Chg
1	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

LDE_1

Transparent Data Latch with Gate Enable and Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDE_1 is a transparent data latch with data (D) and gate enable (GE) inputs. Output Q reflects the data (D) while the gate (G) input is Low and gate enable (GE) is High. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G is High or GE is Low.

The latch is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

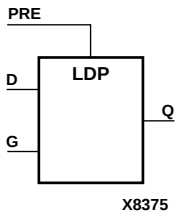
GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
GE	G	D	Q
0	X	X	No Chg
1	0	0	0
1	0	1	1
1	1	X	No Chg
1	↑	D	d
d = state of input one setup time prior to Low-to-High gate transition			

LDP

Transparent Data Latch with Asynchronous Preset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Macro	Primitive	Primitive



LDP is a transparent data latch with asynchronous preset (PRE). When the PRE input is High, it overrides the other inputs and resets the data (Q) output High. Q reflects the data (D) input while gate (G) input is High and PRE is Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

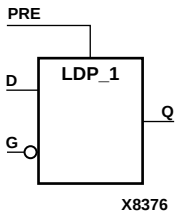
Inputs			Outputs
PRE	G	D	Q
1	X	X	1
0	1	0	0
0	1	1	1
0	0	X	No Chg
0	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

LDP_1

Transparent Data Latch with Asynchronous Preset and Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDP_1 is a transparent data latch with asynchronous preset (PRE). When the PRE input is High, it overrides the other inputs and resets the data (Q) output High. Q reflects the data (D) input while gate (G) input and PRE are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

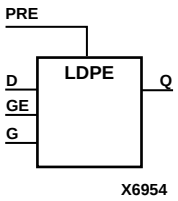
Inputs			Outputs
PRE	G	D	Q
1	X	X	1
0	0	0	0
0	0	1	1
0	1	X	No Chg
0	↑	D	d

d = state of input one setup time prior to Low-to-High gate transition

LDPE

Transparent Data Latch with Asynchronous Preset and Gate Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDPE is a transparent data latch with asynchronous preset and gate enable. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High. If GE is Low, data on D cannot be latched. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remains Low.

The latch is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

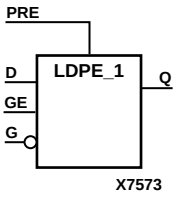
Inputs				Outputs
PRE	GE	G	D	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	1	0	0
0	1	1	1	1
0	1	0	X	No Chg
0	1	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

LDPE_1

Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



LDPE_1 is a transparent data latch with asynchronous preset, gate enable, and inverted gated. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input is Low and gate enable (GE) is High.

If GE is low, data on D cannot be latched. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High or GE remains Low.

The latch is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

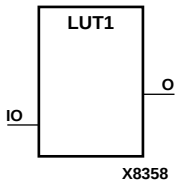
Inputs				Outputs
PRE	GE	G	D	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	0	0	0
0	1	0	1	1
0	1	1	X	No Chg
0	1	↑	D	d

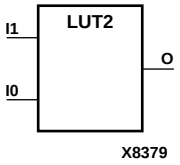
d = state of input one setup time prior to Low-to-High gate transition

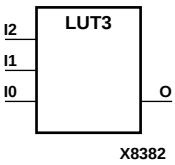
LUT1, 2, 3, 4

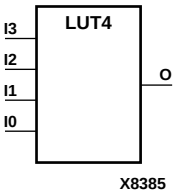
1-, 2-, 3-, 4-Bit Look-Up-Table with General Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A









LUT1, LUT2, LUT3, and LUT4 are, respectively, 1-, 2-, 3-, and 4-bit look-up-tables (LUTs) with general output (O).

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

LUT1 provides a look-up-table version of a buffer or inverter.

LUTs are the basic Virtex, Virtex-E, Virtex-II, Virtex-II PRO, Spartan-II, and Spartan-IIE building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. The variants, "LUT1_D, LUT2_D, LUT3_D, LUT4_D" and "LUT1_L, LUT2_L, LUT3_L, LUT4_L" provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Table 7-1 LUT3 Function Table

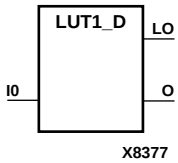
Inputs			Outputs
I2	I1	I0	O
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]

INIT = binary equivalent of the hexadecimal number assigned to the INIT attribute

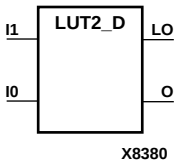
LUT1_D, LUT2_D, LUT3_D, LUT4_D

1-, 2-, 3-, 4-Bit Look-Up-Table with Dual Output

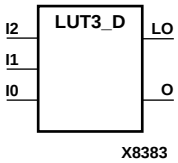
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



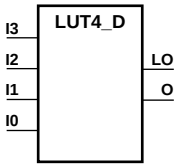
X8377



X8380



X8383



X8386

LUT1_D, LUT2_D, LUT3_D, and LUT4_D are, respectively, 1-, 2-, 3-, and 4-bit look-up-tables (LUTs) with two functionally identical outputs, O and LO. The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

LUT1_D provides a look-up-table version of a buffer or inverter.

See also "LUT1, 2, 3, 4" and "LUT1_L, LUT2_L, LUT3_L, LUT4_L."

Table 7-2 LUT3_D Function Table

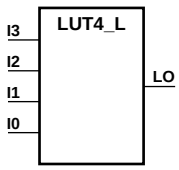
Inputs			Outputs	
I2	I1	I0	O	LO
0	0	0	INIT[0]	INIT[0]
0	0	1	INIT[1]	INIT[1]
0	1	0	INIT[2]	INIT[2]
0	1	1	INIT[3]	INIT[3]
1	0	0	INIT[4]	INIT[4]
1	0	1	INIT[5]	INIT[5]
1	1	0	INIT[6]	INIT[6]
1	1	1	INIT[7]	INIT[7]

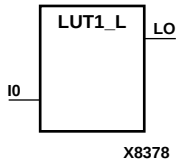
INIT = binary equivalent of the hexadecimal number assigned to the INIT attribute

LUT1_L, LUT2_L, LUT3_L, LUT4_L

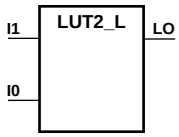
1-, 2-, 3-, 4-Bit Look-Up-Table with Local Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A

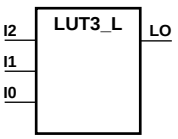




X8378



X8381



X8384

LUT1_L, LUT2_L, LUT3_L, and LUT4_L are, respectively, 1-, 2-, 3-, and 4- bit look-up-tables (LUTs) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

LUT1_L provides a look-up-table version of a buffer or inverter.

See also "LUT1, 2, 3, 4" and "LUT1_D, LUT2_D, LUT3_D, LUT4_D."

Table 7-3 LUT3_L Function Table

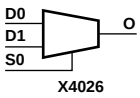
Inputs			Outputs
I2	I1	I0	LO
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]

INIT = binary equivalent of the hexadecimal number assigned to the INIT attribute

M2_1

2-to-1 Multiplexer

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



The M2_1 multiplexer chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects D1.

Inputs			Outputs
S0	D1	D0	O
1	1	X	1
1	0	X	0
0	X	1	1
0	X	0	0

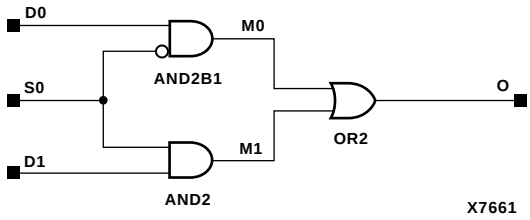
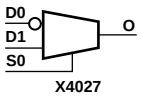


Figure 7-5 M2_1 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

M2_1B1

2-to-1 Multiplexer with D0 Inverted

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



The M2_1B1 multiplexer chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the state of D0. When S0 is High, O reflects the state of D1.

Inputs			Outputs
S0	D1	D0	O
1	1	X	1
1	0	X	0
0	X	1	0
0	X	0	1

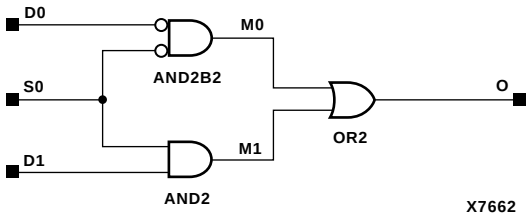
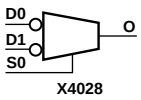


Figure 7-6 M2_1B1 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

M2_1B2

2-to-1 Multiplexer with D0 and D1 Inverted

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



The M2_1B2 multiplexer chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the state of D0. When S0 is High, O reflects the state of D1.

Inputs			Outputs
S0	D1	D0	O
1	1	X	0
1	0	X	1
0	X	1	0
0	X	0	1

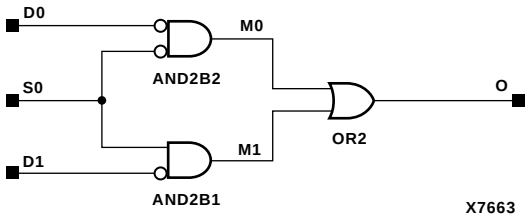
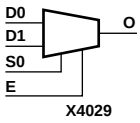


Figure 7-7 M2_1B2 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

M2_1E

2-to-1 Multiplexer with Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



M2_1E is a 2-to-1 multiplexer with enable. When the enable input (E) is High, the M2_1E chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When E is High, the output (O) reflects the state of the selected input. When Low, S0 selects D0 and when High, S0 selects D1. When E is Low, the output is Low.

Inputs				Outputs
E	S0	D1	D0	O
0	X	X	X	0
1	0	X	1	1
1	0	X	0	0
1	1	1	X	1
1	1	0	X	0

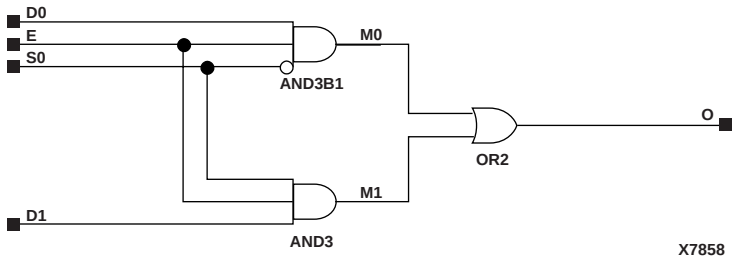
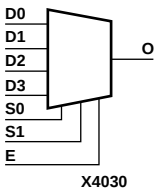


Figure 7-8 M2_1E Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

M4_1E

4-to-1 Multiplexer with Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



M4_1E is an 4-to-1 multiplexer with enable. When the enable input (E) is High, the M4_1E multiplexer chooses one data bit from four sources (D3, D2, D1, or D0) under the control of the select inputs (S1 – S0). The output (O) reflects the state of the selected input as shown in the truth table. When E is Low, the output is Low.

Inputs							Outputs
E	S1	S0	D0	D1	D2	D3	O
0	X	X	X	X	X	X	0
1	0	0	D0	X	X	X	D0
1	0	1	X	D1	X	X	D1
1	1	0	X	X	D2	X	D2
1	1	1	X	X	X	D3	D3

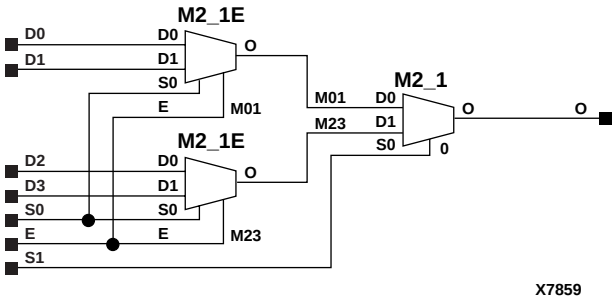


Figure 7-9 M4_1E Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

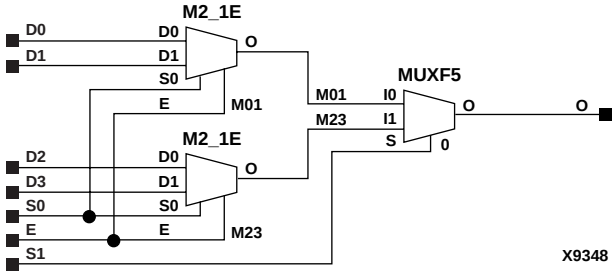
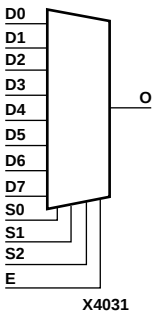


Figure 7-10 M4_1E Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

M8_1E

8-to-1 Multiplexer with Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



M8_1E is an 8-to-1 multiplexer with enable. When the enable input (E) is High, the M8_1E multiplexer chooses one data bit from eight sources (D7 – D0) under the control of the select inputs (S2 – S0). The output (O) reflects the state of the selected input as shown in the truth table. When E is Low, the output is Low.

Inputs					Outputs
E	S2	S1	S0	D7 – D0	O
0	X	X	X	X	0
1	0	0	0	D0	D0
1	0	0	1	D1	D1
1	0	1	0	D2	D2
1	0	1	1	D3	D3
1	1	0	0	D4	D4
1	1	0	1	D5	D5
1	1	1	0	D6	D6
1	1	1	1	D7	D7

Dn represents signal on the Dn input; all other data inputs are don't-cares (X).

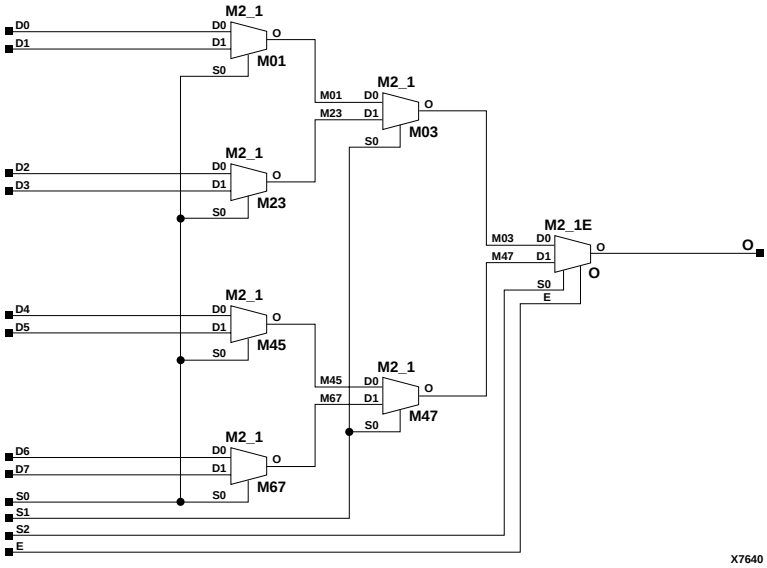


Figure 7-11 M8_1E Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

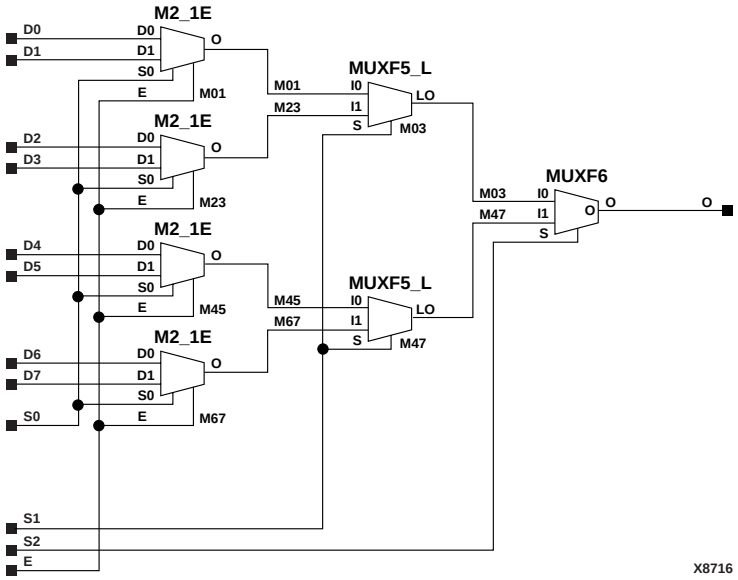
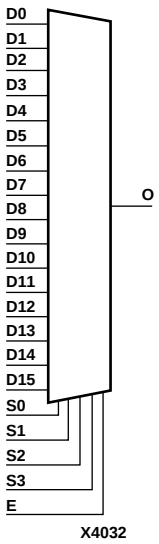


Figure 7-12 M8_1E Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

M16_1E

16-to-1 Multiplexer with Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



M16_1E is a 16-to-1 multiplexer with enable. When the enable input (E) is High, the M16_1E multiplexer chooses one data bit from 16 sources (D15 – D0) under the control of the select inputs (S3 – S0). The output (O) reflects the state of the selected input as shown in the truth table. When E is Low, the output is Low.

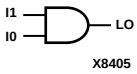
Inputs						Outputs
E	S3	S2	S1	S0	D15 – D0	O
0	X	X	X	X	X	0
1	0	0	0	0	D0	D0
1	0	0	0	1	D1	D1
1	0	0	1	0	D2	D2
1	0	0	1	1	D3	D3
. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	0	0	D12	D12
1	1	1	0	1	D13	D13
1	1	1	1	0	D14	D14
1	1	1	1	1	D15	D15

Dn represents signal on the Dn input; all other data inputs are don't-cares (X).

MULT_AND

Fast Multiplier AND

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MULT_AND is an AND component used exclusively for building fast and smaller multipliers. The I1 and I0 inputs *must* be connected to the I1 and I0 inputs of the associated LUT. The LO output *must* be connected to the DI input of the associated MUXCY, MUXCY_D, or MUXCY_L.

Inputs		Output
I1	I0	LO
0	0	0
0	1	0
1	0	0
1	1	1

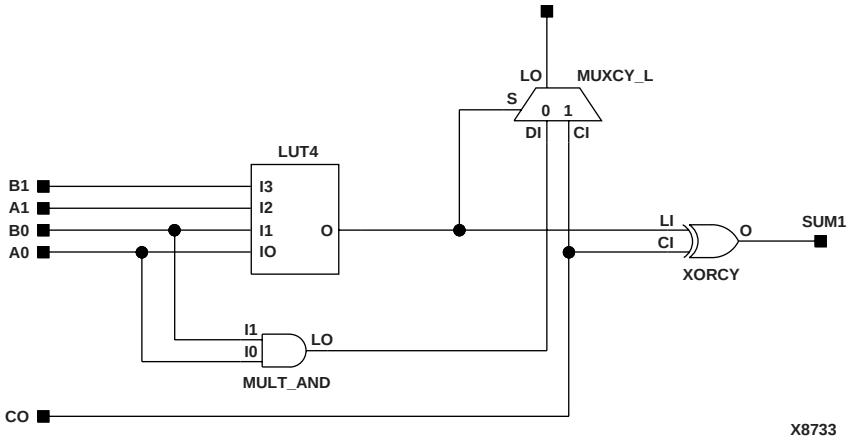
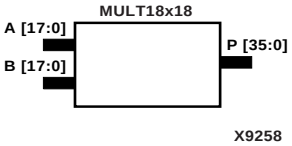


Figure 7-13 Example Multiplier Using MULT_AND

MULT18X18

18 x 18 Signed Multiplier

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



MULT18X18 is a combinational signed 18-bit by 18-bit multiplier. The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B.

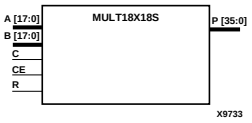
A, B, and P are two's complement.

Inputs		Output
A	B	P
A	B	A * B

MULT18X18S

18 x 18 Signed Multiplier -- Registered Version

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	Primitive	N / A	N / A	N / A



MULT18X18S is the registered version of the 18 x 18 signed multiplier with output P and inputs A, B, C, CE, and R. The registers are initialized to 0 after the GSR pulse.

The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B.

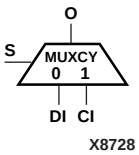
A, B, and P are two's complement.

Inputs					Output
C	CE	Am	Bn	R	P
X	X	X	X	X	--
↑	X	X	X	1	0
↑	1	Am	Bn	0	A * B

MUXCY

2-to-1 Multiplexer for Carry Logic with General Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXCY is used to implement a 1-bit high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of:

- 2-bits per CLB for Virtex, Virtex-E, Spartan-II, and Spartan-IIE
- 4-bits per configurable logic block (CLB) for Virtex-II and Virtex-II PRO

The direct input (DI) of an LC is connected to the DI input of the MUXCY. The carry in (CI) input of an LC is connected to the CI input of the MUXCY. The select input (S) of the MUX is driven by the output of the lookup table (LUT) and configured as a MUX function. The carry out (O) of the MUXCY reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

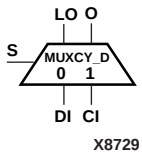
The variants, "MUXCY_D" and "MUXCY_L" provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Inputs			Outputs
S	DI	CI	O
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

MUXCY_D

2-to-1 Multiplexer for Carry Logic with Dual Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXCY_D is used to implement a 1-bit high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_D. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_D. The select input (S) of the MUX is driven by the output of the lookup table (LUT) and configured as an XOR function. The carry out (O and LO) of the MUXCY_D reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output is used to connect to other inputs within the same CLB slice.

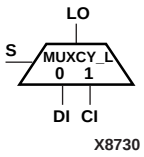
See also "MUXCY" and "MUXCY_L"

Inputs			Outputs	
S	DI	CI	O	LO
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

MUXCY_L

2-to-1 Multiplexer for Carry Logic with Local Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXCY_L is used to implement a 1-bit high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_L. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_L. The select input (S) of the MUX is driven by the output of the lookup table (LUT) and configured as an XOR function. The carry out (LO) of the MUXCY_L reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

The LO output can only connect to other inputs within the same CLB slice.

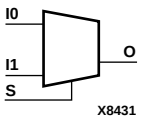
See also "MUXCY" and "MUXCY_D"

Inputs			Outputs
S	DI	CI	LO
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

MUXF5

2-to-1 Lookup Table Multiplexer with General Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXF5 provides a multiplexer function in a CLB slice for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

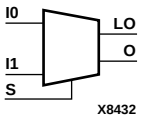
The variants, "MUXF5_D" and "MUXF5_L" provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Inputs			Outputs
S	I0	I1	O
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

MUXF5_D

2-to-1 Lookup Table Multiplexer with Dual Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXF5_D provides a multiplexer function in a CLB slice for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output is used to connect to other inputs within the same CLB slice.

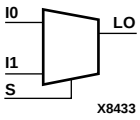
See also "MUXF5" and "MUXF5_L"

Inputs			Outputs	
S	I0	I1	O	LO
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

MUXF5_L

2-to-1 Lookup Table Multiplexer with Local Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXF5_L provides a multiplexer function in a CLB slice for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output is used to connect to other inputs within the same CLB slice.

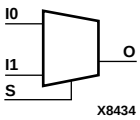
See also "MUXF5" and "MUXCY_L"

Inputs			Output
S	I0	I1	LO
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

MUXF6

2-to-1 Lookup Table Multiplexer with General Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXF6 provides a multiplexer function in a full Virtex, Virtex-E, Virtex-II, Virtex-II PRO, Spartan-II, or Spartan-IIE CLB or one half of a Virtex-II or Virtex-II PRO CLB (two slices) for creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the CLB are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

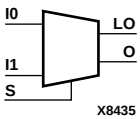
The variants, "MUXF6_D" and "MUXF6_L" provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Inputs			Outputs
S	I0	I1	O
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

MUXF6_D

2-to-1 Lookup Table Multiplexer with Dual Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXF6_D provides a multiplexer function in a full Virtex, Virtex-E, Virtex-II, Virtex-II PRO, Spartan-II, or Spartan-IIE CLB or one half of a Virtex-II or Virtex-II PRO CLB (two slices) for creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the CLB are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output is used to connect to other inputs within the same CLB slice.

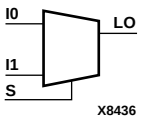
See also "MUXF6" and "MUXF6_L"

Inputs			Outputs	
S	I0	I1	O	LO
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

MUXF6_L

2-to-1 Lookup Table Multiplexer with Local Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



MUXF6_L provides a multiplexer function in a full Virtex, Virtex-E, Virtex-II, Virtex-II PRO, Spartan-II, or Spartan-II E CLB or one half of a Virtex-II or Virtex-II PRO CLB (two slices) for creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the CLB are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output is used to connect to other inputs within the same CLB slice.

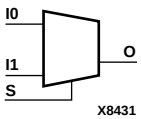
See also "MUXF6" and "MUXF6_D"

Inputs			Output
S	I0	I1	LO
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

MUXF7

2-to-1 Lookup Table Multiplexer with General Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



MUXF7 provides a multiplexer function in a full Virtex-II and Virtex-II PRO CLB for creating a function-of-7 lookup table or a 16-to-1 multiplexer in combination with the associated lookup tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

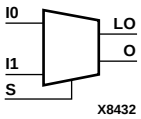
The variants, "MUXF7_D" and "MUXF7_L" provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Inputs			Outputs
S	I0	I1	O
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

MUXF7_D

2-to-1 Lookup Table Multiplexer with Dual Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



MUXF7_D provides a multiplexer function in one full Virtex-II and Virtex-II PRO CLB for creating a function-of-7 lookup table or a 16-to-1 multiplexer in combination with the associated lookup tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output is used to connect to other inputs within the same CLB slice.

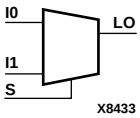
See also "MUXF7" and "MUXF7_L".

Inputs			Outputs	
S	I0	I1	O	LO
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

MUXF7_L

2-to-1 Lookup Table Multiplexer with Local Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



MUXF7_L provides a multiplexer function in a full Virtex-II and Virtex-II PRO CLB for creating a function-of-7 lookup table or a 16-to-1 multiplexer in combination with the associated lookup tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output is used to connect to other inputs within the same CLB slice.

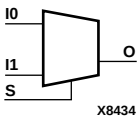
See also "MUXF7" and "MUXF7_D".

Inputs			Output
S	**I0**	**I1**	**LO**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

MUXF8

2-to-1 Lookup Table Multiplexer with General Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



MUXF8 provides a multiplexer function in two full Virtex-II and Virtex-II PRO CLBs for creating a function-of-7 lookup table or a 32-to-1 multiplexer in combination with the associated lookup tables and two MUXF8s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

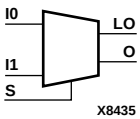
The variants, "MUXF8_D" and "MUXF8_L" provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Inputs			Outputs
S	I0	I1	O
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

MUXF8_D

2-to-1 Lookup Table Multiplexer with Dual Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



MUXF8_D provides a multiplexer function in two full Virtex-II and Virtex-II PRO CLBs for creating a function-of-8 lookup table or a 32-to-1 multiplexer in combination with the associated four lookup tables and two MUXF8s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output is used to connect to other inputs within the same CLB slice.

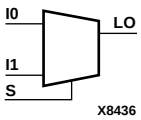
See also "MUXF8" and "MUXF8_L"

Inputs			Outputs	
S	I0	I1	O	LO
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

MUXF8_L

2-to-1 Lookup Table Multiplexer with Local Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



MUXF8_L provides a multiplexer function in two full Virtex-II and Virtex-II PRO CLBs for creating a function-of-8 lookup table or a 32-to-1 multiplexer in combination with the associated four lookup tables and two MUXF8s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output is used to connect to other inputs within the same CLB slice.

See also "MUXF8" and "MUXF8_D".

Inputs			Output
S	I0	I1	LO
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

NAND2-9

2- to 9-Input NAND Gates with Inverted and Non-Inverted Inputs

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner
NAND2, NAND2B1, NAND2B2, NAND3, NAND3B1, NAND3B2, NAND3B3, NAND4, NAND4B1, NAND4B2, NAND4B3, NAND4B4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND5, NAND5B1, NAND5B2, NAND5B3, NAND5B4, NAND5B5	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND6, NAND7, NAND8, NAND9	Macro	Macro	Macro	Primitive	Primitive	Primitive

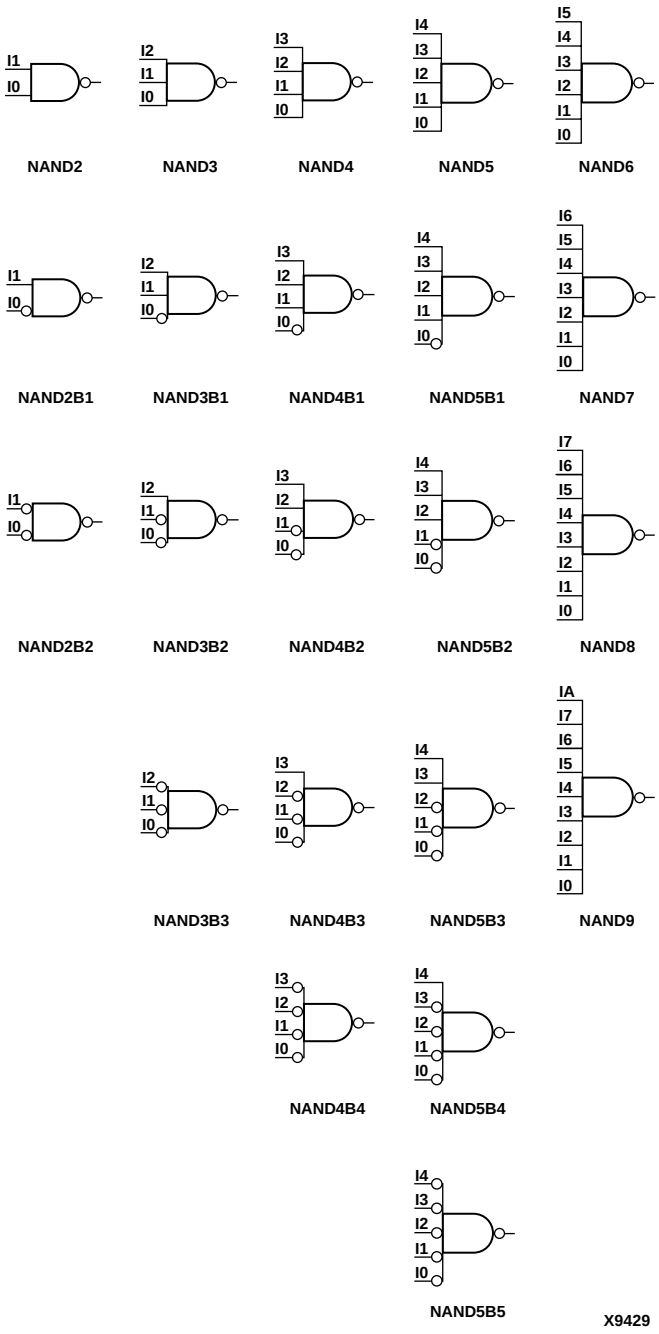


Figure 7-14 NAND Gate Representations

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Since each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

See the "NAND12, 16" section for information on additional NAND functions.

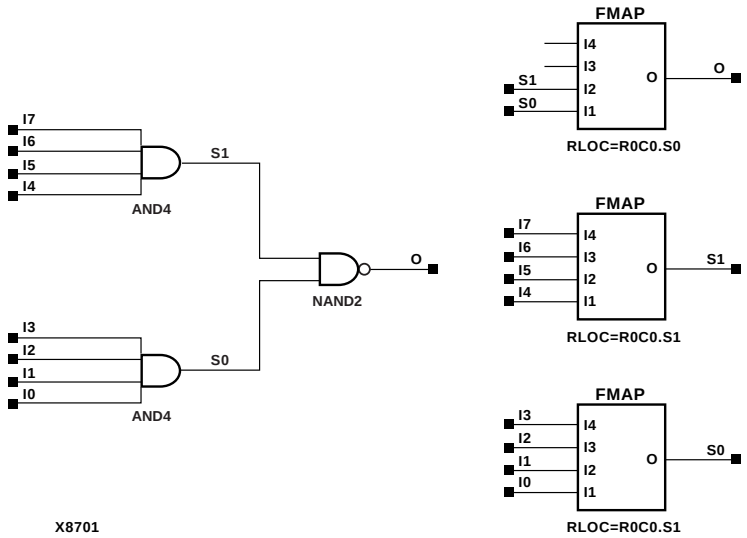


Figure 7-15 NAND8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

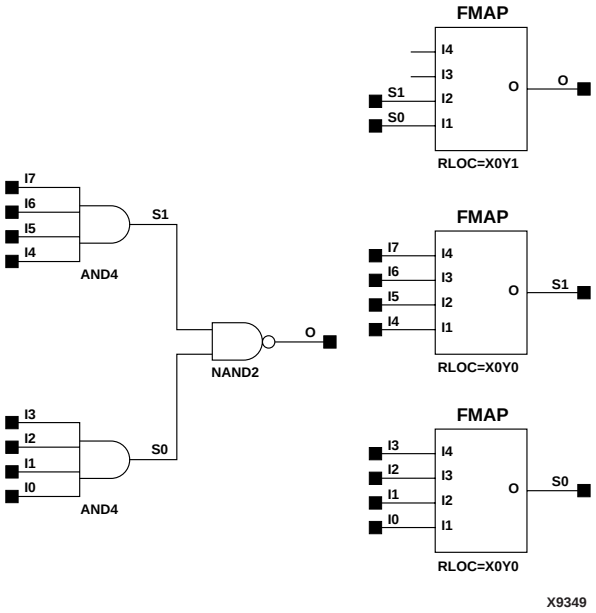
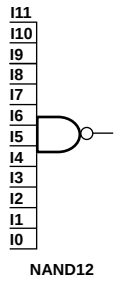


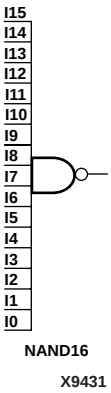
Figure 7-16 NAND8 Implementation Virtex-II, Virtex-II PRO

NAND12, 16

12- and 16-Input NAND Gates with Non-Inverted Inputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A





The NAND function is performed in the Configurable Logic Block (CLB) function generators for Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO. The 12- and 16-input NAND functions are available only with non-inverting inputs. To invert some or all inputs, use external inverters.

See the "NAND2-9" section for more information on NAND functions.

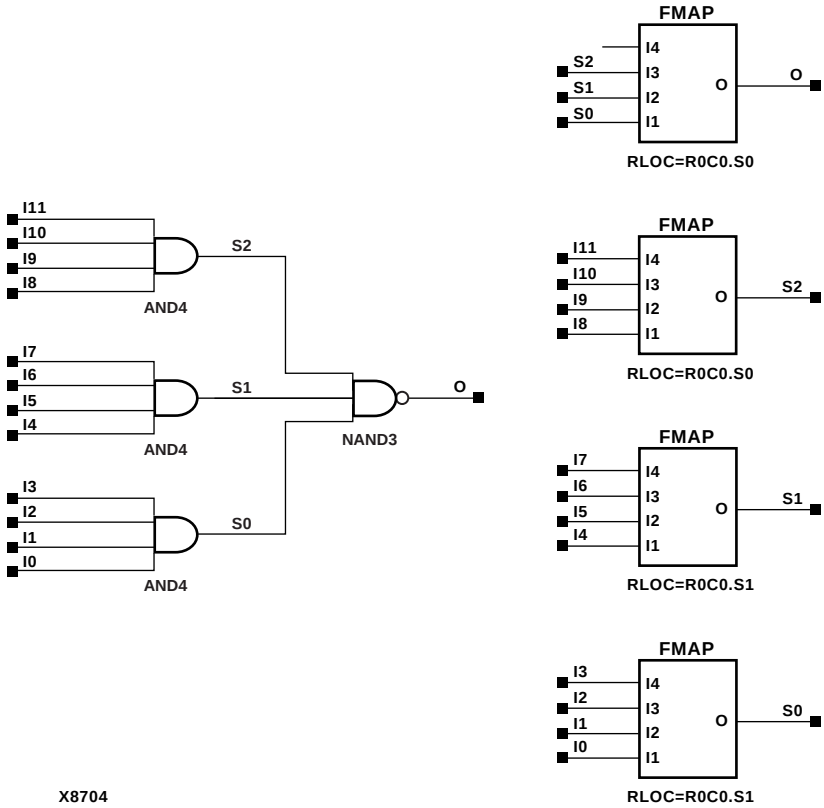


Figure 7-17 NAND12 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

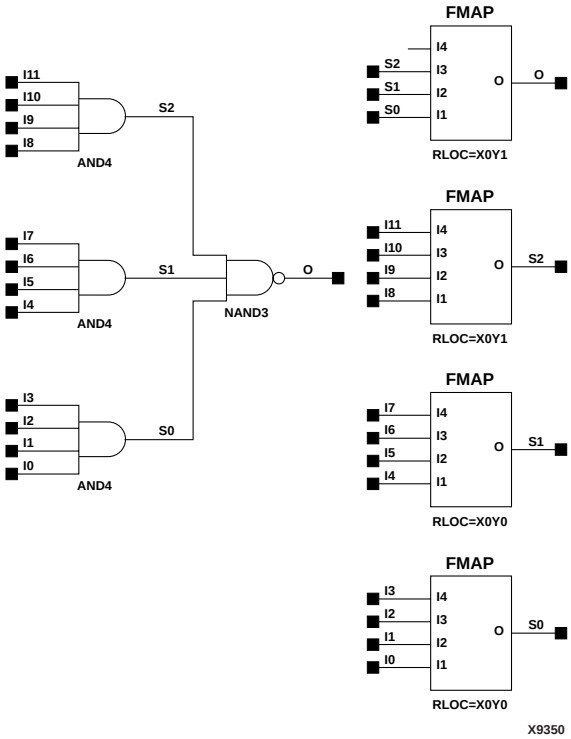


Figure 7-18 NAND12 Implementation Virtex-II, Virtex-II PRO

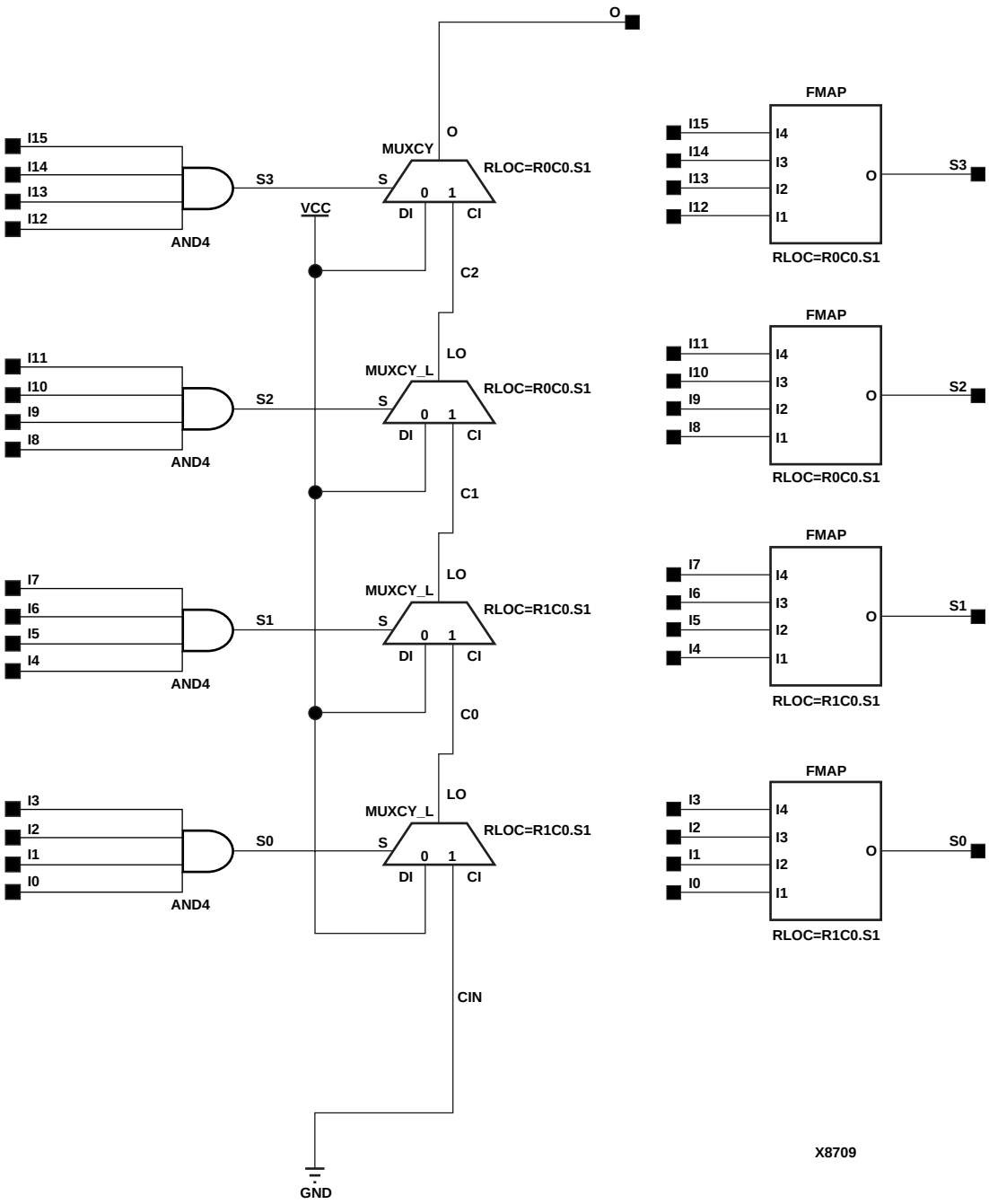


Figure 7-19 NAND16 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

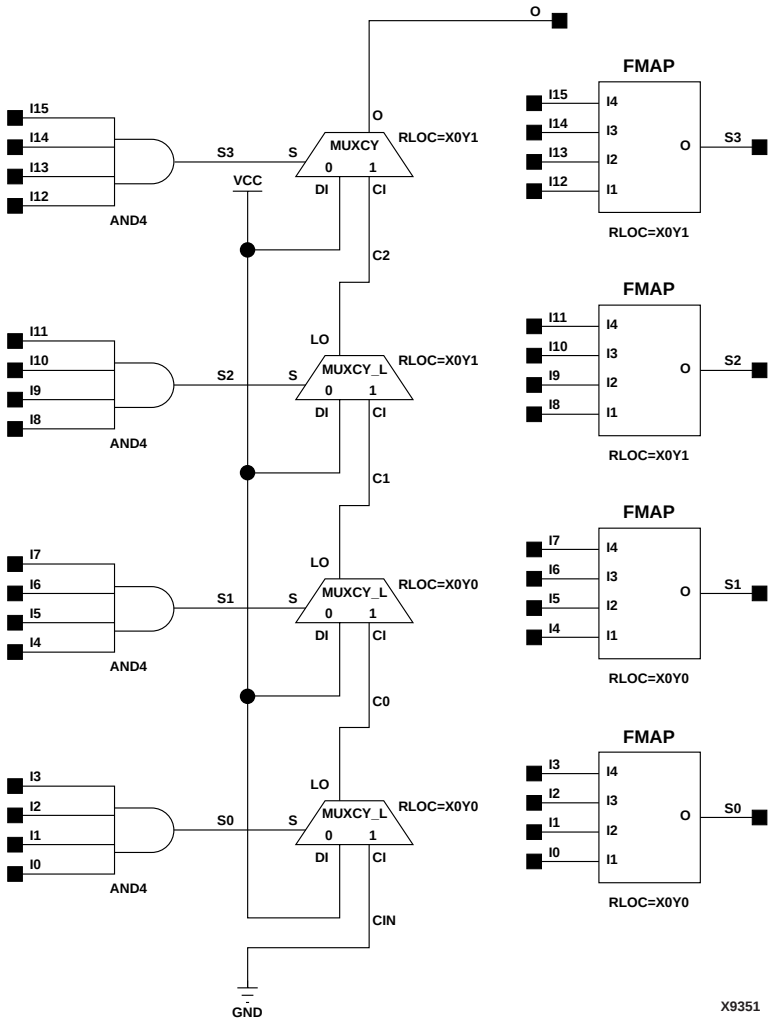


Figure 7-20 NAND16 Implementation Virtex-II, Virtex-II PRO

NOR2-9

2- to 9-Input NOR Gates with Inverted and Non-Inverted Inputs

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
NOR2, NOR2B1, NOR2B2, NOR3, NOR3B1, NOR3B2, NOR3B3, NOR4, NOR4B1, NOR4B2, NOR4B3, NOR4B4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR5, NOR5B1, NOR5B2, NOR5B3, NOR5B4, NOR5B5	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR6, NOR7, NOR8, NOR9	Macro	Macro	Macro	Primitive	Primitive	Primitive

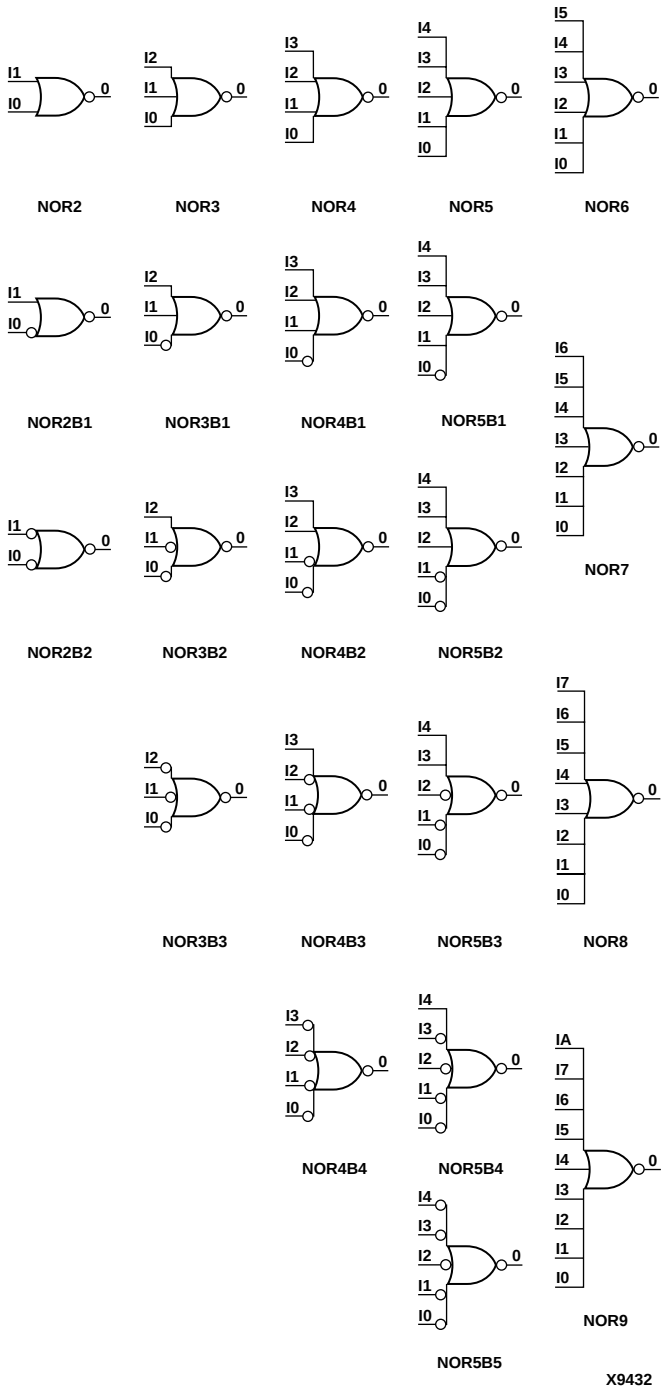


Figure 7-21 NOR Gate Representations

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Since each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

See the "NOR12, 16" section for information on additional NOR functions.

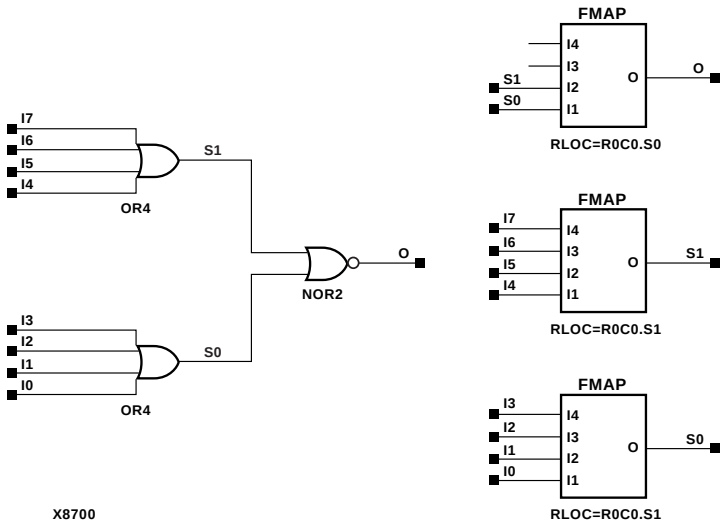


Figure 7-22 NOR8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

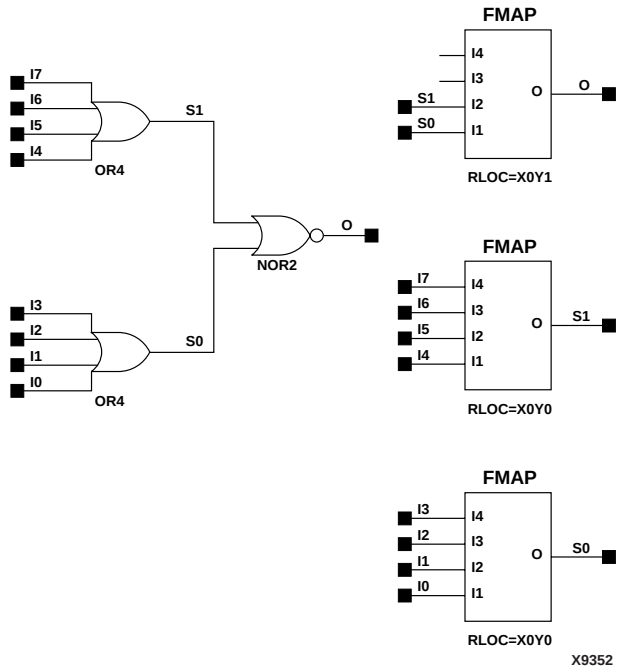
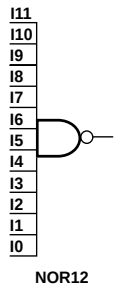


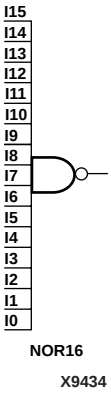
Figure 7-23 NOR8 Implementation Virtex-II, Virtex-II PRO

NOR12, 16

12- and 16-Input NOR Gates with Non-Inverted Inputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A





The 12- and 16-input NOR functions are available only with non-inverting inputs. To invert some or all inputs, use external inverters.

See the "NOR2-9" section for more information on NOR functions.

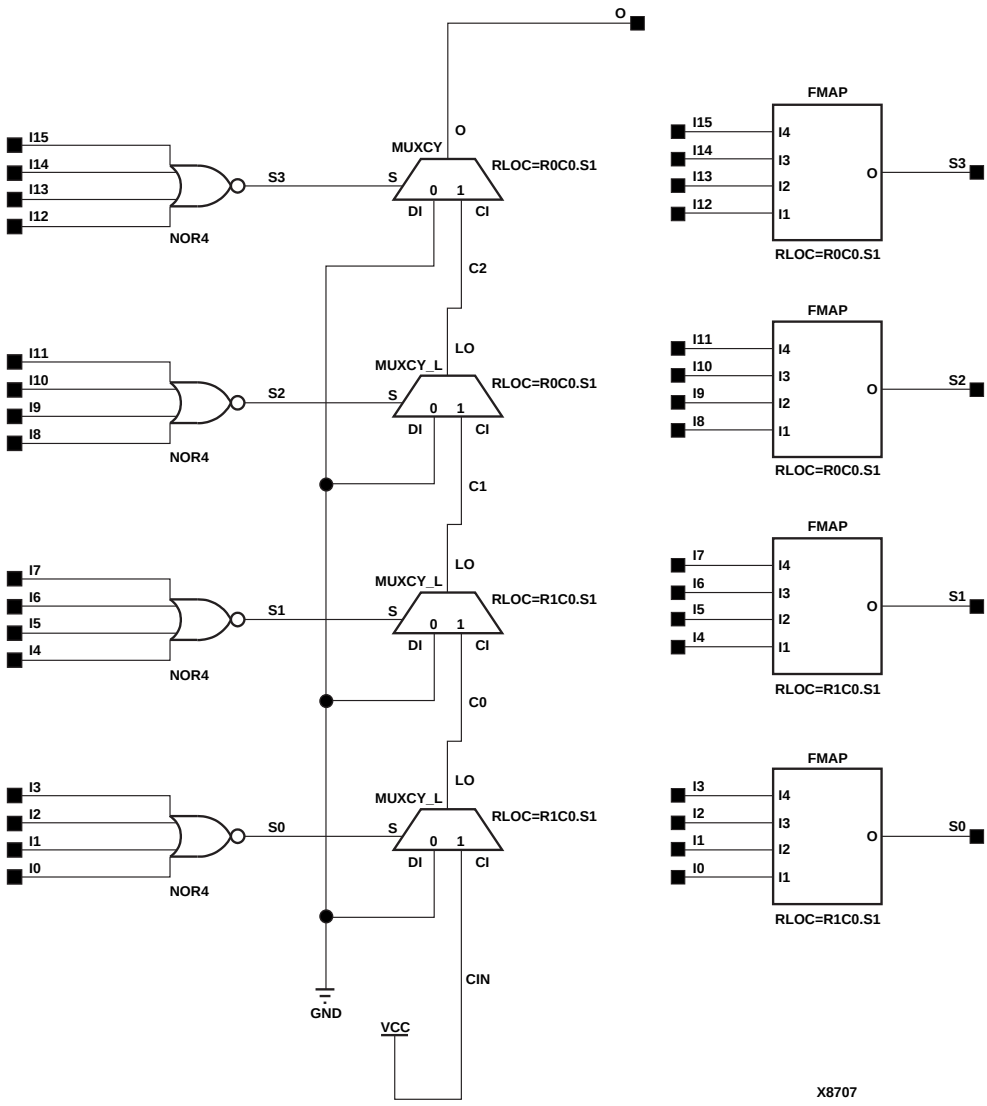


Figure 7-24 NOR16 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

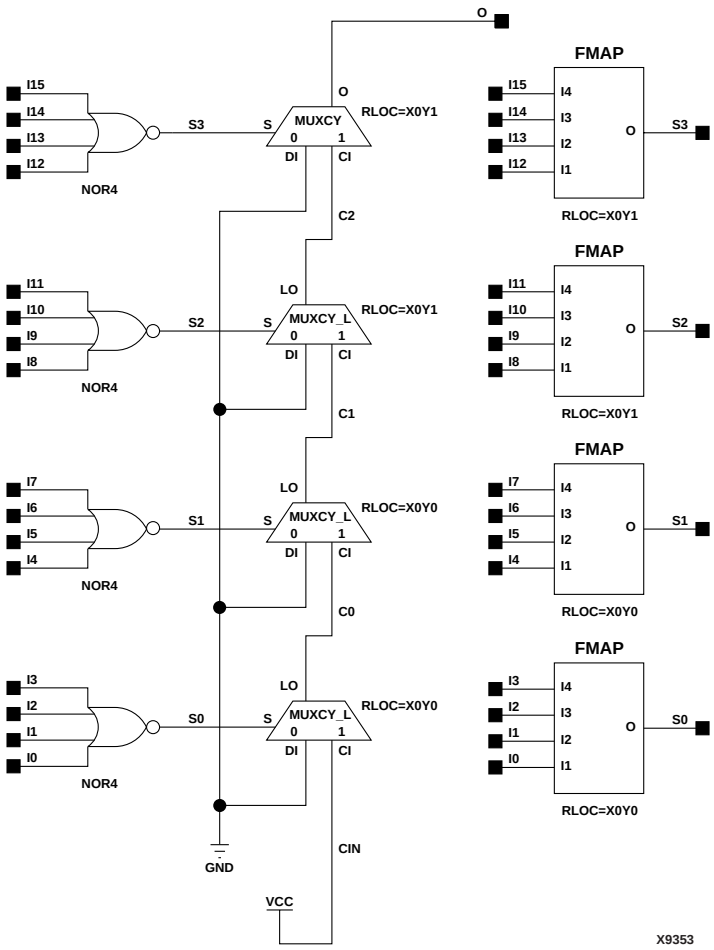


Figure 7-25 NOR16 Implementation Virtex-II, Virtex-II PRO

Chapter 8

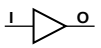
OBUF, 4, 8, 16 to ORCY

OBUF, 4, 8, 16

Single- and Multiple-Output Buffers

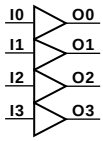
Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OBUF	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OBUF4, OBUF8, OBUF16	Macro	Macro	Macro	Macro	Macro	Macro

OBUF



X9445

OBUF4



X9446

OBUF8

X3804

OBUF16

X3816

OBUF, OBUF4, OBUF8, and OBUF16 are single and multiple output buffers. An OBUF isolates the internal circuit and provides drive current for signals leaving a chip. OBUFs exist in input/output blocks (IOB). The output (O) of an OBUF is connected to an OPAD or an IOPAD.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, if a high impedance (Z) signal from an on-chip 3-state buffer (like BUFE) is applied to the input of an OBUF, it is propagated to the CPLD device output pin.

For Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, see the "OBUF_selectIO" section for information on OBUF variants with selectable I/O interfaces. The I/O interface standard used by OBUF, 4, 8, and 16 is LVTTL. Also, Virtex, Virtex-E, Spartan-II, and Spartan-IIE OBUF, 4, 8, and 16 have selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

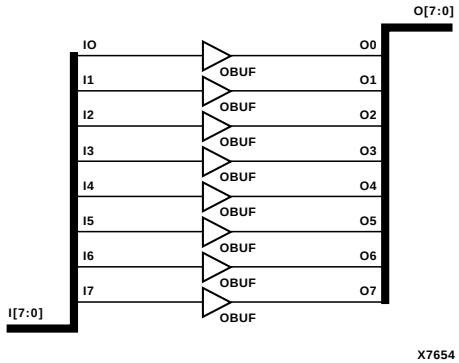


Figure 8-1 OBUF8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E

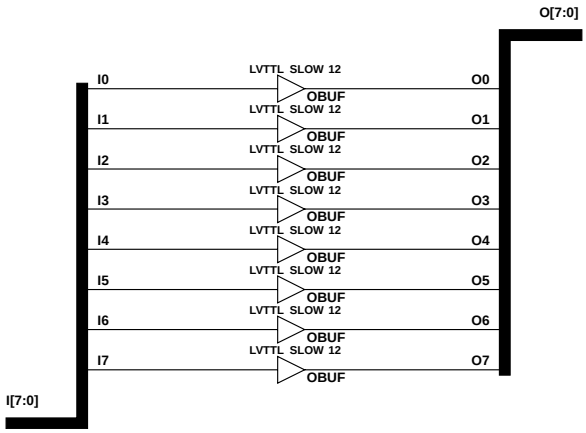
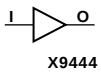


Figure 8-2 OBUF8 Implementation Virtex-II, Virtex-II PRO

OBUF_*selectIO*

Single Output Buffer with Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



For Virtex, Virtex-E, Virtex-II, and Virtex-II PRO, Spartan-II, and Spartan-IIE, OBUF and its selectIO variants (listed in the "Components" column in the table below) are single output buffers whose I/O interface corresponds to a specific I/O standard. The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. The S, F, and 2, 4, 6, 8, 12, 16, 24 extensions specify the slew rate (SLOW or FAST) and the drive power (2, 4, 6, 8, 12, 16, 24 mA) for the LVTTL standard variants. For example, OBUF_F_12 is a single output buffer that uses the LVTTL I/O-signaling standard with a FAST slew and 12mA of drive power. You can attach an IOSTANDARD attribute to an IOBUF instance instead of using an IOBUF_*selectIO* component. Check marks (√) in the "Spartan-II, Spartan-IIE, Virtex" and "Virtex-E" columns indicate the components and IOSTANDARD attribute values available for those architectures.

An OBUF that uses the LVTTL, LVCMOS15, LVCMOS18, LVCMOS25, or LVCMOS33 signaling standards has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

An OBUF isolates the internal circuit and provides drive current for signals leaving a chip. OBUFs exist in input/output blocks (IOB). The output (O) of an OBUF is connected to an OPAD or an IOPAD.

The hardware implementation of the I/O standard requires that you follow a set of usage rules for the SelectI/O buffer components. See the "SelectI/O Usage Rules" under the IBUF_*selectIO* section for information on using these components.

Table 8-1 Spartan-II, Spartan-IIE, Virtex, and Virtex-E OBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II, Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Output VCCO
OBUF	√	√	(default is LVTTL) [b]	3.3
OBUF_S_2	√	√	LVTTL [b]	3.3
OBUF_S_4	√	√	LVTTL [b]	3.3
OBUF_S_6	√	√	LVTTL [b]	3.3
OBUF_S_8	√	√	LVTTL [b]	3.3
OBUF_S_12	√	√	LVTTL [b]	3.3
OBUF_S_16	√	√	LVTTL [b]	3.3
OBUF_S_24	√	√	LVTTL [b]	3.3
OBUF_F_2	√	√	LVTTL [b]	3.3
OBUF_F_4	√	√	LVTTL [b]	3.3
OBUF_F_6	√	√	LVTTL [b]	3.3

Table 8-1 Spartan-II, Spartan-IIE, Virtex, and Virtex-E OBUF_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II, Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Output VCCO
OBUF_F_8	√	√	LVTTL [b]	3.3
OBUF_F_12	√	√	LVTTL [b]	3.3
OBUF_F_16	√	√	LVTTL [b]	3.3
OBUF_F_24	√	√	LVTTL [b]	3.3
OBUF_AGP	√	√	AGP	3.3
OBUF_CTT	√	√	CTT	3.3
OBUF_GTL	√	√	GTL	N / A
OBUF_GTLP	√	√	GTLP	N / A
OBUF_HSTL_I	√	√	HSTL_I	1.5
OBUF_HSTL_III	√	√	HSTL_III	1.5
OBUF_HSTL_IV	√	√	HSTL_IV	1.5
OBUF_LVCMOS2	√		LVCMOS2	2.5
OBUF_LVCMOS18		√	LVCMOS18 [b]	1.8
OBUF_LVCMOS18_F_2			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_F_4			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_F_6			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_F_8			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_F_12			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_S_2			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_S_4			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_S_6			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_S_8			LVCMOS18 [b]	1.8
OBUF_LVCMOS18_S_12			LVCMOS18 [b]	1.8
OBUF_LVDS		√	LVDS	2.5
OBUF_LVPECL		√	LVPECL	3.3
OBUF_PCI33_3	√	√	PCI33_3	3.3
OBUF_PCI33_5	√	√	PCI33_5	3.3
OBUF_PCI66_3, PCIx66_3	√	√	PCI66_3, PCIx66_3	3.3
OBUF_SSTL2_I	√	√	SSTL2_I	2.5
OBUF_SSTL2_II	√	√	SSTL2_II	2.5
OBUF_SSTL3_I	√	√	SSTL3_I	3.3
OBUF_SSTL3_II	√	√	SSTL3_II	3.3

[b] The LVTTL, LVCMOS15, LVCMOS18 attributes also require a slew value (FAST or SLOW) and DRIVE value. See the FAST, SLOW, and DRIVE attribute descriptions in the *Xilinx Constraints Guide* for valid values for each architecture.

The Virtex-II and Virtex-II PRO library includes some OBUF_*selectIO* components for compatibility with older, existing designs and other architectures. For new Virtex-II and Virtex-II PRO designs, however, the recommended method for using OBUF selectI/O buffers is to attach an IOSTANDARD attribute to an OBUF component. For example, attach IOSTANDARD=GTLP to an OBUF instead of using the OBUF_GTLP component for new Virtex-II and Virtex-II PRO designs. The IOSTANDARD attributes that can be attached to an OBUF component are listed in the "IOSTANDARD (Attribute Value)" column in Table 8-2. See the "SelectI/O Usage Rules" section for information on using these IOSTANDARD attributes.

Table 8-2 Virtex-II, Virtex-II PRO OBUF_*selectIO* IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Terminate Type
OBUF[a]	√	AGP*	3.3	None
		*does not apply to Virtex-II PRO		
OBUF[a]	√	F_12	3.3	None
OBUF[a]	√	F_16	3.3	None
OBUF[a]	√	F_2	3.3	None
OBUF[a]	√	F_24	3.3	None
OBUF[a]	√	F_4	3.3	None
OBUF[a]	√	F_6	3.3	None
OBUF[a]	√	F_8	3.3	None
OBUF[a]	√	GTL	N/A	None
OBUF[a]	√	GTL_DCI	1.2	Single
OBUF[a]	√	GTLP	N/A	None
OBUF[a]	√	GTLP_DCI	1.5	Single
OBUF[a]	√	HSTL_I	1.5	None
OBUF[a]	√	HSTL_I_18	1.8	None
OBUF[a]	√	HSTL_I_DCI	1.5	Split
OBUF[a]	√	HSTL_I_DCI_18	1.5	Split
OBUF[a]	√	HSTL_II	1.5	None
OBUF[a]	√	HSTL_II_18	1.5	None
OBUF[a]	√	HSTL_II_DCI	1.5	Split
OBUF[a]	√	HSTL_II_DCI_18	1.8	Split
OBUF[a]	√	HSTL_III	1.5	None
OBUF[a]	√	HSTL_III_18	1.8	None
OBUF[a]	√	HSTL_III_DCI	1.5	Split
OBUF[a]	√	HSTL_III_DCI_18	1.8	Split
OBUF[a]	√	HSTL_IV	1.5	None
OBUF[a]	√	HSTL_IV_18	1.8	None
OBUF[a]	√	HSTL_IV_DCI	1.5	Split
OBUF[a]	√	HSTL_IV_DCI_18	1.8	Split
OBUF[a]	√	LVCMOS15[b]	1.5	None
OBUF[a]	√	LVCMOS15_F_12[b]	1.5	None

Table 8-2 Virtex-II, Virtex-II PRO OBUF_*selectIO* IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Terminate Type
OBUF[a]	√	LVCMOS15_F_16[b]	1.5	None
OBUF[a]	√	LVCMOS15_F_2 [b]	1.5	None
OBUF[a]	√	LVCMOS15_F_4 [b]	1.5	None
OBUF[a]	√	LVCMOS15_F_6[b]	1.5	None
OBUF[a]	√	LVCMOS15_F_8 [b]	1.5	None
OBUF[a]	√	LVCMOS15_S_12 [b]	1.5	None
OBUF[a]	√	LVCMOS15_S_16 [b]	1.5	None
OBUF[a]	√	LVCMOS15_S_2 [b]	1.5	None
OBUF[a]	√	LVCMOS15_S_4[b]	1.5	None
OBUF[a]	√	LVCMOS15_S_6[b]	1.5	None
OBUF[a]	√	LVCMOS15_S_8[b]	1.5	None
OBUF[a]	√	LVCMOS18 [b]	1.8	None
OBUF[a]	√	LVCMOS18 _F_12[b]	1.8	None
OBUF[a]	√	LVCMOS18 _F_16[b]	1.8	None
OBUF[a]	√	LVCMOS18 _F_2[b]	1.8	None
OBUF[a]	√	LVCMOS18 _F_4[b]	1.8	None
OBUF[a]	√	LVCMOS18 _F_6[b]	1.8	None
OBUF[a]	√	LVCMOS18 _F_8[b]	1.8	None
OBUF[a]	√	LVCMOS18 _S_12[b]	1.8	None
OBUF[a]	√	LVCMOS18 _S_16[b]	1.8	None
OBUF[a]	√	LVCMOS18 _S_2[b]	1.8	None
OBUF[a]	√	LVCMOS18 _S_4[b]	1.8	None
OBUF[a]	√	LVCMOS18 _S_6[b]	1.8	None
OBUF[a]	√	LVCMOS18 _S_8[b]	1.8	None
OBUF[a]	√	LVCMOS2 [b]	1.8	None
OBUF[a]	√	LVCMOS25 [b]	2.5	None
OBUF[a]	√	LVCMOS25 _F_12[b]	2.5	None
OBUF[a]	√	LVCMOS25 _F_16[b]	2.5	None
OBUF[a]	√	LVCMOS25 _F_2[b]	2.5	None
OBUF[a]	√	LVCMOS25 _F_24[b]	2.5	None
OBUF[a]	√	LVCMOS25 _F_4[b]	2.5	None
OBUF[a]	√	LVCMOS25 _F_6[b]	2.5	None
OBUF[a]	√	LVCMOS25 _F_8[b]	2.5	None
OBUF[a]	√	LVCMOS25 _S_12[b]	2.5	None
OBUF[a]	√	LVCMOS25 _S_16[b]	2.5	None
OBUF[a]	√	LVCMOS25 _S_2[b]	2.5	None
OBUF[a]	√	LVCMOS25 _S_24[b]	2.5	None
OBUF[a]	√	LVCMOS25 _S_4[b]	2.5	None
OBUF[a]	√	LVCMOS25 _S_6[b]	2.5	None
OBUF[a]	√	LVCMOS25 _S_8[b]	2.5	None

Table 8-2 Virtex-II, Virtex-II PRO OBUF_*selectIO* IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Terminate Type
OBUF[a]	√	LVCMOS33 [b]	3.3	None
OBUF[a]	√	LVCMOS33 _F_12[b]	3.3	None
OBUF[a]	√	LVCMOS33 _F_16[b]	3.3	None
OBUF[a]	√	LVCMOS33 _F_2[b]	3.3	None
OBUF[a]	√	LVCMOS33 _F_24[b]	3.3	None
OBUF[a]	√	LVCMOS33 _F_4[b]	3.3	None
OBUF[a]	√	LVCMOS33 _F_6[b]	3.3	None
OBUF[a]	√	LVCMOS33 _F_8[b]	3.3	None
OBUF[a]	√	LVCMOS33 _S_12[b]	3.3	None
OBUF[a]	√	LVCMOS33 _S_16[b]	3.3	None
OBUF[a]	√	LVCMOS33 _S_2[b]	3.3	None
OBUF[a]	√	LVCMOS33 _S_24[b]	3.3	None
OBUF[a]	√	LVCMOS33 _S_4[b]	3.3	None
OBUF[a]	√	LVCMOS33 _S_6[b]	3.3	None
OBUF[a]	√	LVCMOS33 _S_8[b]	3.3	None
OBUF[a]	√	LVDCI_15	1.5	Driver
OBUF[a]	√	LVDCI_18	1.8	Driver
OBUF[a]	√	LVDCI_25	2.5	Driver
OBUF[a]	√	LVDCI_33	3.3	Driver
OBUF[a]	√	LVDCI_DV2_15	1.5	Driver
OBUF[a]	√	LVDCI_DV2_18	1.8	Driver
OBUF[a]	√	LVDCI_DV2_25	2.5	Driver
OBUF[a]	√	LVDCI_DV2_33	3.3	Driver
OBUF[a]	√	LVTTL [b]	3.3	None
OBUF[a]	√	LVTTL _F_12[b]	3.3	None
OBUF[a]	√	LVTTL _F_16[b]	3.3	None
OBUF[a]	√	LVTTL _F_2[b]	3.3	None
OBUF[a]	√	LVTTL _F_24[b]	3.3	None
OBUF[a]	√	LVTTL _F_4[b]	3.3	None
OBUF[a]	√	LVTTL _F_6[b]	3.3	None
OBUF[a]	√	LVTTL _F_8[b]	3.3	None
OBUF[a]	√	LVTTL _S_12[b]	3.3	None
OBUF[a]	√	LVTTL _S_16[b]	3.3	None
OBUF[a]	√	LVTTL _S_2[b]	3.3	None
OBUF[a]	√	LVTTL _S_24[b]	3.3	None
OBUF[a]	√	LVTTL _S_4[b]	3.3	None
OBUF[a]	√	LVTTL _S_6[b]	3.3	None
OBUF[a]	√	LVTTL _S_8[b]	3.3	None
OBUF[a]	√	PCI33_3	3.3	None
OBUF[a]	√	PCI66_3	3.3	None

Table 8-2 Virtex-II, Virtex-II PRO OBUF_*selectIO* IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Terminate Type
OBUF[a]	√	PCIX	3.3	None
OBUF[a]	√	SSTL2_I	2.5	None
OBUF[a]	√	SSTL2_I_DCI	2.5	Split
OBUF[a]	√	SSTL2_II	2.5	None
OBUF[a]	√	SSTL2_II_DCI	2.5	Split
OBUF[a]	√	SSTL3_I	3.3	None
OBUF[a]	√	SSTL3_I_DCI	3.3	Split
OBUF[a]	√	SSTL3_II	3.3	None
OBUF[a]	√	SSTL3_II_DCI	3.3	Split
OBUF[a]	√		3.3	None
OBUF[a]	√	S_12	3.3	None
OBUF[a]	√	S_16	3.3	None
OBUF[a]	√	S_2	3.3	None
OBUF[a]	√	S_24	3.3	None
OBUF[a]	√	S_4	3.3	None
OBUF[a]	√	S_6	3.3	None
OBUF[a]	√	S_8	3.3	None

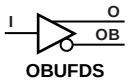
[a]Attach an IOSTANDARD attribute to an OBUF and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the output for the I/O standard associated with that value.

[b] The LVTTL, LVCMOS15, LVCMOS18, LVCMOS25, LVCMOS33 attributes also require a slew value (FAST or SLOW) and DRIVE value. See the FAST, SLOW, and DRIVE attribute descriptions in the *Xilinx Constraints Guide* for valid values for each architecture.

OBUFDS

Differential Signaling Output Buffer with Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



OBUFDS is a single output buffer that supports low-voltage, differential signaling (1.8v CMOS). OBUFDS isolates the internal circuit and provides drive current for signals leaving the chip. Its output is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET and MYNETB).

Inputs	Outputs	
I	O	OB
0	0	1
1	1	0

The IOSTANDARD attribute values listed in the following table can be applied to an OBUFGDS component to provide selectI/O interface capability. See the *Xilinx Constraints Guide* for information using these attributes.

Component	IOSTANDARD (Attribute Value)	Output VCCO	VREF	Terminate Type
OBUFDS[a]	BLVDS_25	2.5	N/A	TBD
OBUFDS[a]	LDT_25	2.5	N/A	TBD
OBUFDS[a]	LVDS_25 (default)	2.5	N/A	None
OBUFDS[a]	LVDS_33*	3.3	N/A	None
	*does not apply to Virtex-II PRO			
OBUFDS[a]	LVPECL-33*	3.3	N/A	None
	*does not apply to Virtex-II PRO			
OBUFDS[a]	LVDSEXT_25	2.5	N/A	None
OBUFDS[a]	LVDSEXT_33*	3.3	N/A	None
	*does not apply to Virtex-II PRO			
OBUFDS[a]	ULVDS_25	TBD	TBD	TBD

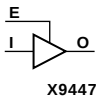
[a]Attach an IOSTANDARD attribute to an OBUFDS and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the output for the I/O standard associated with that value.

OBUFE, 4, 8, 16

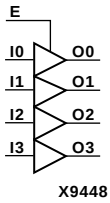
3-State Output Buffers with Active-High Output Enable

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OBUFE	Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUFE4, OBUFE8, OBUFE16	Macro	Macro	Macro	Macro	Macro	Macro

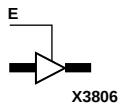
OBUFE



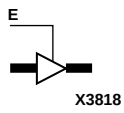
OBUFE4



OBUFE8



OBUFE16



OBUFE, OBUFE4, OBUFE8, and OBUFE16 are 3-state buffers with inputs I, I3 – I0, I7 – I0, and I15-I0, respectively; outputs O, O3 – O0, O7 – O0, and O15-O0, respectively; and active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). An OBUFE isolates the internal circuit and provides drive current for signals leaving a chip. An OBUFE output is connected to an OPAD or an IOPAD. An OBUFE input is connected to the internal circuit.

Inputs		Outputs
E	I	O
0	X	Z
1	1	1
1	0	0

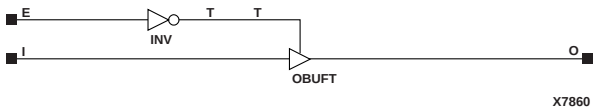


Figure 8-3 OBUFE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

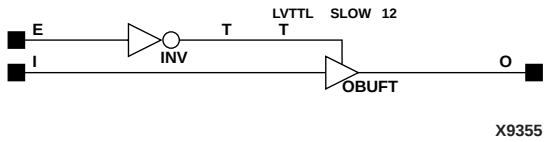


Figure 8-4 OBUFE Implementation Virtex-II, Virtex-II PRO

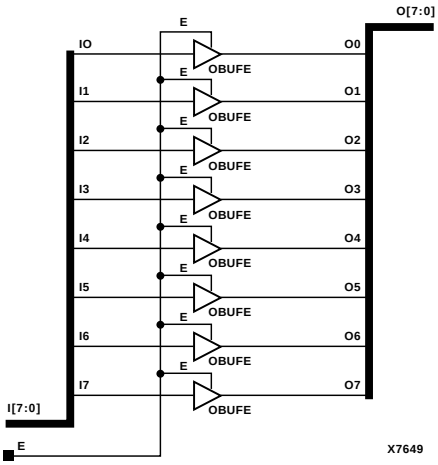


Figure 8-5 OBUFE8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

OBUFT, 4, 8, 16

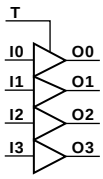
Single and Multiple 3-State Output Buffers with Active-Low Output Enable

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OBUFT	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OBUFT4, OBUFT8, OBUFT16	Macro	Macro	Macro	Macro	Macro	Macro

OBUFT

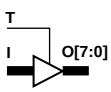
X9449

OBUFT4



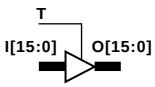
X9450

OBUFT8



X3805

OBUFT16



X3817

OBUFT, OBUFT4, OBUFT8, and OBUFT16 are single and multiple 3-state output buffers with inputs I, I3 – I0, I7 – I0, I15 – I0, outputs O, O3 – O0, O7 – O0, O15 – O0, and active-Low output enables (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs isolate the internal circuit and provide extra drive current for signals leaving a chip. An OBUFT output is connected to an OPAD or an IOPAD.

For Virtex, Virtex-E, Virtex-II, Virtex-II PRO, Spartan-II, and Spartan-IIE, see the "OBUFT_selectIO" section for information on OBUFT variants with selectable I/O interfaces. OBUFT, 4, 8, and 16 use the LVTTL standard. Also, Virtex, Virtex-E, Virtex-II, Virtex-II PRO, Spartan-II, and Spartan-IIE OBUFT, 4, 8, and 16 have selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Inputs		Outputs
T	I	O
1	X	Z
0	1	1
0	0	0

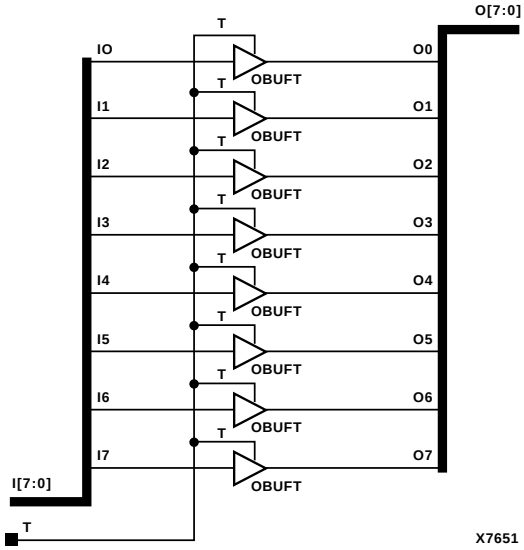


Figure 8-6 OBUFT8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E

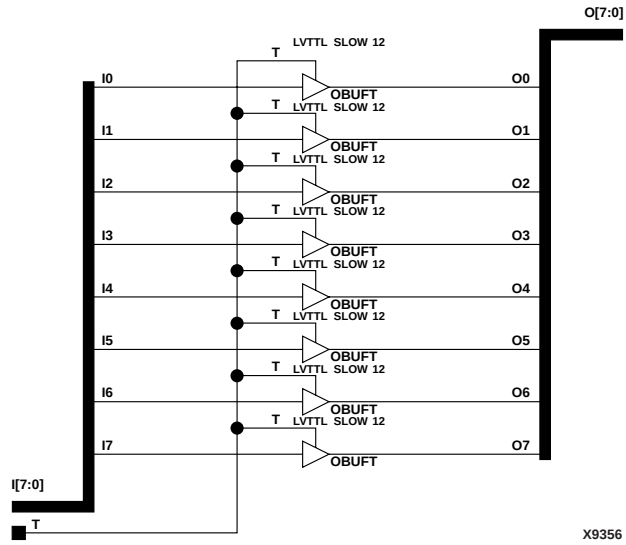
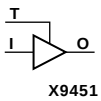


Figure 8-7 OBUFT8 Implementation Virtex-II, Virtex-II PRO

OBUFT_*selectIO*

Single 3-State Output Buffer with Active-Low Output Enable and Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



For Virtex, Virtex-E, Virtex-II, Virtex-II PRO, Spartan-II, and Spartan-IIE, OBUFT and its selectIO variants (listed in the "Components" column in the table below) are single 3-state output buffers with active-Low output Enable whose I/O interface corresponds to a specific I/O standard. The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. The S, F, and 2, 4, 6, 8, 12, 16, 24 extensions specify the slew rate (SLOW or FAST) and the drive power (2, 4, 6, 8, 12, 16, 24 mA) for the LVTTL standard. For example, OBUFT_S_4 is a 3-state output buffer with active-Low output enable that uses the LVTTL I/O signaling standard with a SLOW slew and 4mA of drive power. You can attach an IOSTANDARD attribute to an OBUFT instance instead of using an OBUFT_*selectIO* component. Check marks (√) in the "Spartan-II, Spartan-IIE, Virtex," and "Virtex-E" columns indicate the components and IOSTANDARD attribute values available for each architecture.

The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffers. See the "SelectI/O Usage Rules" under the IBUF_*selectIO* section for information on using these components and IOSTANDARD attributes.

Table 8-3 Spartan-II, Spartan-IIE, Virtex, and Virtex-E OBUFT_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II, Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Output VCCO
OBUFT	√	√	defaults to LVTTL	3.3
OBUFT_S_2	√	√	LVTTL [b]	3.3
OBUFT_S_4	√	√	LVTTL [b]	3.3
OBUFT_S_6	√	√	LVTTL [b]	3.3
OBUFT_S_8	√	√	LVTTL [b]	3.3
OBUFT_S_12	√	√	LVTTL [b]	3.3
OBUFT_S_16	√	√	LVTTL [b]	3.3
OBUFT_S_24	√	√	LVTTL [b]	3.3
OBUFT_F_2	√	√	LVTTL [b]	3.3
OBUFT_F_4	√	√	LVTTL [b]	3.3
OBUFT_F_6	√	√	LVTTL [b]	3.3
OBUFT_F_8	√	√	LVTTL [b]	3.3
OBUFT_F_12	√	√	LVTTL [b]	3.3
OBUFT_F_16	√	√	LVTTL [b]	3.3

Table 8-3 Spartan-II, Spartan-IIE, Virtex, and Virtex-E OBUFT_*selectIO* Components and IOSTANDARD Attributes

Component	Spartan-II, Spartan-IIE, Virtex	Virtex-E	IOSTANDARD (Attribute Value)	Output VCCO
OBUFT_F_24	√	√	LVTTL [b]	3.3
OBUFT_AGP	√	√	AGP	3.3
OBUFT_CTT	√	√	CTT	3.3
OBUFT_GTL	√	√	GTL	N / A
OBUFT_GTLP	√	√	GTLP	N / A
OBUFT_HSTL_I	√	√	HSTL_I	1.5
OBUFT_HSTL_III	√	√	HSTL_III	1.5
OBUFT_HSTL_IV	√	√	HSTL_IV	1.5
OBUFT_LVCMOS2	√		LVCMOS2	2.5
OBUFT_LVCMOS15		√	LVCMOS15 [b]	1.5
OBUFT_LVCMOS18		√	LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_F_2			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_F_4			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_F_6			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_F_8			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_F_12			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_S_2			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_S_4			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_S_6			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_S_8			LVCMOS18 [b]	1.8
OBUFT_LVCMOS18_S_12			LVCMOS18 [b]	1.8
OBUFT_LVDS		√	LVDS	2.5
OBUFT_LVPECL		√	LVPECL	3.3
OBUFT_LVTTL	√	√	LVTTL [b]	3.3
OBUFT_PCI33_3	√	√	PCI33_3	3.3
OBUFT_PCI33_5	√	√	PCI33_5	3.3
OBUFT_PCI66_3	√	√	PCI66_3	3.3
OBUFT_SSTL2_I	√	√	SSTL2_I	2.5
OBUFT_SSTL2_II	√	√	SSTL2_II	2.5
OBUFT_SSTL3_I	√	√	SSTL3_I	3.3
OBUFT_SSTL3_II	√	√	SSTL3_II	3.3

[b] The LVTTL, LVCMOS15, LVCMOS18, LVCMOS25, LVCMOS33 attributes also require a slew value (FAST or SLOW) and DRIVE value. See the FAST, SLOW, and DRIVE attribute descriptions in the *Xilinx Constraints Guide* for valid values for each architecture.

The Virtex-II and Virtex-II PRO library includes some OBUFT_*selectIO* components for compatibility with older, existing designs and other architectures. For new Virtex-II and Virtex-II PRO designs, however, the recommended method for using OBUFT selectI/O buffers is to attach an IOSTANDARD attribute to an OBUFT component.

For example, attach IOSTANDARD=GTLP to an OBUFT instead of using the OBUFT_GTLP component for new Virtex-II and Virtex-II PRO designs. The IOSTANDARD attributes that can be attached to an OBUFT component are listed in the "IOSTANDARD (Attribute Value)" column in Table 8-4. See the "SelectI/O Usage Rules" section for information on using these IOSTANDARD attributes.

Table 8-4 Virtex-II, Virtex-II PRO OBUFT_*selectIO* IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Terminate Type
OBUFT[a]	√	AGP	3.3	None
		*does not apply to Virtex-II PRO		
OBUFT[a]	√	F_12	3.3	None
OBUFT[a]	√	F_16	3.3	None
OBUFT[a]	√	F_2	3.3	None
OBUFT[a]	√	F_24	3.3	None
OBUFT[a]	√	F_4	3.3	None
OBUFT[a]	√	F_6	3.3	None
OBUFT[a]	√	F_8	3.3	None
OBUFT[a]	√	GTL	N/A	None
OBUFT[a]	√	GTL_DCI	1.2	Single
OBUFT[a]	√	GTLP	N/A	None
OBUFT[a]	√	GTLP_DCI	1.5	Single
OBUFT[a]	√	HSTL_I	1.5	None
OBUFT[a]	√	HSTL_I_18	1.8	None
OBUFT[a]	√	HSTL_I_DCI	1.5	Split
OBUFT[a]	√	HSTL_I_DCI_18	1.8	Split
OBUFT[a]	√	HSTL_II	1.5	None
OBUFT[a]	√	HSTL_II_18	1.8	None
OBUFT[a]	√	HSTL_II_DCI	1.5	Split
OBUFT[a]	√	HSTL_II_DCI_18	1.8	Split
OBUFT[a]	√	HSTL_III	1.5	None
OBUFT[a]	√	HSTL_III_18	1.8	None
OBUFT[a]	√	HSTL_III_DCI	1.5	Split
OBUFT[a]	√	HSTL_III_DCI_18	1.8	Split
OBUFT[a]	√	HSTL_IV	1.5	None
OBUFT[a]	√	HSTL_IV_18	1.8	None
OBUFT[a]	√	HSTL_IV_DCI	1.5	Split
OBUFT[a]	√	HSTL_IV_DCI_18	1.8	Split
OBUFT[a]	√	LVCMOS15 [b]	1.5	None
OBUFT[a]	√	LVCMOS15 _F_12[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _F_16[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _F_2[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _F_4[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _F_6[b]	1.5	None

Table 8-4 Virtex-II, Virtex-II PRO OBUFT_*selectIO* IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Terminate Type
OBUFT[a]	√	LVCMOS15 _F_8[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _S_12[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _S_16[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _S_2[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _S_4[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _S_6[b]	1.5	None
OBUFT[a]	√	LVCMOS15 _S_8[b]	1.5	None
OBUFT[a]	√	LVCMOS18 [b]	1.8	None
OBUFT[a]	√	LVCMOS18 _F_12[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _F_16[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _F_2[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _F_4[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _F_6[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _F_8[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _S_12[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _S_16[6b]	1.8	None
OBUFT[a]	√	LVCMOS18 _S_2[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _S_4[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _S_6[b]	1.8	None
OBUFT[a]	√	LVCMOS18 _S_8[b]	1.8	None
OBUFT[a]	√	LVCMOS2 [b]	2.5	None
OBUFT[a]	√	LVCMOS25 [b]	2.5	None
OBUFT[a]	√	LVCMOS25 _F_12[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _F_16[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _F_2[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _F_24[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _F_4[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _F_6[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _F_8[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _S_12[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _S_16[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _S_2[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _S_24[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _S_4[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _S_6[b]	2.5	None
OBUFT[a]	√	LVCMOS25 _S_8[b]	2.5	None
OBUFT[a]	√	LVCMOS33 [b]	3.3	None
OBUFT[a]	√	LVCMOS33 _F-12[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _F-16[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _F-2[b]	3.3	None

Table 8-4 Virtex-II, Virtex-II PRO OBUFT_*selectIO* IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Terminate Type
OBUFT[a]	√	LVCMOS33 _F-24[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _F-4[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _F-6[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _F-8[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _S-12[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _S-16[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _S-2[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _S-24[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _S-4[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _S-6[b]	3.3	None
OBUFT[a]	√	LVCMOS33 _S-8[b]	3.3	None
OBUFT[a]	√	LVDCI_15	1.5	Driver
OBUFT[a]	√	LVDCI_18	1.8	Driver
OBUFT[a]	√	LVDCI_25	2.5	Driver
OBUFT[a]	√	LVDCI_33	3.3	Driver
OBUFT[a]	√	LVDCI_DV2_15	1.5	Driver
OBUFT[a]	√	LVDCI_DV2_18	1.8	Driver
OBUFT[a]	√	LVDCI_DV2_25	2.5	Driver
OBUFT[a]	√	LVDCI_DV2_33	3.3	Driver
OBUFT[a]	√	LVTTL [b]	3.3	None
OBUFT[a]	√	LVTTL _F_12[b]	3.3	None
OBUFT[a]	√	LVTTL _F_16[b]	3.3	None
OBUFT[a]	√	LVTTL _F_2[b]	3.3	None
OBUFT[a]	√	LVTTL _F_24[b]	3.3	None
OBUFT[a]	√	LVTTL _F_4[b]	3.3	None
OBUFT[a]	√	LVTTL _F_6[b]	3.3	None
OBUFT[a]	√	LVTTL _F_8[b]	3.3	None
OBUFT[a]	√	LVTTL _S_12[b]	3.3	None
OBUFT[a]	√	LVTTL _S_16[b]	3.3	None
OBUFT[a]	√	LVTTL _S_2[b]	3.3	None
OBUFT[a]	√	LVTTL _S_24[b]	3.3	None
OBUFT[a]	√	LVTTL _S_4[b]	3.3	None
OBUFT[a]	√	LVTTL _S_6[b]	3.3	None
OBUFT[a]	√	LVTTL _S_8[b]	3.3	None
OBUFT[a]	√	PCI33_3	3.3	None
OBUFT[a]	√	PCI66_3	3.3	None
OBUFT[a]	√	PCIX	3.3	None
OBUFT[a]	√	SSTL2_I	2.5	None
OBUFT[a]	√	SSTL2_I_DCI	2.5	Split
OBUFT[a]	√	SSTL2_II	2.5	None

Table 8-4 Virtex-II, Virtex-II PRO OBUFT_*selectIO* IOSTANDARD Attributes

Component	Virtex-II, Virtex-II PRO	IOSTANDARD (Attribute Value)	Output VCCO	Terminate Type
OBUFT[a]	√	SSTL2_II_DCI	2.5	Split
OBUFT[a]	√	SSTL3_I	3.3	None
OBUFT[a]	√	SSTL3_I_DCI	3.3	Split
OBUFT[a]	√	SSTL3_II	3.3	None
OBUFT[a]	√	SSTL3_II_DCI	3.3	Split
OBUFT[a]	√	S_12	3.3	None
OBUFT[a]	√	S_16	3.3	None
OBUFT[a]	√	S_2	3.3	None
OBUFT[a]	√	S_24	3.3	None
OBUFT[a]	√	S_4	3.3	None

[a]Attach an IOSTANDARD attribute to an OBUFT and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the output for the I/O standard associated with that value.

[b] The LVTTL, LVCMOS15, LVCMOS18, LVCMOS25, LVCMOS33 attributes also require a slew value (FAST or SLOW) and DRIVE value. See the FAST, SLOW, and DRIVE attribute descriptions in the *Xilinx Constraints Guide* for valid values for each architecture.

OBUFT and its variants have selectable drive and slew rates using the DRIVE and FAST or SLOW constraints. The defaults are DRIVE=12 mA and SLOW slew.

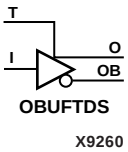
When T is Low, data on the input of the buffer is transferred to the output. When T is High, the output is high impedance (off or Z state). OBUFTs isolate the internal circuit and provide extra drive current for signals leaving a chip. An OBUFT_*selectIO* output is connected to an OPAD or an IOPAD.

Inputs		Output
T	I	O
1	X	Z
0	1	1
0	0	0

OBUFTDS

3-State Differential Signaling Output Buffer with Active Low Output Enable and Selectable I/O Interface

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



OBUFTDS is a single 3-state, differential signaling output buffer with active Low enable and a selectIO interface.

When T is Low, data on the input of the buffer is transferred to the output. When T is High, both outputs are high impedance (off or Z state).

Inputs		Outputs	
I	T	O	OB
X	1	Z	Z
0	0	0	1
1	0	1	0

The IOSTANDARD attribute values listed in the following table can be applied to an IBUFGDS component to provide *selectIO* interface capability. See the *Xilinx Constraints Guide* for information using these attributes. The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffer components. See the "SelectI/O Usage Rules" under the IBUF_*selectIO* section for information on using these IOSTANDARD attributes.

Component	IOSTANDARD (Attribute Value)	Output VCCO	VREF	Terminate Type
OBUFTDS[a]	BLVDS_25	2.5	N/A	None
OBUFTDS[a]	LDT_25	2.5	N/A	None
OBUFTDS[a]	LVDS_25 (default)	2.5	N/A	None
OBUFTDS[a]	LVDS_33*	3.3	N/A	None
	*does not apply to Virtex-II PRO			
OBUFTDS[a]	LVPECL_33*	3.3	N/A	None
	*does not apply to Virtex-II PRO			
OBUFTDS[a]	LVDSEXT_25	2.5	N/A	None
OBUFTDS[a]	LVDSEXT_33*	3.3	N/A	None
	*does not apply to Virtex-II PRO			

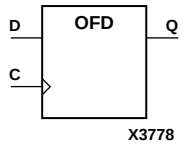
Component	IOSTANDARD (Attribute Value)	Output VCCO	VREF	Terminate Type
OBUFTDS[a]	ULVDS_25	2.5	N/A	None

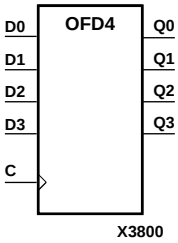
[a]Attach an IOSTANDARD attribute to an OBUFTDS and assign the value indicated in the "IOSTANDARD (Attribute Value)" column to program the outputs for the I/O standard associated with that value.

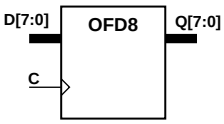
OFD, 4, 8, 16

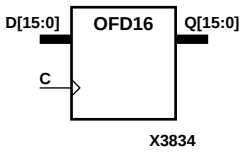
Single- and Multiple-Output D Flip-Flops

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OFD	Macro	Macro	Macro	Macro	Macro	Macro
OFD4, OFD8, OFD16	Macro	Macro	Macro	Macro	Macro	Macro









OFD, OFD4, OFD8, and OFD16 are single and multiple output D flip-flops except for XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II

The outputs (for example, Q3 – Q0) are connected to OPADs or IOPADs. The data on the D inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the Q outputs.

The flip-flops are asynchronously cleared with Low outputs when power is applied.

For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	C	Q
D	↑	dn

dn = state of referenced input one setup time prior to active clock transition

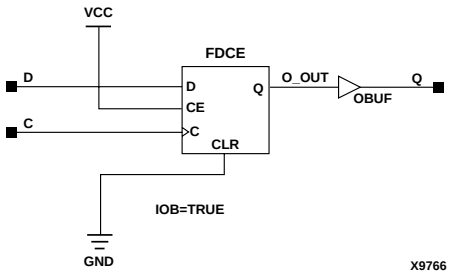


Figure 8-8 OFD Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

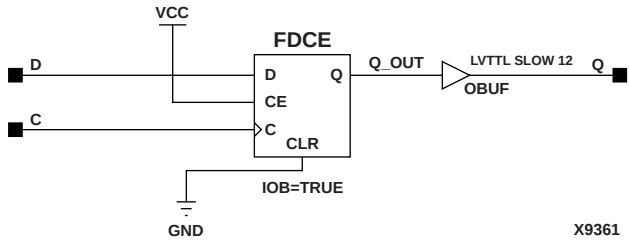


Figure 8-9 OFD Implementation Virtex-II, Virtex-II PRO

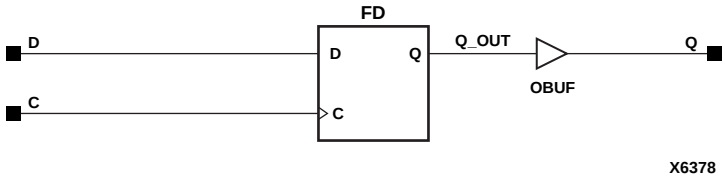


Figure 8-10 OFD Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

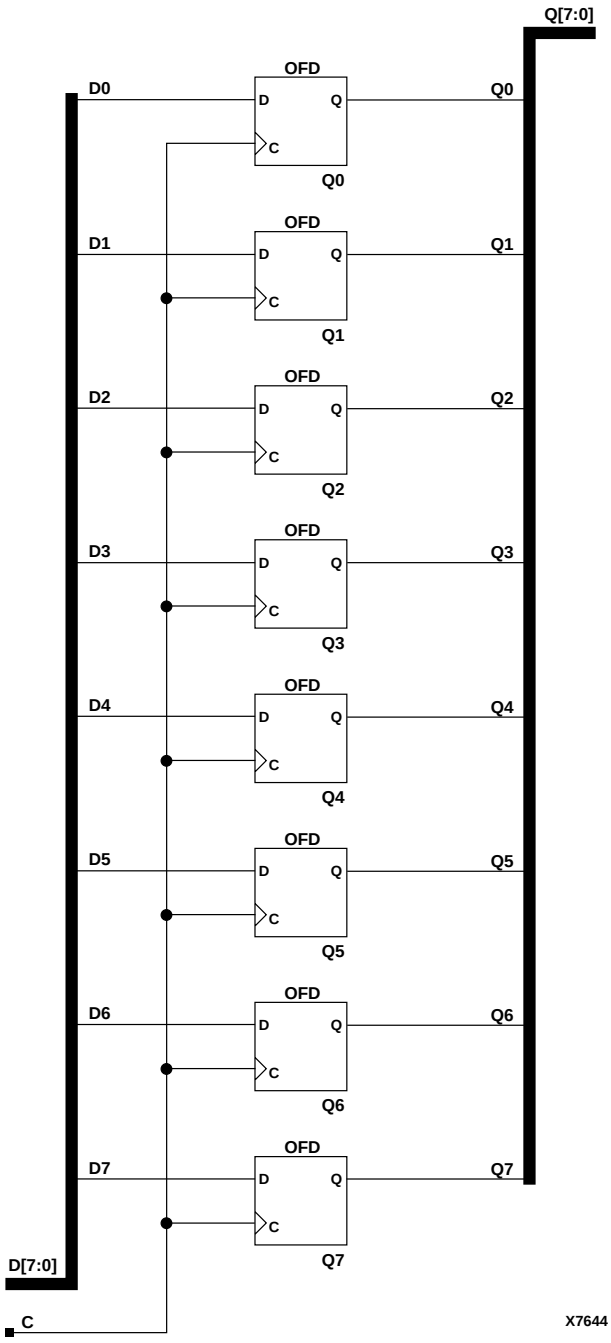


Figure 8-11 OFD8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

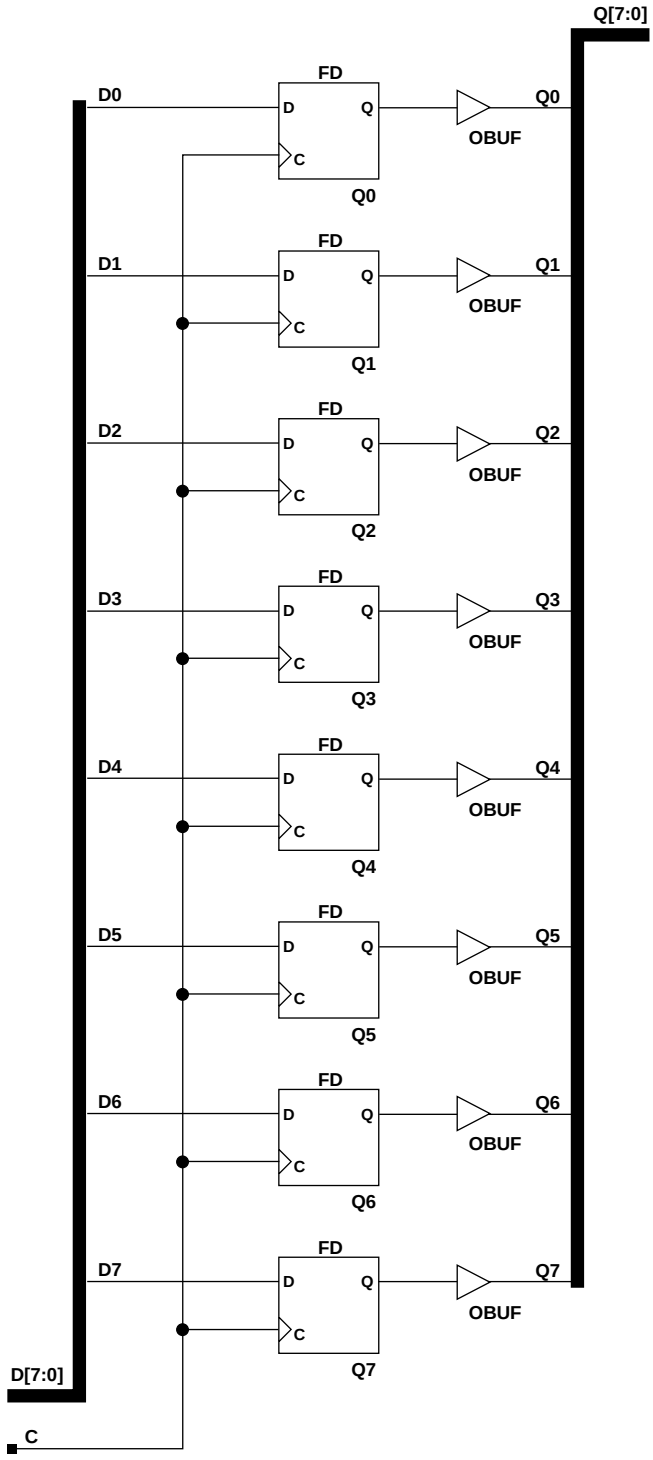
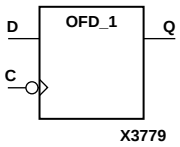


Figure 8-12 OFD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

OFD_1

Output D Flip-Flop with Inverted Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



OFD_1 is located in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output.

The flip-flop is asynchronously cleared, output Low, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	C	Q
D	↓	d

d = state of referenced input one setup time prior to active clock transition

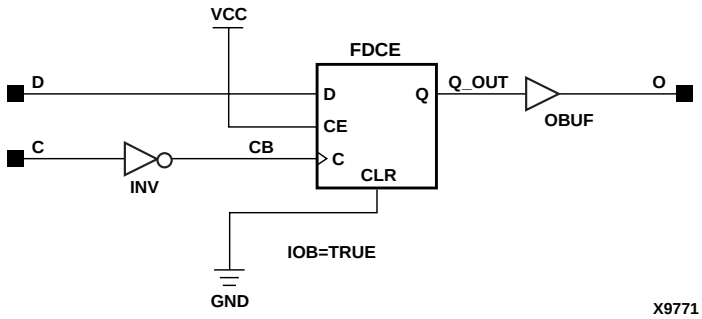
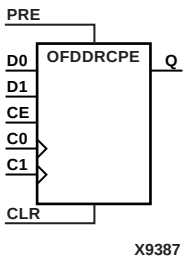


Figure 8-13 OFD_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

OFDDRCPE

Dual Data Rate Output D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



OFDDRCPE is a dual data rate (DDR) output D flip-flop with clock enable (CE) and asynchronous preset (PRE) and clear (CLR). It consists of one output buffer and one dual data rate flip-flop (FDDRCPE).

When the asynchronous PRE is High and CLR is Low, the Q output is preset High. When CLR is High, Q is set Low. Data on the D0 input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High C0 clock transition. Data on the D1 input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High C1 clock transition.

The INIT attribute does not apply to OFDDRCPE components.

The flip-flops are asynchronously cleared with Low outputs when power is applied.

Inputs							Outputs
C0	C1	CE	D0	D1	CLR	PRE	Q
X	X	X	X	X	1	0	0
X	X	X	X	X	0	1	1
X	X	X	X	X	1	1	0
X	X	0	X	X	0	0	No Chg
↑	X	1	D0	X	0	0	D0
X	↑	1	X	D1	0	0	D1

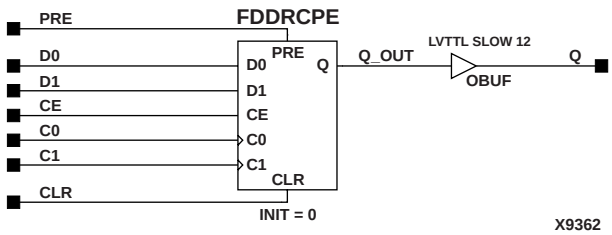
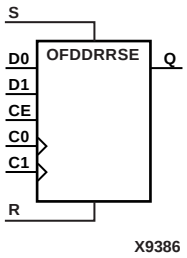


Figure 8-14 OFDDRCPE Implementation Virtex-II, Virtex-II PRO

OFDDRRSE

Dual Data Rate Output D Flip-Flop with Synchronous Reset and Set and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



OFDDRRSE is a dual data rate (DDR) output D flip-flop with synchronous reset (R) and set (S) and clock enable (CE). It consists of one output buffer and one dual data rate flip-flop (FDDRRSE).

On a Low-to-High clock transition (C0 or C1), a High R input resets the Q output Low; a Low R input with a High S input sets Q High. When both R and S are Low and clock enable is High, data on the D0 input is loaded into the flip-flop on a Low-to-High C0 clock transition and data on the D1 input is loaded into the flip-flop on a Low-to-High C1 clock transition.

The flip-flops are asynchronously cleared with Low outputs when power is applied.

The INIT attribute does not apply to OFDDRRSE components.

Inputs							Outputs
C0	C1	CE	D0	D1	R	S	Q
↑	X	X	X	X	1	0	0
↑	X	X	X	X	0	1	1
↑	X	X	X	X	1	1	0
X	↑	X	X	X	1	0	0
X	↑	X	X	X	0	1	1
X	↑	X	X	X	1	1	0
X	X	0	X	X	0	0	No Chg
↑	X	1	D0	X	0	0	D0
X	↑	1	X	D1	0	0	D1

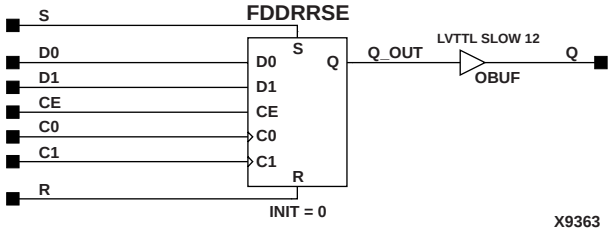
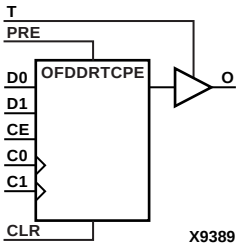


Figure 8-15 OFDDRRSE Implementation Virtex-II, Virtex-II PRO

OFDDRTCPE

Dual Data Rate D Flip-Flop with Active-Low 3-State Output Buffer, Clock Enable, and Asynchronous Preset and Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



OFDDRTCPE is a dual data rate (DDR) D flip-flop with clock enable (CE) and asynchronous preset and clear whose output is enabled by a 3-state buffer. It consists of a dual data rate flip-flop (FDDRCPE) and a 3-state output buffer (OBUFT). The data output (O) of the flip-flop is connected to the input of the output buffer (OBUFT). The output of the OBUFT is connected to an OPAD or IOPAD.

When the active-Low enable input (T) is Low, output is enabled and the data on the flip-flop's Q output appears on the OBUFT's O output. When the asynchronous PRE is High and CLR is Low, the O output is preset High. When CLR is High, O is set Low. Data on the D0 input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High C0 clock transition. Data on the D1 input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High C1 clock transition.

When T is High, outputs are high impedance (Off). When CE is Low and T is Low, the outputs do not change.

The flip-flops are asynchronously cleared with Low outputs when power is applied.

The INIT attribute does not apply to OFDDRTCPE components.

Inputs								Outputs
C0	C1	CE	D0	D1	CLR	PRE	T	O
X	X	X	X	X	X	X	1	Z
X	X	X	X	X	1	0	0	0
X	X	X	X	X	0	1	0	1
X	X	X	X	X	1	1	0	0
X	X	0	X	X	0	0	0	No Chg
↑	X	1	D0	X	0	0	0	D0
X	↑	1	X	D1	0	0	0	D1

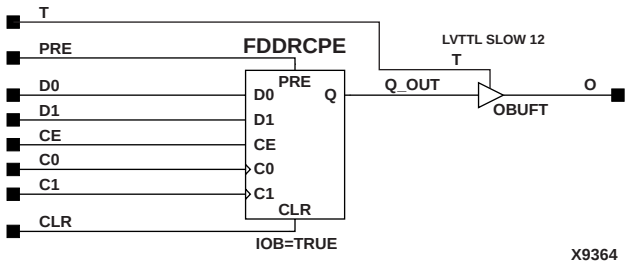
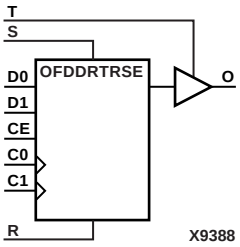


Figure 8-16 OFDDRTCPE Implementation Virtex-II, Virtex-II PRO

OFDDRTRSE

Dual Data Rate D Flip-Flop with Active-Low 3-State Output Buffer, Synchronous Reset and Set, and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



OFDDRTRSE is a dual data rate (DDR) D flip-flop with clock enable (CE) and synchronous reset and set whose output is enabled by a 3-state buffer. It consists of a dual data rate flip-flop (FDDRRSE) and a 3-state output buffer (OBUFT). The data output (O) of the flip-flop is connected to the input of the output buffer (OBUFT). The output of the OBUFT is connected to an OPAD or IOPAD

When the active-Low enable input (T) is Low, output is enabled and the data on the flip-flop's Q output appears on the OBUFT's O output. On a Low-to-High clock transition (C0 or C1), a High R input resets the Q output Low; a Low R input with a High S input sets O High. When both R and S are Low and clock enable is High, data on the D0 input is loaded into the flip-flop on a Low-to-High C0 clock transition and data on the D1 input is loaded into the flip-flop on a Low-to-High C1 clock transition.

When T is High, outputs are high impedance (Off). When CE is Low and T is Low, the outputs do not change.

The flip-flops are asynchronously cleared with Low outputs when power is applied.

The INIT attribute does not apply to OFDDRTRSE components.

Inputs								Outputs
C0	C1	CE	D0	D1	R	S	T	O
X	X	X	X	X	X	X	1	Z
↑	X	X	X	X	1	0	0	0
↑	X	X	X	X	0	1	0	1
↑	X	X	X	X	1	1	0	0
X	↑	X	X	X	1	0	0	0
X	↑	X	X	X	0	1	0	1
X	↑	X	X	X	1	1	0	0
X	X	0	X	X	0	0	0	No Chg
↑	X	1	D0	X	0	0	0	D0
X	↑	1	X	D1	0	0	0	D1

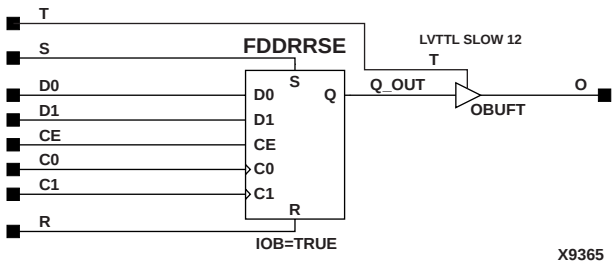
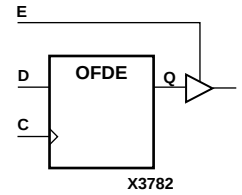


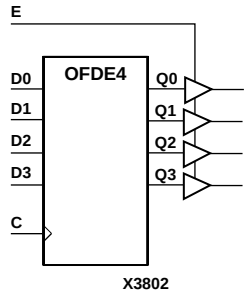
Figure 8-17 OFDDRTRSE Implementation Virtex-II, Virtex-II PRO

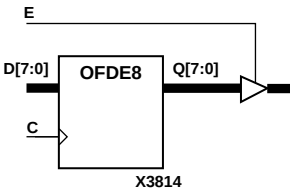
OFDE, 4, 8, 16

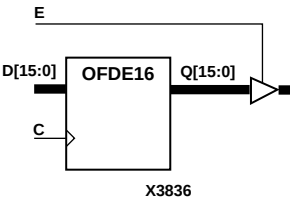
D Flip-Flops with Active-High Enable Output Buffers

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OFDE, OFDE4, OFDE8, OFDE16	Macro	Macro	Macro	Macro	Macro	Macro









OFDE, OFDE4, OFDE8, and OFDE16 are single or multiple D flip-flops whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the O outputs. When E is Low, outputs are high impedance (Z state or Off).

The flip-flops are asynchronously cleared with Low outputs when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
E	D	C	O
0	X	X	Z, not off
1	1	↑	1
1	0	↑	0

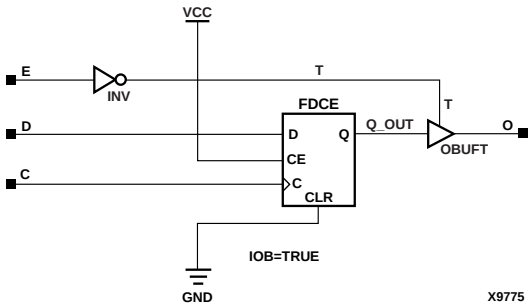


Figure 8-18 OFDE Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

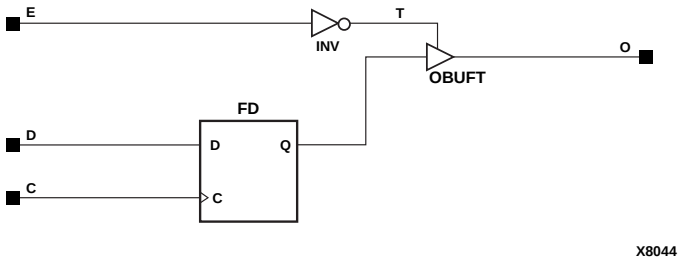


Figure 8-19 OFDE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

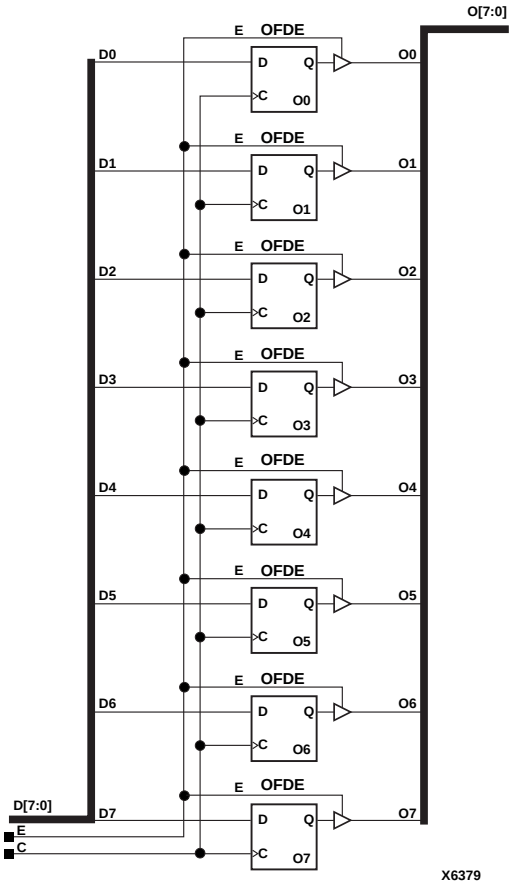
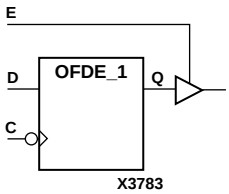


Figure 8-20 OFDE8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

OFDE_1

D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



OFDE_1 and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or Off).

The flip-flop is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	1	↓	1
1	0	↓	0

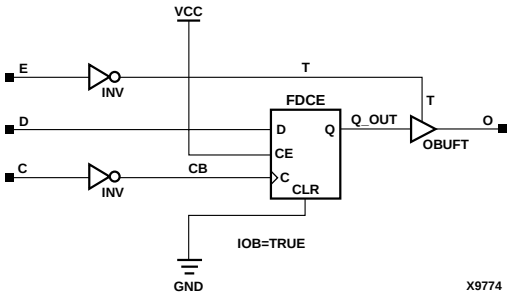


Figure 8-21 OFDE_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

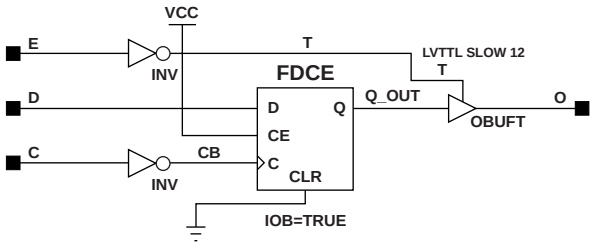
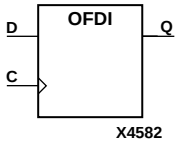


Figure 8-22 OFDE_1 Implementation Virtex-II, Virtex-II PRO

OFDI

Output D Flip-Flop (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



OFDI is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q).

The flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	**C**	**Q**
D	↑	d

d = state of referenced input one setup time prior to active clock transition

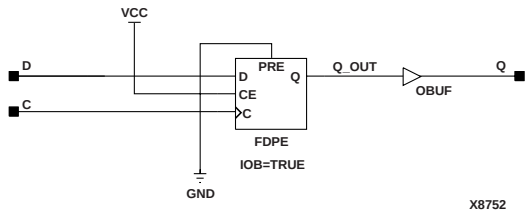


Figure 8-23 OFDI Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

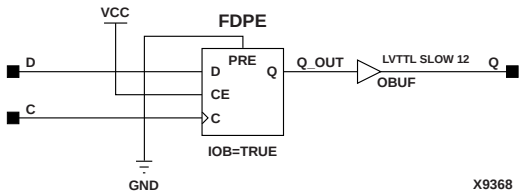
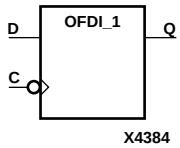


Figure 8-24 OFDI Implementation Virtex-II, Virtex-II PRO

OFDI_1

Output D Flip-Flop with Inverted Clock (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



OFDI_1 exists in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output.

The flip-flop is asynchronously preset, output High, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs		Outputs
D	C	Q
D	↓	d

d = state of referenced input one setup time prior to the active clock transition

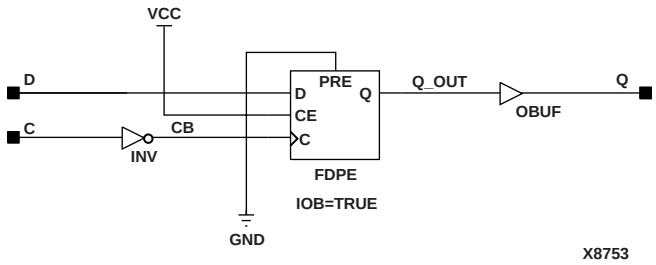


Figure 8-25 OFDI_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

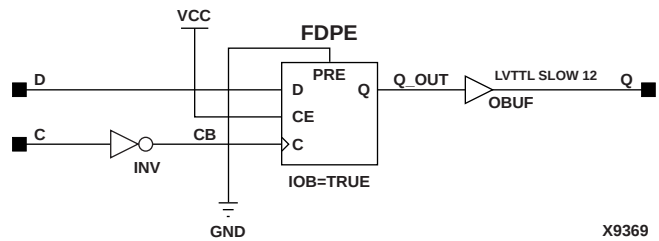
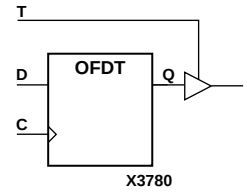


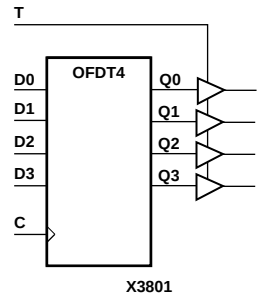
Figure 8-26 OFDI_1 Implementation Virtex-II, Virtex-II PRO

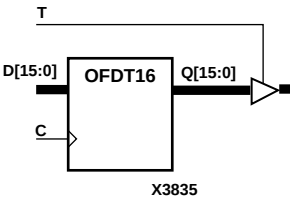
OFDT, 4, 8, 16

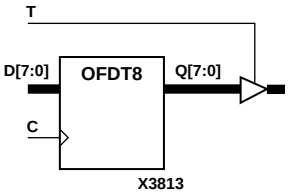
Single and Multiple D Flip-Flops with Active-Low 3-State Output Enable Buffers

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OFDT	Macro	Macro	Macro	Macro	Macro	Macro
OFDT4, OFDT8, OFDT16	Macro	Macro	Macro	Macro	Macro	Macro









OFDT, OFDT4, OFDT8, and OFDT16 are single or multiple D flip-flops whose outputs are enabled by a 3-state buffers. The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the O outputs. When T is High, outputs are high impedance (Off).

The flip-flops are asynchronously cleared with Low outputs, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	d

d = state of referenced input one setup time prior to active clock transition

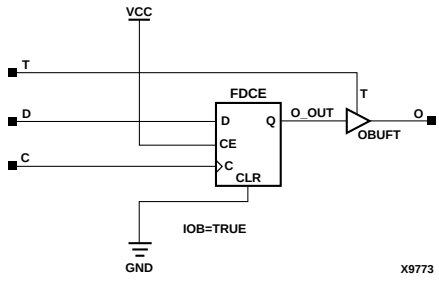


Figure 8-27 OFDT Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

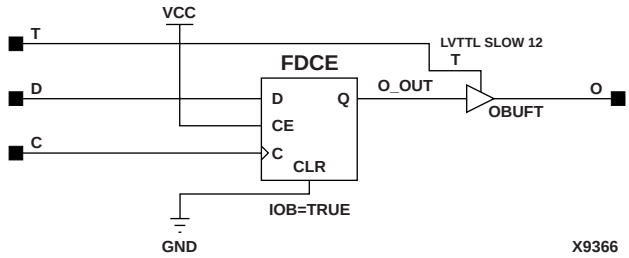


Figure 8-28 OFDT Implementation Virtex-II, Virtex-II PRO

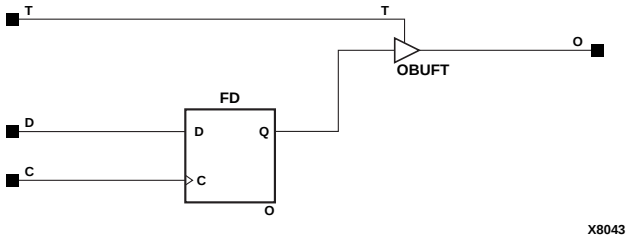


Figure 8-29 OFDT Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

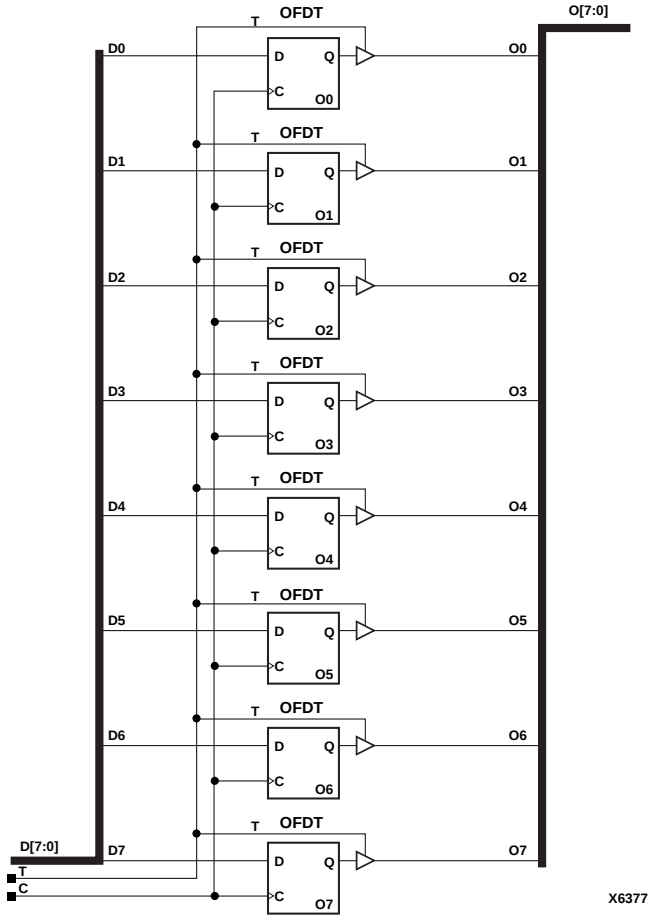
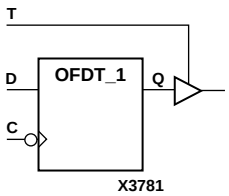


Figure 8-30 OFDT8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

OFDT_1

D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



OFDT_1 and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the O output. When T is High, the output is high impedance (Off).

The flip-flop is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	1	↓	1
0	0	↓	0

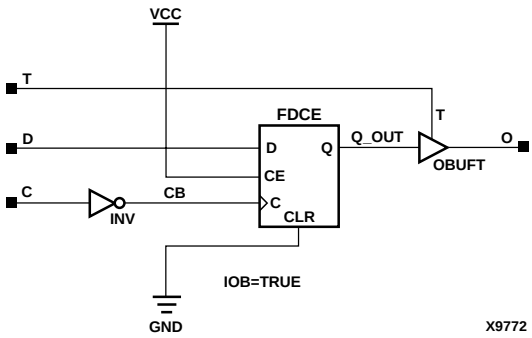


Figure 8-31 OFDT_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

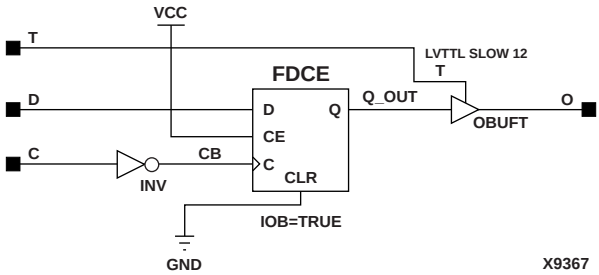
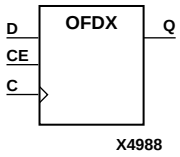


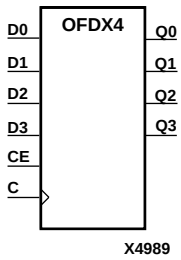
Figure 8-32 OFDT_1 Implementation Virtex-II, Virtex-II PRO

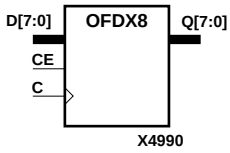
OFDX, 4, 8, 16

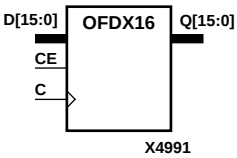
Single- and Multiple-Output D Flip-Flops with Clock Enable

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OFDX	Macro	Macro	Macro	N/A	N/A	N/A
OFDX4, OFDX8, OFDX16	Macro	Macro	Macro	N/A	N/A	N/A









OFDX, OFDX4, OFDX8, and OFDX16 are single and multiple output D flip-flops. The Q outputs are connected to OPADs or IOPADs. The data on the D inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the Q outputs. When CE is Low, flip-flop outputs do not change.

The flip-flops are asynchronously cleared with Low outputs, when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CE	D	C	Q
1	D	↑	dn
0	X	X	No Chg

dn = state of referenced input one setup time prior to active clock transition

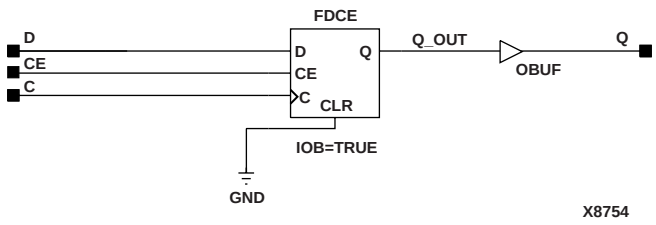


Figure 8-33 OFDX Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

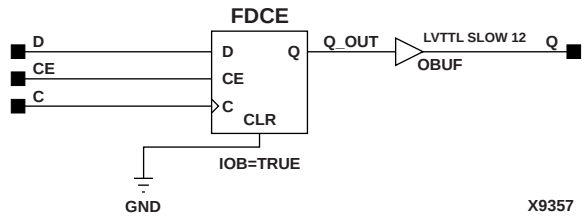


Figure 8-34 OFDX Implementation Virtex-II, Virtex-II PRO

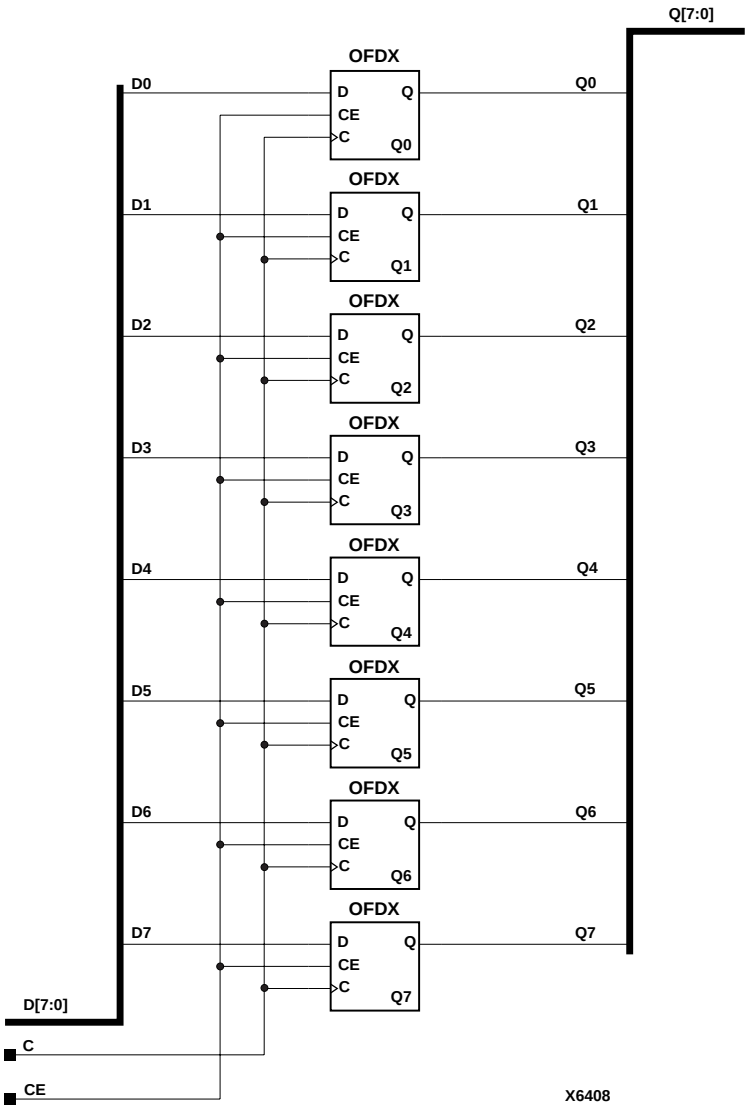
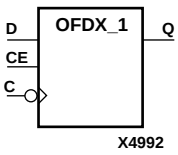


Figure 8-35 OFDX8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

OFDX_1

Output D Flip-Flop with Inverted Clock and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



OFDX_1 is located in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously cleared with Low output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CE	D	C	Q
1	D	↓	d
0	X	X	No Chg

d = state of referenced input one setup time prior to active clock transition

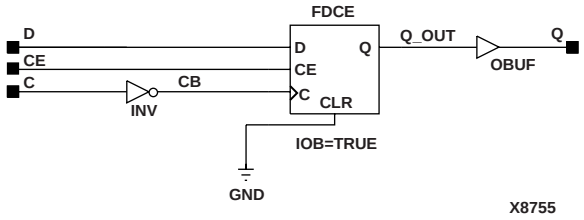


Figure 8-36 OFDX_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

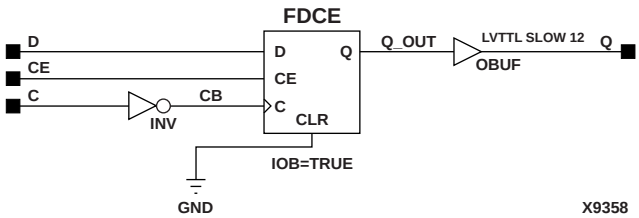
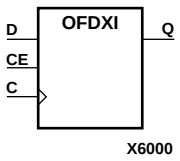


Figure 8-37 OFDX_1 Implementation Virtex-II, Virtex-II PRO

OFDXI

Output D Flip-Flop with Clock Enable (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



OFDXI is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). When CE is Low, the output does not change.

The flip-flop is asynchronously preset with High output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CE	D	C	Q
1	D	↑	d
0	X	X	No Chg

d = state of referenced input one setup time prior to active clock transition

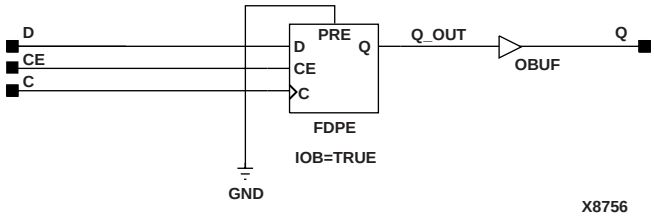


Figure 8-38 OFDXI Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

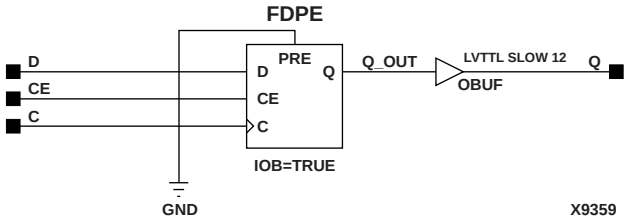
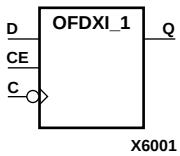


Figure 8-39 OFDXI Implementation Virtex-II, Virtex-II PRO

OFDXI_1

Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



OFDXI_1 is located in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When CE is Low, the output (Q) does not change.

The flip-flop is asynchronously preset with High output when power is applied.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs			Outputs
CE	D	C	Q
1	D	↓	d
0	X	X	No Chg

d = state of referenced input one setup time prior to active clock transition

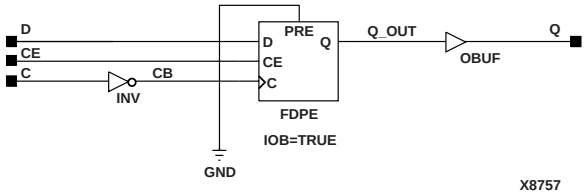


Figure 8-40 OFDXI_1 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

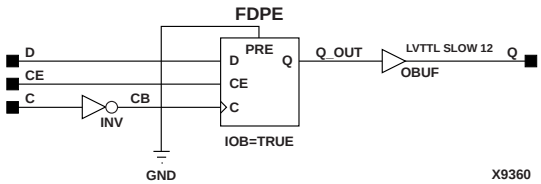
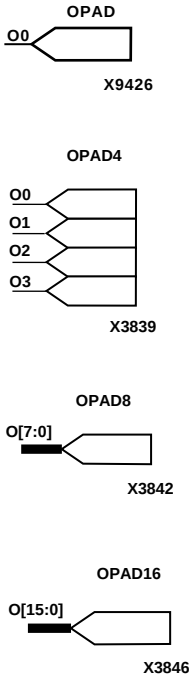


Figure 8-41 OFDXI_1 Implementation Virtex-II, Virtex-II PRO

OPAD, 4, 8, 16

Single- and Multiple-Output Pads

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OPAD	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OPAD4, OPAD8, OPAD16	Macro	Macro	Macro	Macro	Macro	Macro



OPAD, OPAD4, OPAD8, and OPAD16 are single and multiple output pads. An OPAD connects a device pin to an output signal of a PLD. It is internally connected to an input/output block (IOB), which is configured by the software as an OBUF, an OBUFT, an OBUFE, an OFD, or an OFDT.

See the appropriate CAE tool interface user guide for details on assigning pin location and identification.

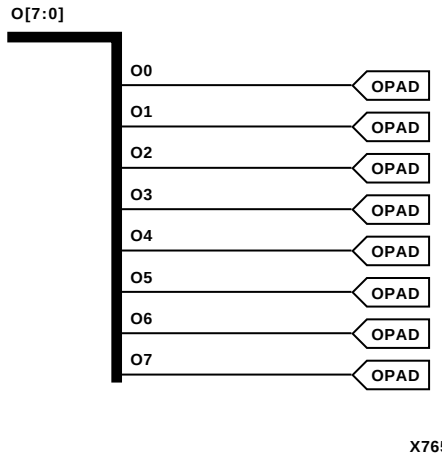


Figure 8-42 OPAD8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

OR2-9

2- to 9-Input OR Gates with Inverted and Non-Inverted Inputs

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
OR2, OR2B1, OR2B2, OR3, OR3B1, OR3B2, OR3B3, OR4, OR4B1, OR4B2, OR4B3, OR4B4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR5, OR5B1, OR5B2, OR5B3, OR5B4, OR5B5	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR6, OR7, OR8, OR9	Macro	Macro	Macro	Primitive	Primitive	Primitive

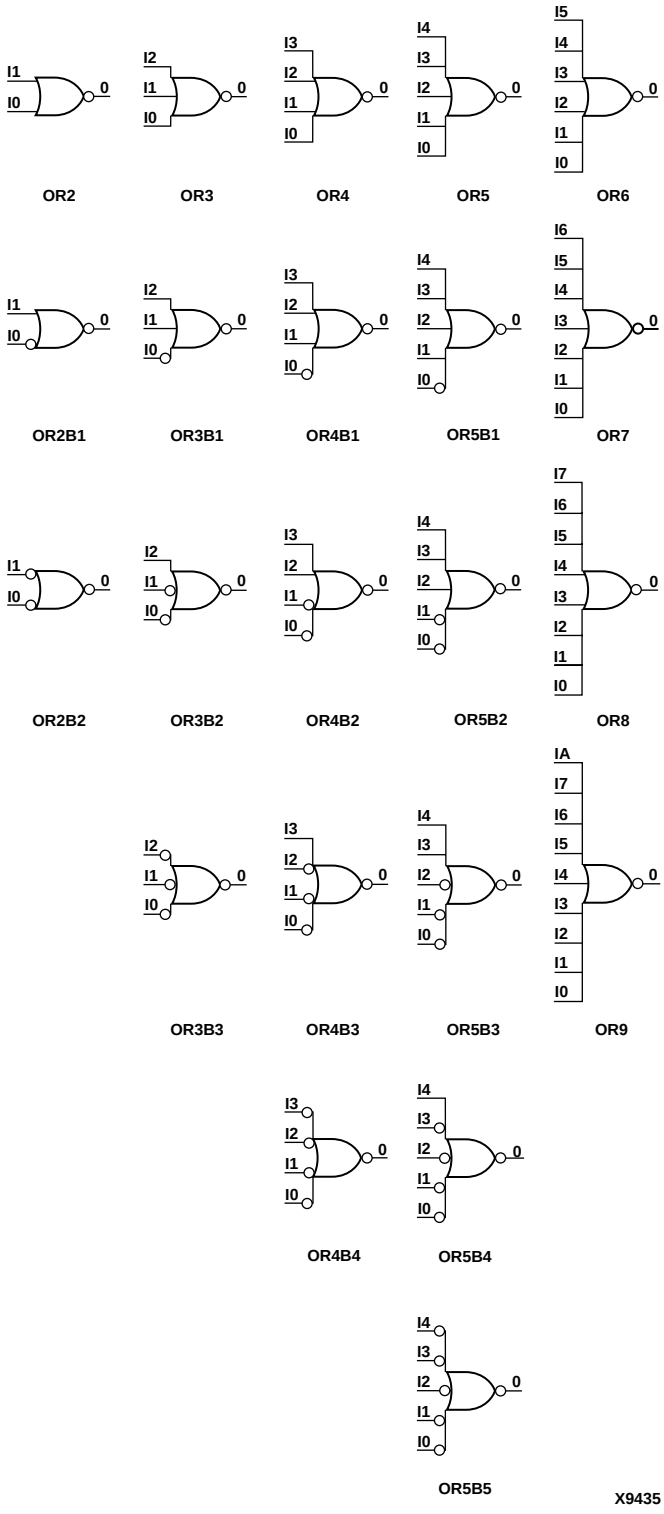


Figure 8-43 OR Gate Representations

The OR function is performed in the Configurable Logic Block (CLB) function generators for Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO. OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Since each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

See the "OR12, 16" section for information on additional OR functions for the Spartan-II, Spartan-IIE, Virtex, and Virtex-E.

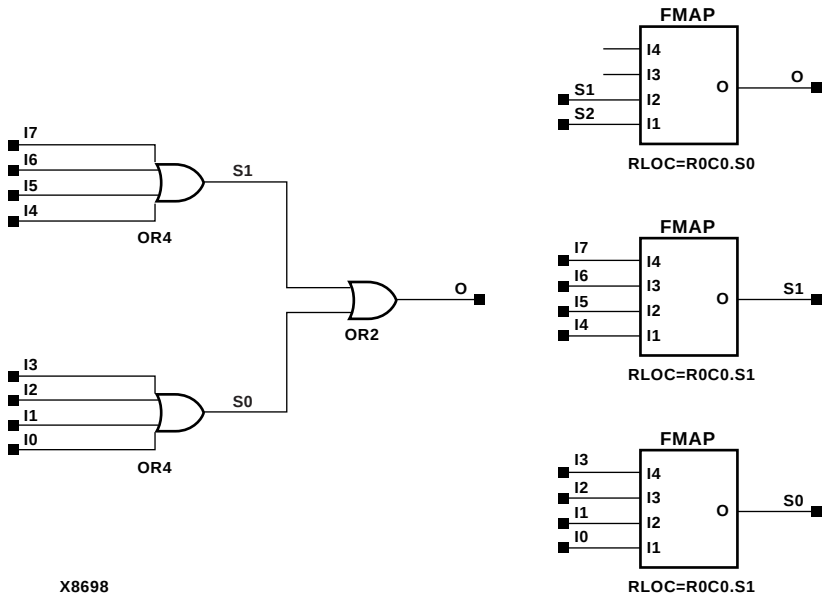


Figure 8-44 OR8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

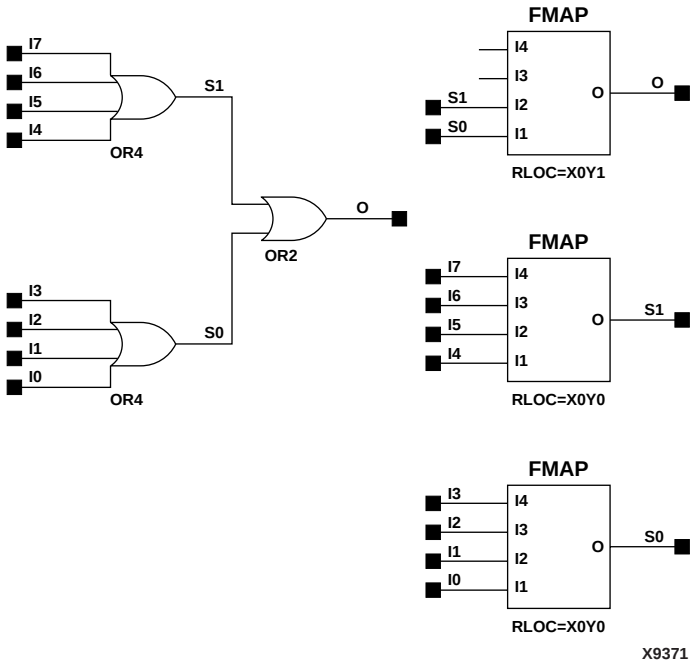
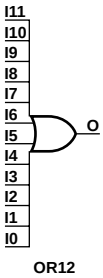


Figure 8-45 OR8 Implementation Virtex-II, Virtex-II PRO

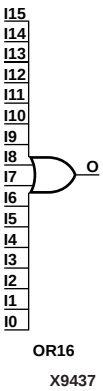
OR12, 16

12- and 16-Input OR Gates with Non-Inverted Inputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



See the "OR2-9" section for information on OR functions.



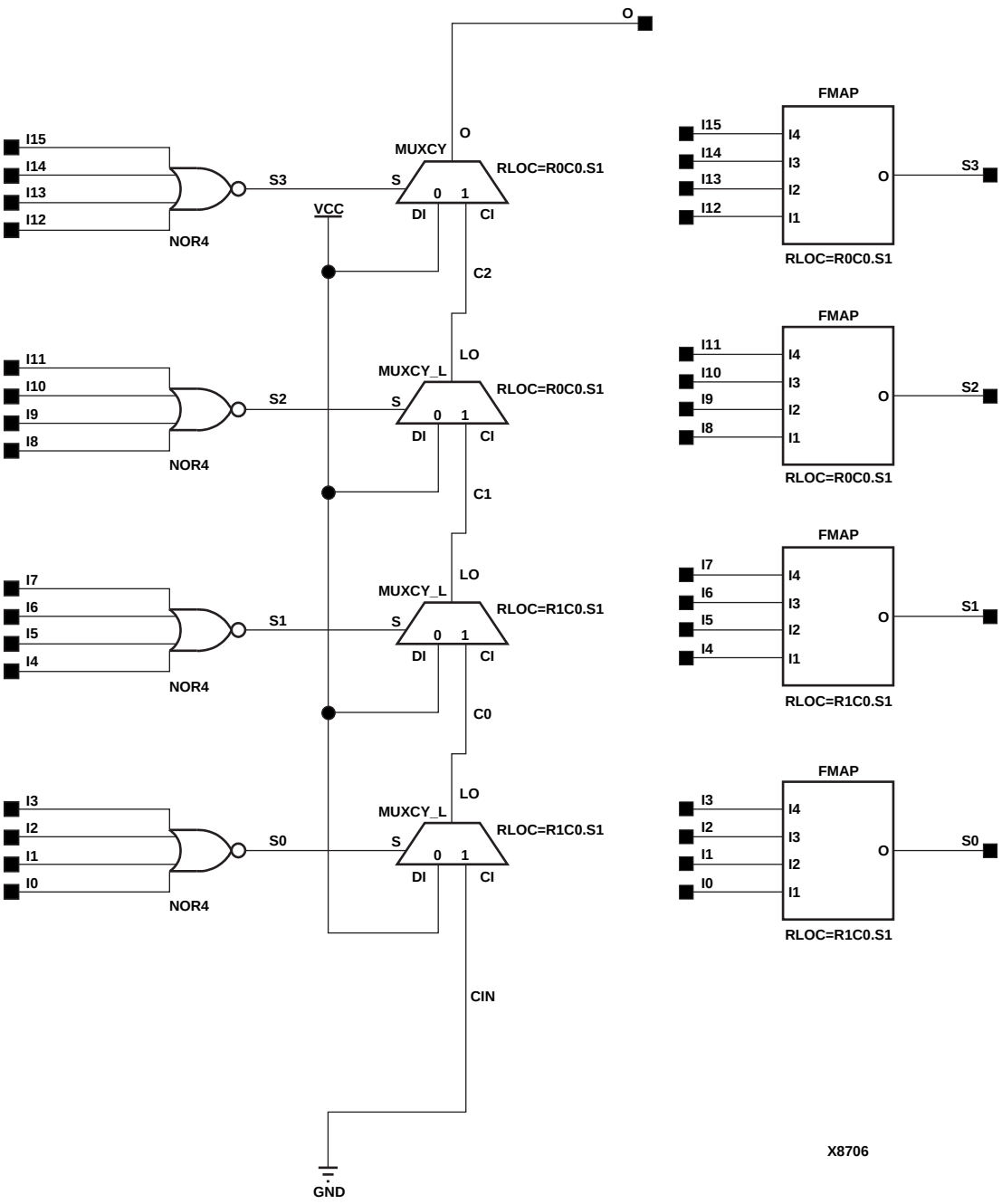


Figure 8-46 OR16 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

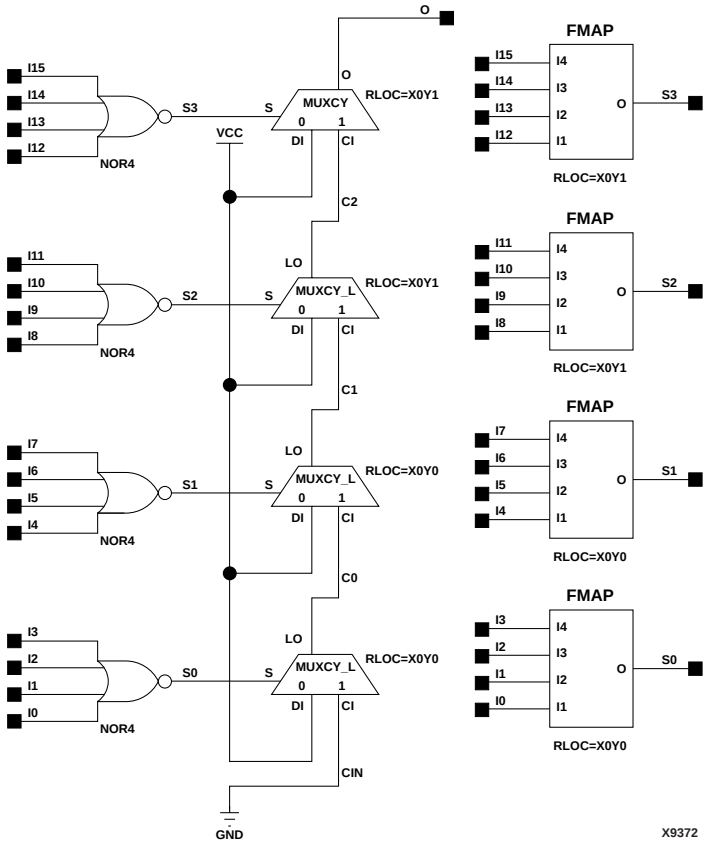
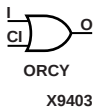


Figure 8-47 OR16 Implementation Virtex-II, Virtex-II PRO

ORCY

OR with Carry Logic

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



ORCY is a special OR with general O output used for generating faster and smaller arithmetic functions.

Each Virtex-II and Virtex-II PRO slice contains a dedicated 2-input OR gate that ORs together carry out values for a series of horizontally adjacent carry chains. The OR gate gets one input external to the slice and the other input from the output of the high order carry mux. The OR gate's output drives the next slice's OR gate horizontally across the die.

Only MUXCY outputs can drive the signal on the CI pin. Only ORCY outputs or logic zero can drive the I pin.

Chapter 9

PPC405 to ROM256X1

PPC405

Primitive for the Power PC Core

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO*	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

*Not supported for Virtex-II. Only supported for Virtex-II PRO.

The PowerPC 405 embedded core is a 32-bit RISC core integrating a PowerPC 405 CPU, separate instruction and data caches, a JTAG port, trace FIFO, multiple timers, and a memory management unit (MMU). Integrated on-chip memory (OCM) controllers provide dedicated interfaces between Block SelectRAM memory and the processor core instruction and data paths for high-speed access. The PowerPC 405 core implements the PowerPC User Instruction Set.

For complete information about the PowerPC 405, see the following documents:

- Virtex-II Pro Datasheet
- Virtex-II Pro Handbook
- The PowerPC 405 Core Processor Block Manual
- The PowerPC 405 User Guide

The following table lists the inputs and outputs of the primitive. For detailed information about the pinouts, see the DS083 Virtex-II PRO Data Sheet.

Inputs	Outputs
BRAMDSOCMCLK	C405CPMCORESLEEPREQ
BRAMDSOCMRDDBUS [0:31]	C405CPMMSRCE
BRAMISOCMCLK	C405CPMMSREE
BRAMISOCMRDDBUS [0:63]	C405CPMTIMERIRQ
CPMC405CLOCK	C405CPMTIMERRESETREQ
CPMC405CORECLKINACTIVE	C405DBGMSRWE
CPMC405CPUCLKEN	C405DBGSTOPACK
CPMC405JTAGCLKEN	C405DBGWBCOMPLETE
CPMC405TIMERCLKEN	C405DBGWBFULL

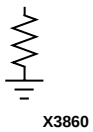
Inputs	Outputs
CPMC405TIMERTICK	C405DBGWBIAR[0:29]
DBGC405DEBUGHALT	C405DCRABUS [0:9]
DBGC405EXTBUSHOLDACK	C405DCRDBUSOUT [0:31]
DBGC405UNCONDDEBUGEVENT	C405DCRREAD
DCRC405ACK	C405DCRWRITE
DCRC405DBUSIN [0:31]	C405JTGCAPTUREDR
DSARCVALUE [0:7]	C405JTGEXTEST
DSCNTLVALUE [0:7]	C405JTGPGMOUT
EICC405CRITINPUTIRQ	C405JTGSHIFTDR
EICC405EXTINPUTIRQ	C405JTGTDO
ISARCVALUE [0:7]	C405JTGTDOEN
ISCNTLVALUE [0:7]	C405JTGUPDATEDR
JTGC405BNDSCANTDO	C405PLBDCUABORT
JTGC405TCK	C405PLBDCUABUS [0:31]
JTGC405TDI	C405PLBDCUBE [0:7]
JTGC405TMS	C405PLBDCUCACHEABLE
JTGC405TRSTNEG	C405PLBDCUGUARDED
MCBCPUCLKEN	C405PLBDCUPRIORITY [0:1]
MCBJTAGEN	C405PLBDCUREQUEST
MCBTIMEREN	C405PLBDCURNW
MCPPCRST	C405PLBDCUSIZE2
PLBC405DCUADDRACK	C405PLBDCUU0ATTR
PLBC405DCUBUSY	C405PLBDCUWRDBUS [0:63]
PLBC405DCUERR	C405PLBDCUWRITETHRU
PLBC405DCURDDACK	C405PLBICUABORT
PLBC405DCURDDBUS [0:63]	C405PLBICUABUS [0:29]
PLBC405DCURDWDADDR [1:3]	C405PLBICUCACHEABLE
PLBC405DCUSSIZE1	C405PLBICUPRIORITY [0:1]
PLBC405DCUWRDACK	C405PLBICUREQUEST
PLBC405ICUADDRACK	C405PLBICUSIZE [2:3]
PLBC405ICUBUSY	C405PLBICUU0ATTR
PLBC405ICUERR	C405RSTCHIPRESETREQ
PLBC405ICURDDACK	C405RSTCORERESETREQ
PLBC405ICURDDBUS [0:63]	C405RSTSYSRESETREQ
PLBC405ICURDWDADDR [1:3]	C405TRCCYCLE
PLBC405ICUSSIZE1	C405TRCEVENEXECUTIONSTATUS [0:1]
PLBCLK	C405TRCODDEXECUTIONSTATUS [0:1]
RSTC405RESETCHIP	C405TRCTRACESTATUS [0:3]
RSTC405RESETCORE	C405TRCTRIGGEREVENTOUT

Inputs	Outputs
RSTC405RESETSYS	C405TRCTRIGGEREVENTTYPE [0:10]
TIEC405DETERMINISTICMULT	C405XXXMACHINECHECK
TIEC405DISOPERANDFWD	DSOCMBRAMABUS [8:29]
TIEC405MMUEN	DSOCMBRAMBYTEWRITE [0:3]
TIEDSOCMDCRADDR [0:7]	DSOCMBRAMEN
TIEISOCMDCRADDR [0:7]	DSOCMBRAMWRDBUS [0:31]
TRCC405TRACEDISABLE	DSOCMBUSY
TRCC405TRIGGEREVENTIN	ISOCMBRAMEN
	ISOCMBRAMEVENWRITEEN
	ISOCMBRAMODDWRITEEN
	ISOCMBRAMRDABUS [8:28]
	ISOCMBRAMWRABUS [8:28]
	ISOCMBRAMWRDBUS [0:31]

PULLDOWN

Resistor to GND for Input Pads

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



PULLDOWN resistor elements are connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

PULLUP

Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A

X3861

The pull-up elements establish a High logic level for open-drain elements and macros (DECODE, WAND, WORAND) or 3-state nodes (TBUF) when all the drivers are off.

The buffer outputs are connected together as a wired-AND to form the output (O). When all the inputs are High, the output is off. To establish an output High level, a PULLUP resistor(s) is tied to output (O). One PULLUP resistor uses the least power, two pull-up resistors achieve the fastest Low-to-High speed.

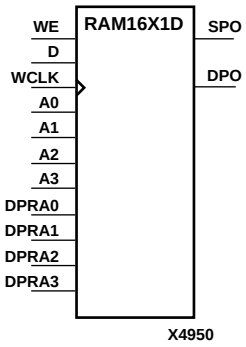
To indicate two PULLUP resistors, append a DOUBLE parameter to the pull-up symbol attached to the output (O) node. See the appropriate CAE tool interface user guide for details.

The PULLUP element is ignored in XC9500/XV/XL designs. Internal 3-state nodes (from BUFE or BUFT) in XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II are always pulled up when not driven.

RAM16X1D

16-Deep by 1-Wide Static Dual Port Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



RAM16X1D is a 16-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A3-A0

data_d = word addressed by bits DPRA3-DPRA0

The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note The write process is not affected by the address on the read address port.

Specifying Initial Contents of a RAM

You can use the INIT attribute to specify an initial value dirctly on the symbol if the RAM is 1 bit wide and 16, 32, 64, or 128 bits deep. The value must be a hexadecimal number, for example, INIT=ABAC. If the INIT attribute is not specified, the RAM is initialized with zero.

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, lower INIT values get mapped to the G function generator and upper INIT values get mapped to the F function generator.

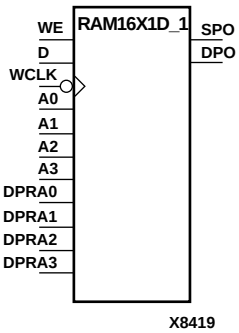
Refer to the "INIT" section of the *Constraints Guide* for more information on the INIT attribute.

For Virtex-II and Virtex-II PRO, wide RAMs (2, 4, and 8-bit wide single port synchronous RAMs with a WCLK) can also be initialized. These RAMs, however, require INIT_xx attributes. See "Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM" in the RAM16X2S section for more information on initializing Virtex-II wide RAM.

RAM16X1D_1

16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



RAM16X1D_1 is a 16-word by 1-bit static dual port random access memory with synchronous write capability and negative-edge clock. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM16X1D_1 during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↓	D	D	data_d
1 (read)	↑	X	data_a	data_d

data_a = word addressed by bits A3-A0

data_d = word addressed by bits DPRA3-DPRA0

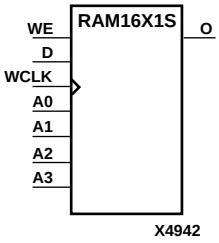
The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note The write process is not affected by the address on the read address port.

RAM16X1S

16-Deep by 1-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



RAM16X1S is a 16-word by 1-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM16X1S during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

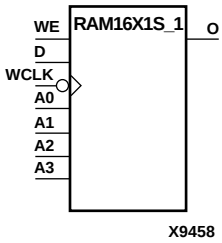
Inputs			Outputs
WE(mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

RAM16X1S_1

16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N / A	N / A	N / A



RAM16X1S_1 is a 16-word by 1-bit static random access memory with synchronous write capability and negative-edge clock. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM16X1S_1 during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

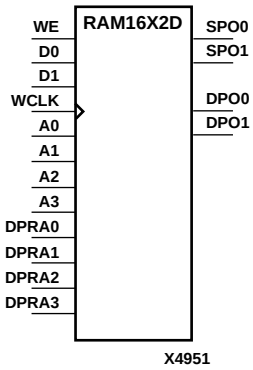
Inputs			Outputs
WE(mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data

Data = word addressed by bits A3 – A0

RAM16X2D

16-Deep by 2-Wide Static Dual Port Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



RAM16X2D is a 16-word by 2-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO1 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The initial contents of RAM16X2D cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D1-D0	SPO1-SPO0	DPO1-DPO0
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D1-D0	D1-D0	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A3-A0

data_d = word addressed by bits DPRA3-DPRA0

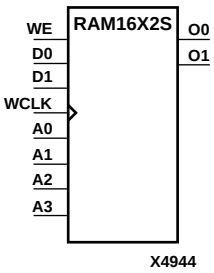
The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note The write process is not affected by the address on the read address port.

RAM16X2S

16-Deep by 2-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Primitive	N/A	N/A	N/A



RAM16X2S is a 16-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Except for Virtex-II and Virtex-II PRO, the initial contents of RAM16X2S cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

For Virtex-II and Virtex-II PRO, you can use the INIT_00 and INIT_01 properties to specify the initial contents of RAM16X2S as described in "Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM" in this section.

Mode selection is shown in the following truth table.

Inputs			Outputs
WE (mode)	WCLK	D1-D0	O1-O0
0 (read)	X	X	Data
1(read)	0	X	Data
1(read)	1	X	Data
1(write)	↑	D1-D0	D1-D0
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

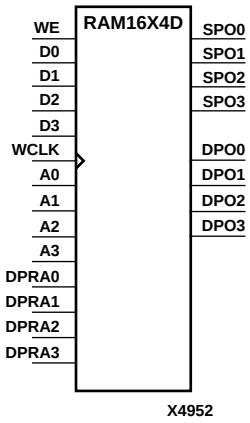
Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM

You can use the INIT_xx properties to specify the initial contents of a Virtex-II and Virtex-II PRO wide RAM. INIT_00 initializes the RAM cells corresponding to the O0 output, INIT_01 initializes the cells corresponding to the O1 output, etc. For example, a RAM16X2S instance is initialized by INIT_00 and INIT_01 containing 4 hex characters each. A RAM16X8S instance is initialized by eight properties INIT_00 through INIT_07 containing 4 hex characters each. A RAM64x2S instance is completely initialized by two properties INIT_00 and INIT_01 containing 16 hex characters each. See the "INIT_xx" section of the *Constraints Guide* for more information on the INIT_xx attribute.

RAM16X4D

16-Deep by 4-Wide Static Dual Port Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N/A	N/A	N/A



RAM16X4D is a 16-word by 4-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO3 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3 – D0) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The initial contents of RAM16X4D cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D3-D0	SPO3-SPO0	DPO3-DPO0
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D3-D0	D3-D0	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A3-A0

data_d = word addressed by bits DPRA3-DPRA0

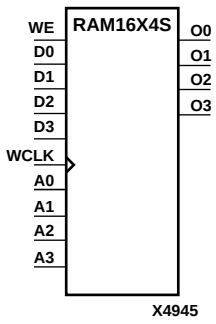
The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note The write process is not affected by the address on the read address port.

RAM16X4S

16-Deep by 4-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Primitive	N/A	N/A	N/A



RAM16X4S is a 16-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O3 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Except for Virtex-II and Virtex-II PRO, the initial contents of RAM16X4S cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

For Virtex-II and Virtex-II PRO, you can use INIT_00 through INIT_03 to specify the initial contents of RAM16X4S as described in the "Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM"section in the RAM16X2S section.

Mode selection is shown in the following truth table.

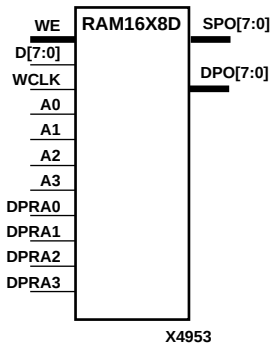
Inputs			Outputs
WE (mode)	WCLK	D3 – D0	O3 – O0
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3-D0	D3-D0
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

RAM16X8D

16-Deep by 8-Wide Static Dual Port Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	N / A	N / A	N / A



RAM16X8D is a 16-word by 8-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO7 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D7 – D0) into the word selected by the 4-bit write address (A3 – A0). For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The initial contents of RAM16X8D cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D7-D0	SP7-SPO0	DPO7-DPO0
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D7-D0	D7-D0	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A3-A0

data_d = word addressed by bits DPRA3-DPRA0

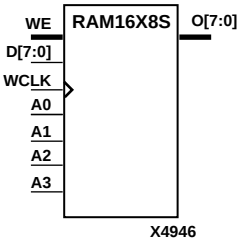
The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note The write process is not affected by the address on the read address port.

RAM16X8S

16-Deep by 8-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Primitive	N/A	N/A	N/A



RAM16X8S is a 16-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on data inputs (D7 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O7 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Except for Virtex-II and Virtex-II PRO, the initial contents of RAM16X8S cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

For Virtex-II and Virtex-II PRO, you can use INIT_00 through INIT_07 to specify the initial contents of RAM16X4S as described in the "Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM" section in the RAM16X2S section.

Mode selection is shown in the following truth table.

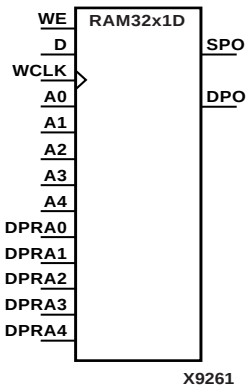
Inputs			Outputs
WE (mode)	WCLK	D7-D0	O7-O0
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7-D0	D7-D0
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

RAM32X1D

32-Deep by 1-Wide Static Dual Static Port Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



RAM32X1D is a 32-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA4 – DPRA0) and the write address (A4 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM32X1D during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A4-A0

data_d = word addressed by bits DPRA4-DPRA0

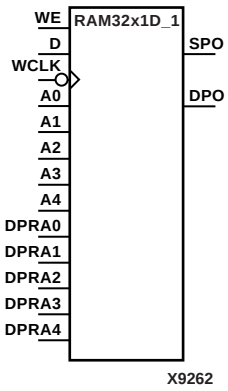
The SPO output reflects the data in the memory cell addressed by A4 – A0. The DPO output reflects the data in the memory cell addressed by DPRA4 – DPRA0.

Note The write process is not affected by the address on the read address port.

RAM32X1D_1

32-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



RAM32X1D_1 is a 32-word by 1-bit static dual port random access memory with synchronous write capability and a negative-edge clock. The device has two separate address ports: the read address (DPRA4 – DPRA0) and the write address (A4 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-Low WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM32X1D_1 during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↓	D	D	data_d
1 (read)	↑	X	data_a	data_d

data_a = word addressed by bits A4-A0

data_d = word addressed by bits DPRA4-DPRA0

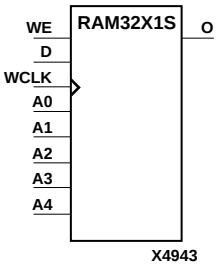
The SPO output reflects the data in the memory cell addressed by A4 – A0. The DPO output reflects the data in the memory cell addressed by DPRA4 – DPRA0.

Note The write process is not affected by the address on the read address port.

RAM32X1S

32-Deep by 1-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



RAM32X1S is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM32X1S during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

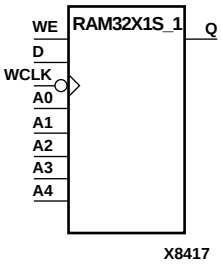
Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

RAM32X1S_1

32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



RAM32X1S_1 is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM32X1S_1 during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

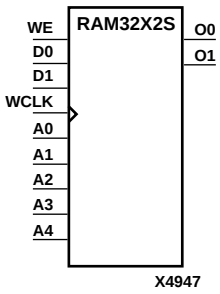
Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data

Data = word addressed by bits A4 – A0

RAM32X2S

32-Deep by 2-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Primitive	N/A	N/A	N/A



RAM32X2S is a 32-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Except for Virtex-II and Virtex-II PRO, the initial contents of RAM32X2S cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

For Virtex-II and Virtex-II PRO, you can use the INIT_00 and INIT_01 properties to specify the initial contents of RAM32X2S as described in "Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM" in the RAM16X2S section.

Mode selection is shown in the following truth table.

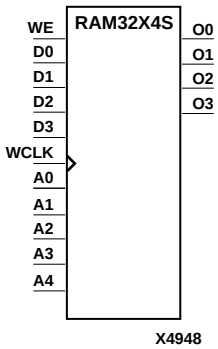
Inputs			Outputs
WE (mode)	WCLK	D0-D1	O0-O1
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1-D0	D1-D0
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

RAM32X4S

32-Deep by 4-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Primitive	N/A	N/A	N/A



RAM32X4S is a 32-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D3 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O3 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Except for Virtex-II and Virtex-II PRO, the initial contents of RAM32X4S cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

For Virtex-II and Virtex-II PRO, you can use the INIT_00 through INIT_03 properties to specify the initial contents of RAM32X4S as described in "Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM" in the RAM16X2S section.

Mode selection is shown in the following truth table.

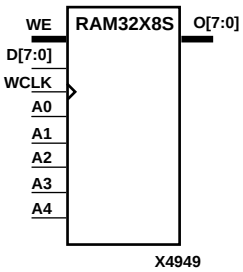
Inputs			Outputs
WE	WCLK	D3-D0	O3-O0
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3-D0	D3-D0
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

RAM32X8S

32-Deep by 8-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Primitive	N/A	N/A	N/A



RAM32X8S is a 32-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D7 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O7 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Except for Virtex-II and Virtex-II PRO, the initial contents of RAM32X8S cannot be specified directly. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

For Virtex-II and Virtex-II PRO, you can use the INIT_00 through INIT_07 properties to specify the initial contents of RAM32X8S as described in "Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM" in the RAM16X2S section.

Mode selection is shown in the following truth table.

Inputs			Outputs
WE (mode)	WCLK	D7-D0	O7-O0
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7-D0	D7-D0
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

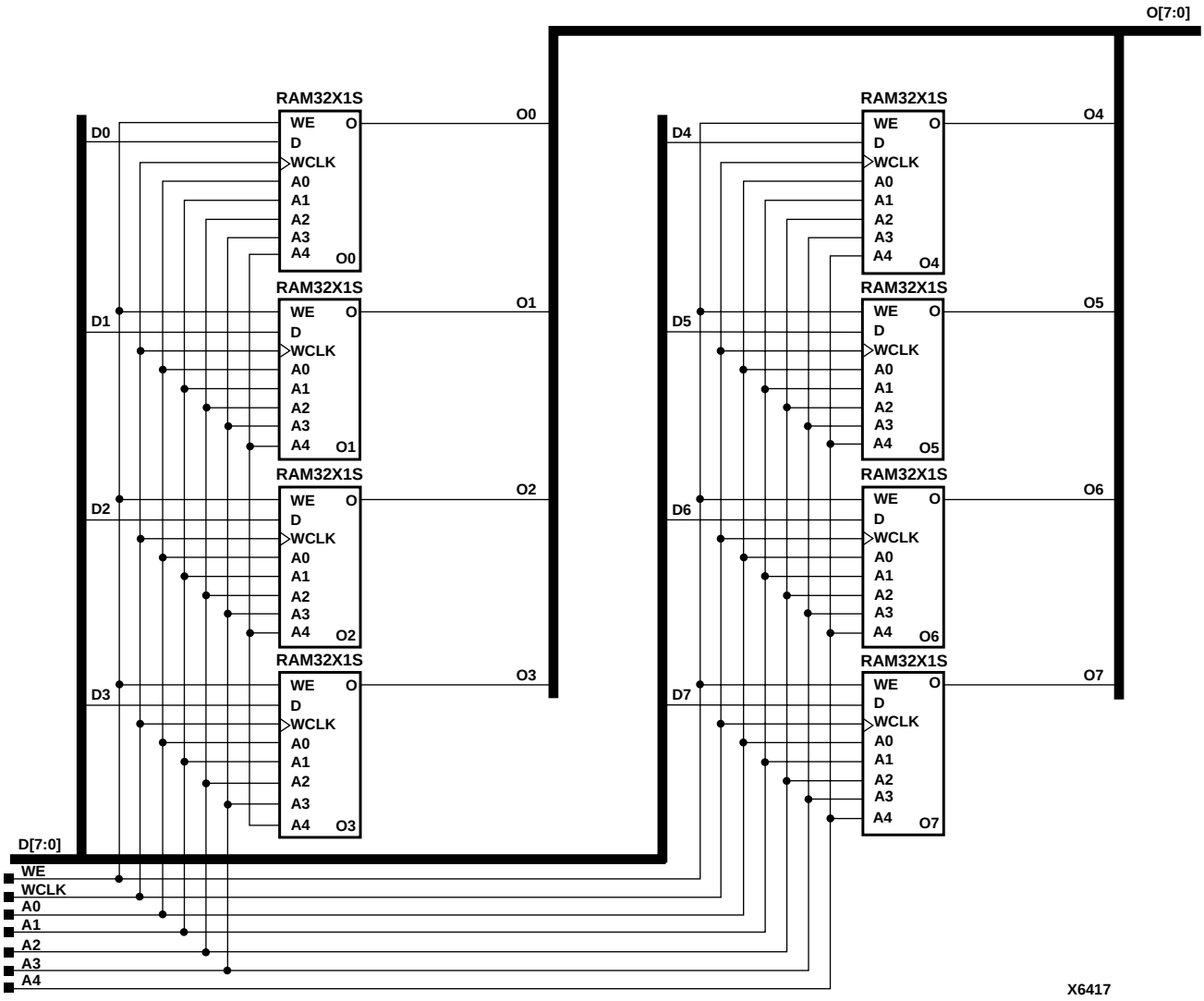
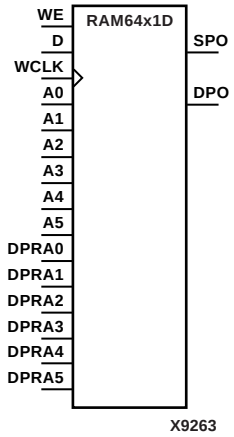


Figure 9-1 RAM32X8S Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

RAM64X1D

64-Deep by 1-Wide Dual Port Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



RAM64X1D is a 64-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA5 – DPRA0) and the write address (A5 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit (A0 - A5) write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM64X1D during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A5-A0

data_d = word addressed by bits DPRA5-DPRA0

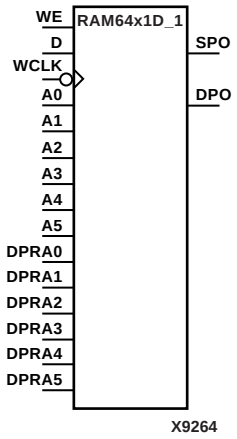
The SPO output reflects the data in the memory cell addressed by A5 – A0. The DPO output reflects the data in the memory cell addressed by DPRA5 – DPRA0.

Note The write process is not affected by the address on the read address port.

RAM64X1D_1

64-Deep by 1-Wide Dual Port Static Synchronous RAM with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



RAM64X1D_1 is a 64-word by 1-bit static dual port random access memory with synchronous write capability and a negative-edge clock. The device has two separate address ports: the read address (DPRA5 – DPRA0) and the write address (A5 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit (A0 - A5) write address. For predictable performance, write address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-Low WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM64X1D_1 during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↓	D	D	data_d
1 (read)	↑	X	data_a	data_d

data_a = word addressed by bits A5-A0

data_d = word addressed by bits DPRA5-DPRA0

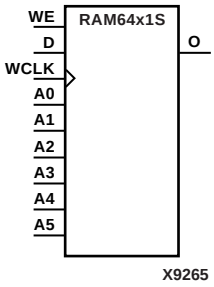
The SPO output reflects the data in the memory cell addressed by A5 – A0. The DPO output reflects the data in the memory cell addressed by DPRA5 – DPRA0.

Note The write process is not affected by the address on the read address port.

RAM64X1S

64-Deep by 1-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



RAM64X1S is a 64-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit address (A5 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM64X1S during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

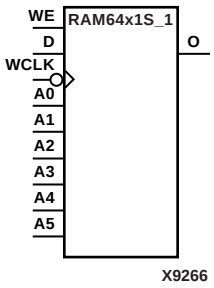
Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Data = word addressed by bits A5 – A0

RAM64X1S_1

64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	Primitive	N / A	N / A	N / A



RAM64X1S_1 is a 64-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit address (A5 – A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM32X1S_1 during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

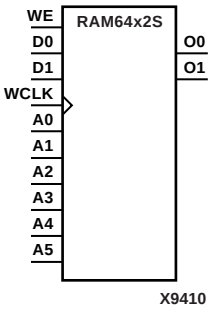
Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data

Data = word addressed by bits A5 – A0

RAM64X2S

64-Deep by 2-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



RAM64X2S is a 64-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 6-bit address (A5 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT_00 and INIT_01 properties to specify the initial contents of RAM64X2S as described in "Specifying Initial Contents of a Virtex-II and Virtex-II PRO Wide RAM" in the RAM16X2S section.

Mode selection is shown in the following truth table.

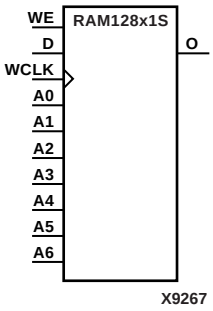
Inputs			Outputs
WE (mode)	WCLK	D0-D1	O0-O1
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1-D0	D1-D0
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

RAM128X1S

128-Deep by 1-Wide Static Synchronous RAM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



RAM128X1S is a 128-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 7-bit address (A6 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM128X1S during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

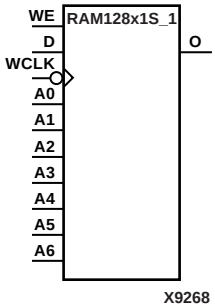
Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Data = word addressed by bits A6 – A0

RAM128X1S_1

128-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



RAM128X1S_1 is a 64-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 7-bit address (A6 – A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM128X1S_1 during configuration using the INIT attribute. See "Specifying Initial Contents of a RAM" in the RAM16X1D section.

Mode selection is shown in the following truth table.

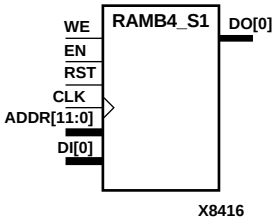
Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data

Data = word addressed by bits A6 – A0

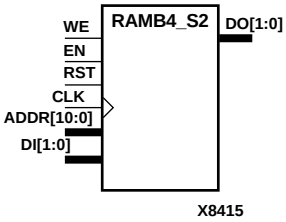
RAMB4_S*n*

4096-Bit Single-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 8, or 16 Bits

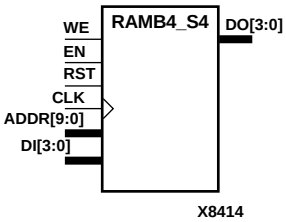
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	N/A	N/A	N/A	N/A



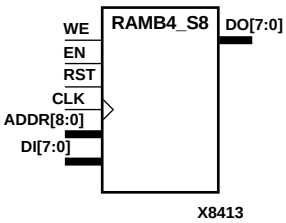
X8416



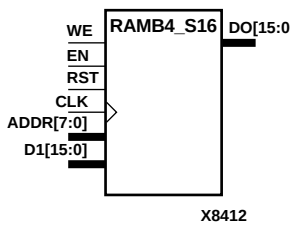
X8415



X8414



X8413



X8412

RAMB4_S1, RAMB4_S2, RAMB4_S4, RAMB4_S8, and RAMB4_S16 are dedicated random access memory blocks with synchronous write capability. They provide the capability for fast, discrete, large blocks of RAM in each Virtex, Virtex-E, Spartan-II, and Spartan-IIE device.The RAMB4_Sn cell configurations are listed in the following table.

Component	Depth	Width	Address Bus	Data Bus
RAMB4_S1	4096	1	(11:0)	(0:0)
RAMB4_S2	2048	2	(10:0)	(1:0)
RAMB4_S4	1024	4	(9:0)	(3:0)
RAMB4_S8	512	8	(8:0)	(7:0)
RAMB4_S16	256	16	(7:0)	(15:0)

The enable (EN) pin controls read, write, and reset. When EN is Low, no data is written and the output (DO) retains the last state. When EN is High and reset (RST) is High, DO is cleared during the Low-to-High clock (CLK) transition; if write enable (WE) is High, the memory contents reflect the data at DI. When EN is High and WE is Low, the data stored in the RAM address (ADDR) is read during the Low-to-High clock transition. When EN and WE are High, the data on the data input (DI) is loaded into the word selected by the write address (ADDR) during the Low-to-High clock transition and the data output (DO) reflects the selected (addressed) word.

The above description assumes an active High EN, WE, RST, and CLK. However, the active level can be changed by placing an inverter on the port. Any inverter placed on a RAMB4 port is absorbed into the block and does not use a CLB resource.

RAMB4_Sn's may be initialized during configuration. See "Specifying Initial Contents of a Block RAM" below.

Block RAM output registers are asynchronously cleared, output Low, when power is applied. The initial contents of the block RAM are not altered.

Virtex, Virtex-E, Spartan-II, and Spartan-IIE simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Mode selection is shown in the following truth table.

Inputs						Outputs	
EN	RST	WE	CLK	ADDR	DI	DO	RAM Contents
0	X	X	X	X	X	No Chg	No Chg
1	1	0	↑	X	X	0	No Chg
1	1	1	↑	addr	data	0	RAM(addr) <=data
1	0	0	↑	addr	X	RAM(addr)	No Chg
1	0	1	↑	addr	data	data	RAM(addr) <=data

addr=RAM address

RAM(addr)=RAM contents at address ADDR

data=RAM input data

Specifying Initial Contents of a Block RAM

You can use the INIT_xx attributes to specify an initial value during device configuration. The initialization of each RAMB4_Sn is set by 16 initialization attributes (INIT_00 through INIT_0F) of 64 hex values for a total of 4096 bits. See the "INIT_xx" section of the *Constraints Guide* for more information on these attributes.

If any INIT_0x attribute is not specified, it is configured as zeros. Partial initialization strings are padded with zeros to the left.

RAMB4_S*m*_S*n*

4096-Bit Dual-Port Synchronous Block RAM with Port Width (m or n) Configured to 1, 2, 4, 8, or 16 Bits

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	N / A	N / A	N / A	N / A

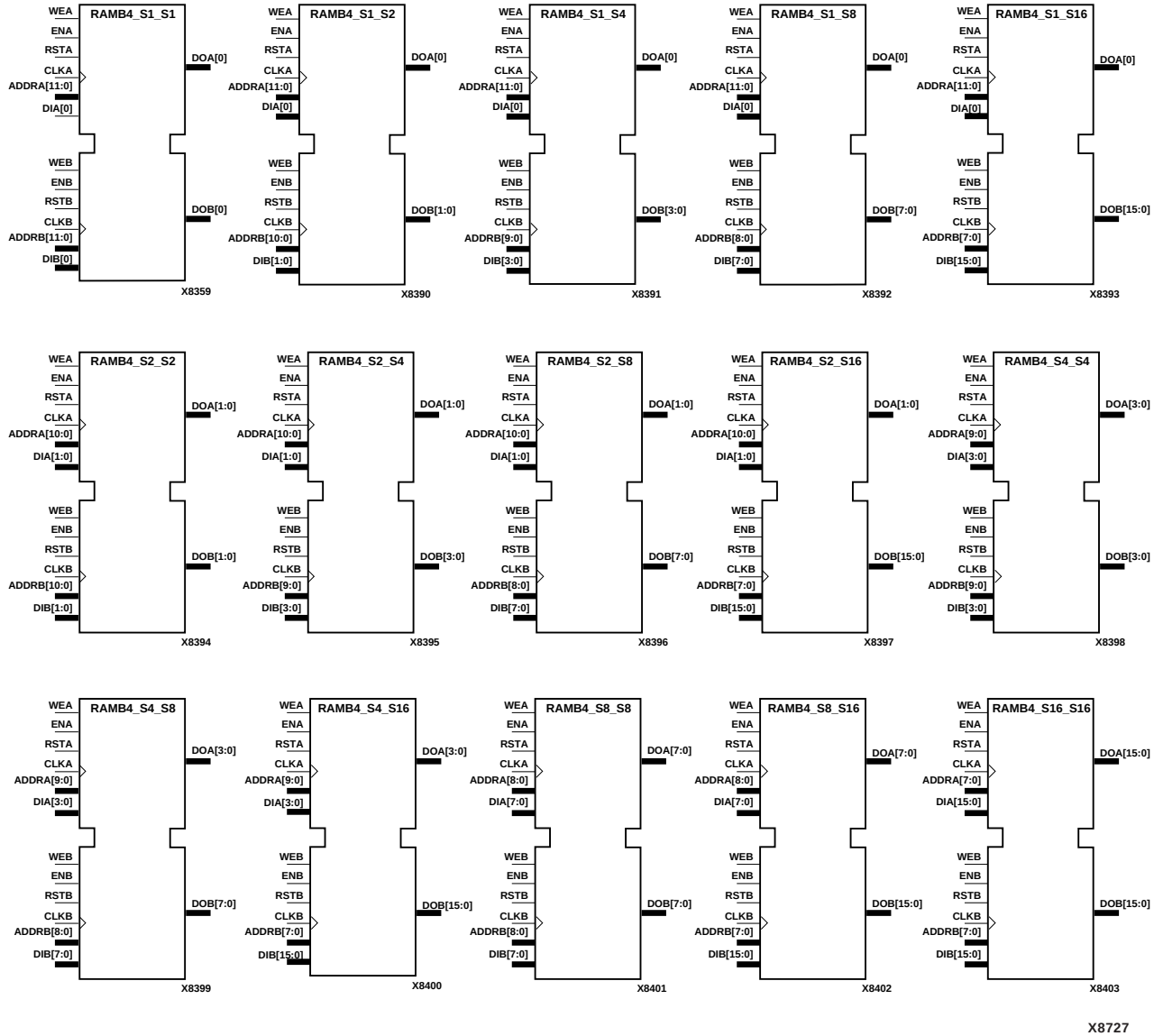


Figure 9-2 RAMB4_Sm_Sn Representations

The RAMB4_S*m*_S*n* components listed in the following table are 4096-bit dual-ported dedicated random access memory blocks with synchronous write capability. Each port is independent of the other while accessing the same set of 4096 memory cells. Each port is independently configured to a specific data width.

Component	Port A Depth	Port A Width	Port A ADDR	Port A DI	Port B Depth	Port B Width	Port B ADDR	Port B DI
RAMB4_S1_S1	4096	1	(11:0)	(0:0)	4096	1	(11:0)	(0:0)
RAMB4_S1_S2	4096	1	(11:0)	(0:0)	2048	2	(10:0)	(1:0)
RAMB4_S1_S4	4096	1	(11:0)	(0:0)	1024	4	(9:0)	(3:0)
RAMB4_S1_S8	4096	1	(11:0)	(0:0)	512	8	(8:0)	(7:0)
RAMB4_S1_S16	4096	1	(11:0)	(0:0)	256	16	(7:0)	(15:0)
RAMB4_S2_S2	2048	2	(10:0)	(1:0)	2048	2	(10:0)	(1:0)
RAMB4_S2_S4	2048	2	(10:0)	(1:0)	1024	4	(9:0)	(3:0)
RAMB4_S2_S8	2048	2	(10:0)	(1:0)	512	8	(8:0)	(7:0)
RAMB4_S2_S16	2048	2	(10:0)	(1:0)	256	16	(7:0)	(15:0)
RAMB4_S4_S4	1024	4	(9:0)	(3:0)	1024	4	(9:0)	(3:0)
RAMB4_S4_S8	1024	4	(9:0)	(3:0)	512	8	(8:0)	(7:0)
RAMB4_S4_S16	1024	4	(9:0)	(3:0)	256	16	(7:0)	(15:0)
RAMB4_S8_S8	512	8	(8:0)	(7:0)	512	8	(8:0)	(7:0)
RAMB4_S8_S16	512	8	(8:0)	(7:0)	256	16	(7:0)	(15:0)
RAMB4_S16_S16	256	16	(7:0)	(15:0)	256	16	(7:0)	(15:0)

ADDR=address bus for the port

DI=data input bus for the port

Each port is fully synchronous with independent clock pins. All port A input pins have setup time referenced to the CLKA pin and its data output bus DIA has a clock-to-out time referenced to the CLKA. All port B input pins have setup time referenced to the CLKB pin and its data output bus DIB has a clock-to-out time referenced to the CLKB.

The enable ENA pin controls read, write, and reset for port A. When ENA is Low, no data is written and the output (DOA) retains the last state. When ENA is High and reset (RSTA) is High, DOA is cleared during the Low-to-High clock (CLKA) transition; if write enable (WEA) is High, the memory contents reflect the data at DIA. When ENA is High and WEA is Low, the data stored in the RAM address (ADDRA) is read during the Low-to-High clock transition. When ENA and WEA are High, the data on the data input (DIA) is loaded into the word selected by the write address (ADDRA) during the Low-to-High clock transition and the data output (DOA) reflects the selected (addressed) word.

The enable ENB pin controls read, write, and reset for port B. When ENB is Low, no data is written and the output (DOB) retains the last state. When ENB is High and reset (RSTB) is High, DOB is cleared during the Low-to-High clock (CLKB) transition; if write enable (WEB) is High, the memory contents reflect the data at DIB. When ENB is High and WEB is Low, the data stored in the RAM address (ADDRB) is read during the Low-to-High clock transition. When ENB and WEB are High, the data on the data input (DIB) is loaded into the word selected by the write address (ADDRB) during the Low-to-High clock transition and the data output (DOB) reflects the selected (addressed) word.

The above descriptions assume active High control pins (ENA, WEA, RSTA, CLKA, ENB, WEB, RSTB, and CLKB). However, the active level can be changed by placing an inverter on the port. Any inverter placed on a RAMB4 port is absorbed into the block and does not use a CLB resource.

RAMB_S*m*_S*n*'s may be initialized during configuration. See "Specifying Initial Contents of a Block RAM" below.

Block RAM output registers are asynchronously cleared, output Low, when power is applied. The initial contents of the block RAM are not altered.

Virtex, Virtex-E, Spartan-II, and Spartan-IIE simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Mode selection is shown in the following truth table.

Inputs						Outputs	
EN(A/B)	RST(A/B)	WE(A/B)	CLK(A/B)	ADDR(A/B)	DI(A/B)	DO(A/B)	RAM Contents
0	X	X	X	X	X	No Chg	No Chg
1	1	0	↑	X	X	0	No Chg
1	1	1	↑	addr	data	0	RAM(addr) <=data
1	0	0	↑	addr	X	RAM(addr)	No Chg
1	0	1	↑	addr	data	data	RAM(addr) <=data

addr=RAM address of port A/B

RAM(addr)=RAM contents at address ADDRA/ADDRB

data=RAM input data at pins DIA/DIB

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme that is dependent on the width of the port. The physical RAM location that is addressed for a particular width is determined from the following formula.

```
Start=((ADDR port+1)*(Widthport)) -1
End=(ADDRport)*(Widthport)
```

The following table shows address mapping for each port width.

Table 9-1 Port Address Mapping

Port Width	Port Addresses																	
1	4096	<-----	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2048	<-----	07		06		05		04		03		02		01		00	
4	1024	<-----	03				02				01				00			
8	512	<-----	01								00							
16	256	<-----	00															

Port A and Port B Conflict Resolution

A RAMB4_S*m*_S*n* component is a true dual-ported RAM in that it allows simultaneous reads of the same memory cell. When one port is performing a write to a given memory cell, the other port should not address that memory cell (for a write or a read) within the clock-to-clock setup window.

If both ports write to the same memory cell simultaneously, violating the clock-to-setup requirement, the data stored will be invalid.

If one port attempts to read from the same memory cell that the other is simultaneously writing to, violating the clock setup requirement, the write will be successful but the data read will be invalid.

Specifying Initial Contents of a Block RAM

You can use the INIT_0x attributes to specify an initial value during device configuration. The initialization of each RAMB4_S*m*_S*n* is set by 16 initialization attributes (INIT_00 through INIT_0F) of 64 hex values for a total of 4096 bits. See the "INIT_xx" section of the *Constraints Guide* for more information on these attributes.

If any INIT_0x attribute is not specified, it is configured as zeros. Partial initialization strings are padded with zeros to the left.

RAMB16_S*n*

16384-Bit Data Memory and 2048-Bit Parity Memory, Single-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 9, 18, or 36 Bits

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

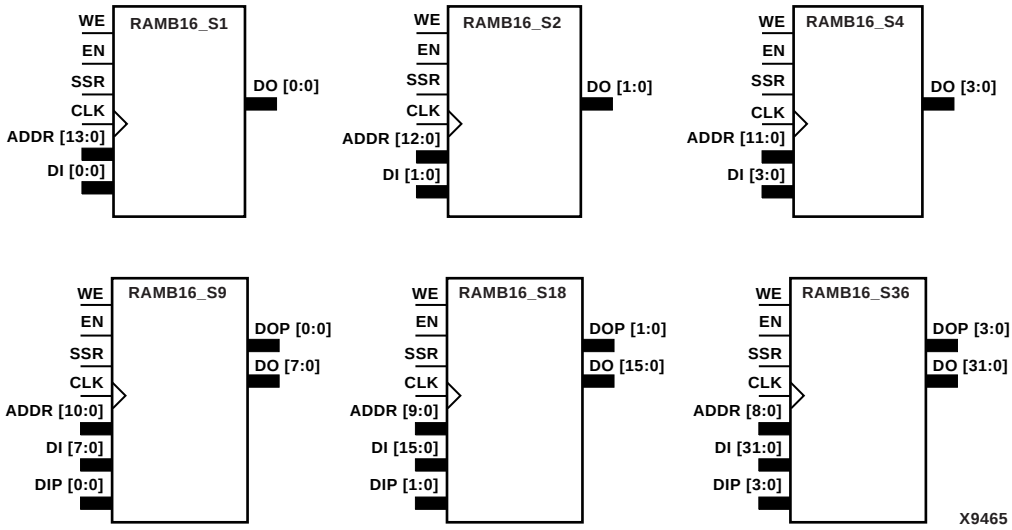


Figure 9-3 RAMB16_S1 through RAMB16_S36 Representations

RAMB16_S1, RAMB16_S2, RAMB16_S4, RAMB16_S9, RAMB16_S18, and RAMB16_S36 are dedicated random access memory blocks with synchronous write capability. The block RAM port has 16384 bits of data memory. RAMB16_S9, RAMB16_S18, and RAMB16_S36 have an additional 2048 bits of parity memory. The RAMB16_Sn cell configurations are listed in the following table.

Component	Data Cells		Parity Cells		Address Bus	Data Bus	Parity Bus
	Depth	Width	Depth	Width			
RAMB16_S1	16384	1	-	-	(13:0)	(0:0)	-
RAMB16_S2	8192	2	-	-	(12:0)	(1:0)	-
RAMB16_S4	4096	4	-	-	(11:0)	(3:0)	-
RAMB16_S9	2048	8	2048	1	(10:0)	(7:0)	(0:0)
RAMB16_S18	1024	16	1024	2	(9:0)	(15:0)	(1:0)
RAMB16_S36	512	32	512	4	(8:0)	(31:0)	(3:0)

The enable (EN) pin controls read, write, and reset. When EN is Low, no data is written and the outputs (DO and DOP) retain the last state. When EN is High and reset (SSR) is High, DO and DOP are set to SRVAL during the Low-to-High clock (CLK) transition; if write enable (WE) is High, the memory contents reflect the data at DI and DIP. When SSR is Low, EN is High, and WE is Low, the data stored in the RAM address (ADDR) is read during the Low-to-High clock transition. By default WRITE_MODE=WRITE_FIRST, whenever EN and WE are High, the data on the data inputs (DI and DIP) is loaded into the word selected by the write address (ADDR) during the Low-to-High clock transition and the data outputs (DO and DOP) reflect the selected (addressed) word. See the "Write Mode Selection" section for information on setting the WRITE_MODE.

The above description assumes an active High EN, WE, SSR, and CLK. However, the active level can be changed by placing an inverter on the port. Any inverter placed on a RAMB16 port is absorbed into the block and does not use a CLB resource.

Inputs								Outputs			
GSR	EN	SSR	WE	CLK	ADDR	DI	DIP	DO	DOP	RAM Contents	
										Data RAM	Parity RAM
1	X	X	X	X	X	X	X	INIT	INIT	No Chg	No Chg
0	0	X	X	X	X	X	X	No Chg	No Chg	No Chg	No Chg
0	1	1	0	↑	X	X	X	SRVAL	SRVAL	No Chg	No Chg
0	1	1	1	↑	addr	data	pdata	SRVAL	SRVAL	RAM(addr) <=data	RAM(addr) <=pdata
0	1	0	0	↑	addr	X	X	RAM(addr)	RAM(addr)	No Chg	No Chg
0	1	0	1	↑	addr	data	pdata	No Chg[a] RAM (addr)[b] data[c]	No Chg[a] RAM(addr)[b] pdata[c]	RAM(addr) <=data	RAM(addr) <=pdata

GSR=Global Set Reset signal

INIT=Value specified by the INIT attribute for data memory. Default is all zeros.
SRVAL=Value after assertion of SSR as specified by the SRVAL attribute.

addr=RAM address
RAM(addr)=RAM contents at address ADDR
data=RAM input data
pdata=RAM parity data

[a]WRITE_MODE=NO_CHANGE
[b]WRITE_MODE=READ_FIRST
[c]WRITE_MODE=WRITE_FIRST

Initializing Memory Contents of a Single-Port RAMB16

You can use the INIT_xx attributes to specify an initialization value for the memory contents of a RAMB16 during device configuration. The initialization of each RAMB16_Sn is set by 64 initialization attributes (INIT_00 through INIT_3F) of 64 hex values for a total of 16384 bits.

You can use the INITP_xx attributes to specify an initial value for the parity memory during device configuration or assertion. The initialization of the parity memory for ports configured for 9, 18, or 36 bits is set by 8 initialization attributes (INITP_00 through INITP_07) of 64 hex values for a total of 2048 bits.

If any INIT_xx or INITP_xx attribute is not specified, it is configured as zeros. Partial strings are padded with zeros to the left.

See the *Constraints Guide* for more information on these attributes.

Initializing the Output Register of a Single-Port RAMB16

In Virtex-II and Virtex-II PRO, each bit in the output register can be initialized at power on to either a 0 or 1. In addition, the initial state specified for power on can be different than the state that results from assertion of a set/reset. Two types of properties control initialization of the output register for a single-port RAMB16: INIT and SRVAL. The INIT attribute specifies the output register value at power on. You can use the SRVAL attribute to define the state resulting from assertion of the SSR (set/reset) input.

The INIT and SRVAL attributes specify the initialization value as a hexadecimal string. The value is dependent upon the port width. For example, for a RAMB16_S1 with port width equal to 1, the output register contains 1 bit. Therefore, the INIT or SRVAL value can only be specified as a 1 or 0. For RAMB16_S4 with port width equal to 4, the output register contains 4 bits. In this case, you can specify a hexadecimal value from 0 through F to initialize the 4 bits of the output register.

For those ports that include parity bits, the parity portion of the output register is specified in the high order bit position of the INIT or SRVAL value.

The INIT and SRVAL attributes default to zero if they are not set by the user.

See the *Constraints Guide* for more information on these attributes.

Write Mode Selection

The WRITE_MODE attribute controls RAMB16 memory and output contents. By default, the WRITE_MODE is set to WRITE_FIRST. This means that input is read, written to memory, and then passed to output. You can set the WRITE_MODE to READ_FIRST to read the memory contents, pass the memory contents to the outputs, and then write the input to memory. Or, you can set the WRITE_MODE to NO_CHANGE to have the input written to memory without changing the output.

RAMB16_S*m*_S*n*

16384-Bit Data Memory and 2048-Bit Parity Memory, Dual-Port Synchronous Block RAM with Port Width (m or n) Configured to 1, 2, 4, 9, 18, or 36 Bits

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A

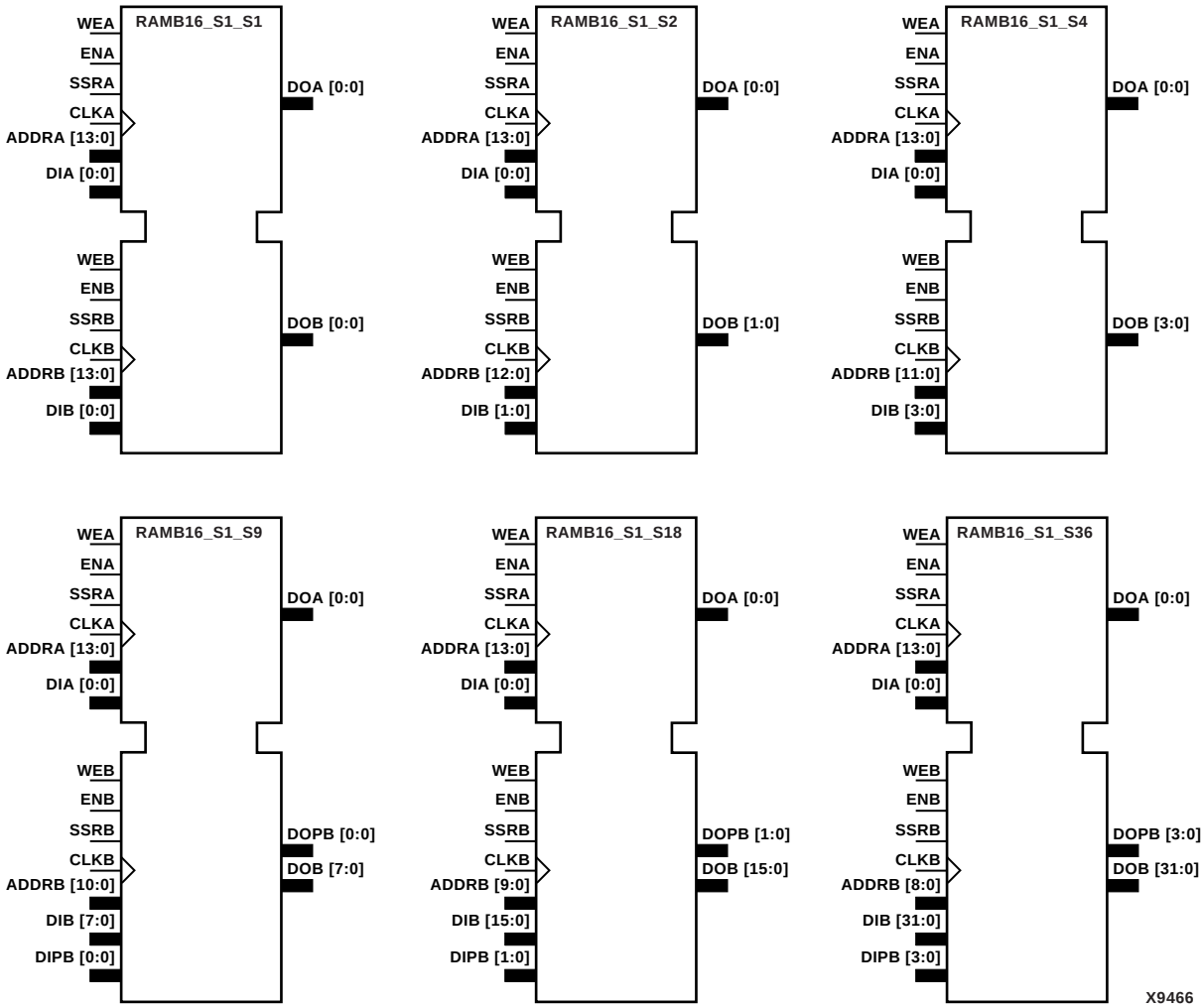


Figure 9-4 RAMB16_S1_S1 through RAMB16_S1_S36 Representations

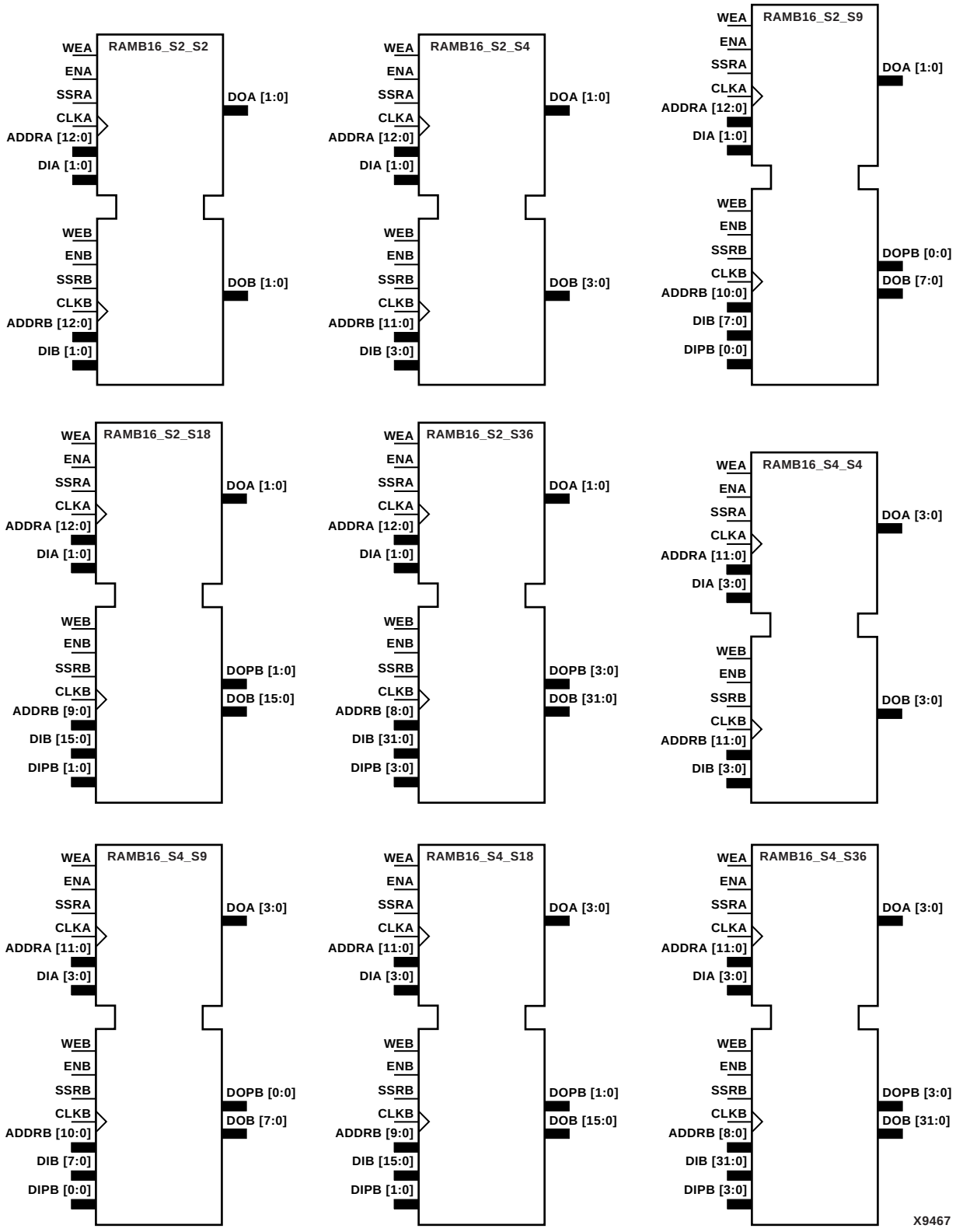


Figure 9-5 RAMB16_S2_S2 through RAMB16_S4_S36 Representations

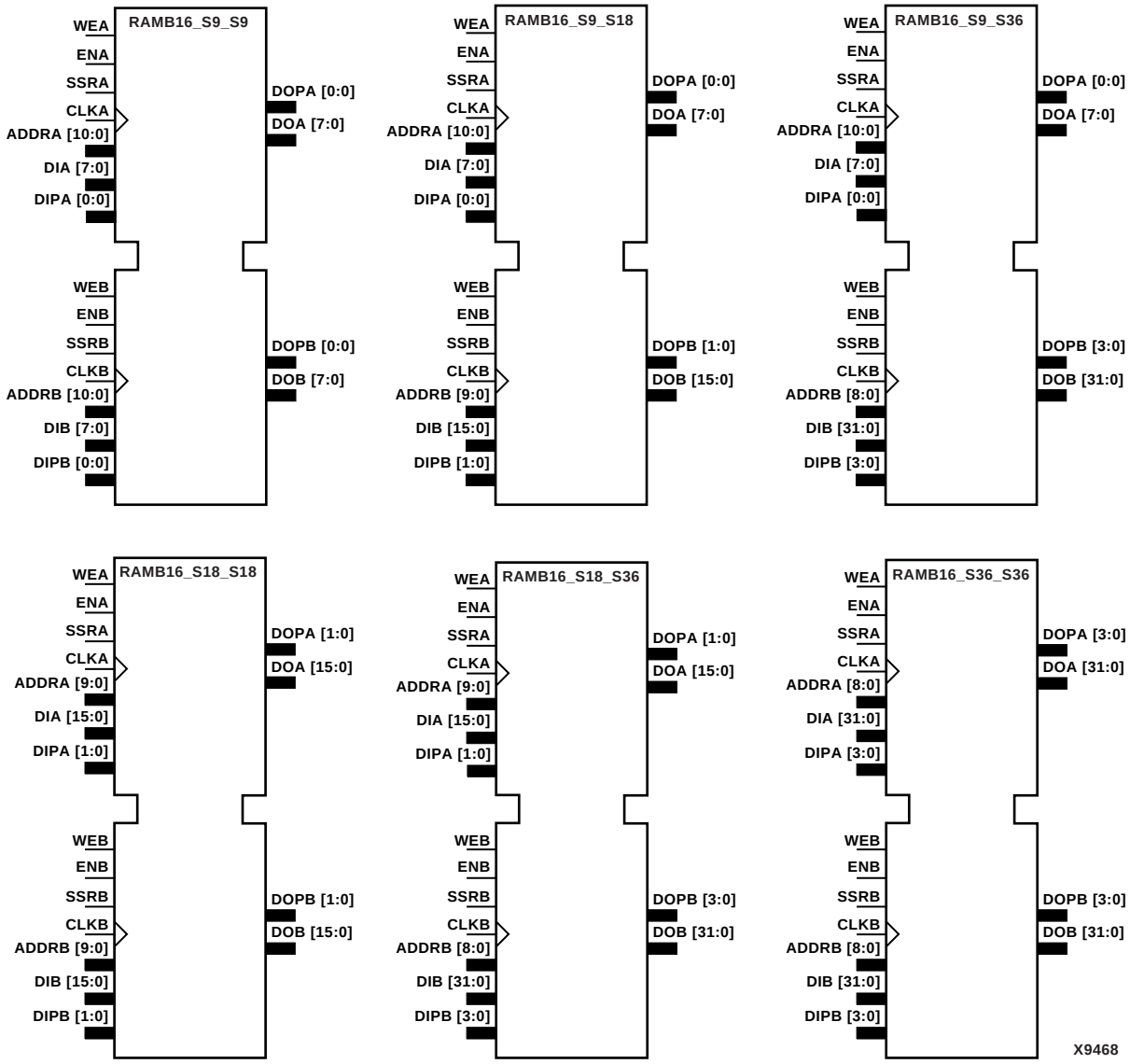


Figure 9-6 RAMB16_S9_S9 through RAMB16_S36_S36 Representations

The RAMB16_S*m*_S*n* components listed in the following table are dual-ported dedicated random access memory blocks with synchronous write capability. Each block RAM port has 16384 bits of data memory. Ports configured as 9, 18, or 36-bits wide have an additional 2048 bits of parity memory. Each port is independent of the other while accessing the same set of 16384 data memory cells. Each port is independently configured to a specific data width. The possible port and cell configurations are listed in the following table.

Component	Port A					Port B				
	Data Cells[a]	Parity Cells[a]	Address Bus	Data Bus	Parity Bus	Data Cells[a]	Parity Cells[a]	Address Bus	Data Bus	Parity Bus
RAMB16_S1_S1	16384 x 1	-	(13:0)	(0:0)	-	16384 x 1	-	(13:0)	(0:0)	-
RAMB16_S1_S2	16384 x 1	-	(13:0)	(0:0)	-	8192 x 2	-	(12:0)	(1:0)	-
RAMB16_S1_S4	16384 x 1	-	(13:0)	(0:0)	-	4096 x 4	-	(11:0)	(3:0)	-
RAMB16_S1_S9	16384 x 1	-	(13:0)	(0:0)	-	2048 x 8	2048 x 1	(10:0)	(7:0)	(0:0)
RAMB16_S1_S18	16384 x 1	-	(13:0)	(0:0)	-	1024 x 16	1024 x 2	(9:0)	(15:0)	(1:0)
RAMB16_S1_S36	16384 x 1	-	(13:0)	(0:0)	-	512 x 32	512 x 4	(8:0)	(31:0)	(3:0)
RAMB16_S2_S2	8192 x 2	-	(12:0)	(1:0)	-	8192 x 2	-	(12:0)	(1:0)	-
RAMB16_S2_S4	8192 x 2	-	(12:0)	(1:0)	-	4096 x 4	-	(11:0)	(3:0)	-
RAMB16_S2_S9	8192 x 2	-	(12:0)	(1:0)	-	2048 x 8	2048 x 1	(10:0)	(7:0)	(0:0)
RAMB16_S2_S18	8192 x 2	-	(12:0)	(1:0)	-	1024 x 16	1024 x 2	(9:0)	(15:0)	(1:0)
RAMB16_S2_S36	8192 x 2	-	(12:0)	(1:0)	-	512 x 32	512 x 4	(8:0)	(31:0)	(3:0)
RAMB16_S4_S4	4096 x 4	-	(11:0)	(3:0)	-	4096 x 4	-	(11:0)	(3:0)	-
RAMB16_S4_S9	4096 x 4	-	(11:0)	(3:0)	-	2048 x 8	2048 x 1	(10:0)	(7:0)	(0:0)
RAMB16_S4_S18	4096 x 4	-	(11:0)	(3:0)	-	1024 x 16	1024 x 2	(9:0)	(15:0)	(1:0)
RAMB16_S4_S36	4096 x 4	-	(11:0)	(3:0)	-	512 x 32	512 x 4	(8:0)	(31:0)	(3:0)
RAMB16_S9_S9	2048 x 8	2048 x 1	(10:0)	(7:0)	(0:0)	2048 x 8	2048 x 1	(10:0)	(7:0)	(0:0)
RAMB16_S9_S18	2048 x 8	2048 x 1	(10:0)	(7:0)	(0:0)	1024 x 16	1024 x 2	(9:0)	(15:0)	(1:0)
RAMB16_S9_S36	2048 x 8	2048 x 1	(10:0)	(7:0)	(0:0)	512 x 32	512 x 4	(8:0)	(31:0)	(3:0)
RAMB16_S18_S18	1024 x 16	1024 x 2	(9:0)	(15:0)	(1:0)	1024 x 16	1024 x 2	(9:0)	(15:0)	(1:0)
RAMB16_S18_S36	1024 x 16	1024 x 2	(9:0)	(15:0)	(1:0)	512 x 32	512 x 4	(8:0)	(31:0)	(3:0)
RAMB16_S36_S36	512 x 32	512 x 4	(8:0)	(31:0)	(3:0)	512 x 32	512 x 4	(8:0)	(31:0)	(3:0)

[a] Depth x Width

Each port is fully synchronous with independent clock pins. All port A input pins have setup time referenced to the CLKA pin and its data output bus DIA has a clock-to-out time referenced to the CLKA. All port B input pins have setup time referenced to the CLKB pin and its data output bus DIB has a clock-to-out time referenced to the CLKB.

The enable ENA pin controls read, write, and reset for port A. When ENA is Low, no data is written and the outputs (DOA and DOPA) retain the last state. When ENA is High and reset (SSRA) is High, DOA and DOPA are set to SRVAL_A during the Low-to-High clock (CLKA) transition; if write enable (WEA) is High, the memory contents reflect the data at DIA and DIPA. When ENA is High and WEA is Low, the data stored in the RAM address (ADDRA) is read during the Low-to-High clock transition. By default, WRITE_MODE_A=WRITE_FIRST, when ENA and WEA are High, the data on the data inputs (DIA and DIPA) is loaded into the word selected by the write address (ADDRA) during the Low-to-High clock transition and the data outputs (DOA and DOPA) reflect the selected (addressed) word.

The enable ENB pin controls read, write, and reset for port B. When ENB is Low, no data is written and the outputs (DOB and DOPB) retain the last state. When ENB is High and reset (SSRB) is High, DOB and DOPB are set to SRVAL_B during the Low-to-High clock (CLKB) transition; if write enable (WEB) is High, the memory contents reflect the data at DIB and DIPB. When ENB is High and WEB is Low, the data stored in the RAM address (ADDRB) is read during the Low-to-High clock transition. By default, WRITE_MODE_B=WRITE_FIRST, when ENB and WEB are High, the data on the data inputs (DIB and PB) are loaded into the word selected by the write address (ADDRB) during the Low-to-High clock transition and the data outputs (DOB and DOPB) reflect the selected (addressed) word.

The above descriptions assume active High control pins (ENA, WEA, RSTA, CLKA, ENB, WEB, RSTB, and CLKB). However, the active level can be changed by placing an inverter on the port. Any inverter placed on a RAMB16 port is absorbed into the block and does not use a CLB resource.

Table 9-2 Port A Truth Table

Inputs								Outputs			
GSR	ENA	SSRA	WEA	CLKA	ADDRA	DIA	DIPA	DOA	DOPA	RAM Contents	
										Data RAM	Parity RAM
1	X	X	X	X	X	X	X	INIT_A	INIT_A	No Chg	No Chg
0	0	X	X	X	X	X	X	No Chg	No Chg	No Chg	No Chg
0	1	1	0	↑	X	X	X	SRVAL_A	SRVAL_A	No Chg	No Chg
0	1	1	1	↑	addr	data	pdata	SRVAL_A	SRVAL_A	RAM(addr) <=data	RAM(addr) <=pdata
0	1	0	0	↑	addr	X	X	RAM(addr)	RAM(addr)	No Chg	No Chg
0	1	0	1	↑	addr	data	pdata	No Chg[1] RAM (addr)[2] data[3]	No Chg[1] RAM(addr)[2] pdata[3]	RAM(addr) <=data	RAM(addr) <=pdata

GSR=Global Set Reset

INIT_A=Value specified by the INIT_A attribute for output register. Default is all zeros.
SRVAL_A=register value

addr=RAM address
RAM(addr)=RAM contents at address ADDR
data=RAM input data
pdata=RAM parity data

[1]WRITE_MODE_A=NO_CHANGE
[2]WRITE_MODE_A=READ_FIRST
[3]WRITE_MODE_A=WRITE_FIRST

Table 9-3 Port B Truth Table

Inputs								Outputs			
GSR	ENB	SSRB	WEB	CLKB	ADDRB	DIB	DIPB	DOB	DOPB	RAM Contents	
										Data RAM	Parity RAM
1	X	X	X	X	X	X	X	INIT_B	INIT_B	No Chg	No Chg
0	0	X	X	X	X	X	X	No Chg	No Chg	No Chg	No Chg
0	1	1	0	↑	X	X	X	SRVAL_B	SRVAL_B	No Chg	No Chg
0	1	1	1	↑	addr	data	pdata	SRVAL_B	SRVAL_B	RAM(addr) <=data	RAM(addr) <=pdata
0	1	0	0	↑	addr	X	X	RAM(addr)	RAM(addr)	No Chg	No Chg
0	1	0	1	↑	addr	data	pdata	No Chg[1] RAM (addr)[2] data[3]	No Chg[1] RAM(addr)[2] pdata[3]	RAM(addr) <=data	RAM(addr) <=pdata

GSR=Global Set Reset

INIT_B=Value specified by the INIT_B attribute for output registers. Default is all zeros.
SRVAL_B=register value

addr=RAM address
RAM(addr)=RAM contents at address ADDR
data=RAM input data
pdata=RAM parity data

[1]WRITE_MODE_B=NO_CHANGE
[2]WRITE_MODE_B=READ_FIRST
[3]WRITE_MODE_B=WRITE_FIRST

Address Mapping

Each port accesses the same set of 18432 memory cells using an addressing scheme that is dependent on the width of the port. For all port widths, 16384 memory cells are available for data as shown in Table 9-4. For 9-, 18-, and 36-bit wide ports, 2408 parity memory cells are also available as shown in Table 9-5. The physical RAM location that is addressed for a particular width is determined from the following formula.

```
Start=((ADDR port+1)*(Widthport)) -1
End=(ADDRport)*(Widthport)
```

The following tables shows address mapping for each port width.

Table 9-4 Port Address Mapping for Data

Data Width	Port Data Addresses																															
1	16384	<--	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	8192	<--	15		14		13		12		11		10		09		08		07		06		05		04		03		02		01		00	
4	4096	<--	07				06				05				04				03				02				01				00	
8	2048	<--	03								02								01								00					
16	1024	<--	01																00													
32	512	<--	00																													

Table 9-5 Port Address Mapping for Parity

Parity Width	Port Parity Addresses						
1	2048	<-----	03	02	01	00	
2	1024	<-----	01		00		
4	512	<-----	00				

Initializing Memory Contents of a Dual-Port RAMB16

You can use the INIT_xx attributes to specify an initialization value for the memory contents of a RAMB16 during device configuration. The initialization of each RAMB16_Sm_Sn is set by 64 initialization attributes (INIT_00 through INIT_3F) of 64 hex values for a total of 16384 bits.

You can use the INITP_xx attributes to specify an initial value for the parity memory during device configuration or assertion. The initialization of the parity memory for ports configured for 9, 18, or 36 bits is set by 8 initialization attributes (INITP_00 through INITP_07) of 64 hex values for a total of 2048 bits.

If any INIT_xx or INITP_xx attribute is not specified, it is configured as zeros. Partial strings are padded with zeros to the left.

See the *Constraints Guide* for more information on these attributes.

Initializing the Output Register of a Dual-Port RAMB16

In Virtex-II and Virtex-II PRO, each bit in an output register can be initialized at power on (when GSR is high) to either a 0 or 1. In addition, the initial state specified for power on can be different than the state that results from assertion of a set/reset. Four properties control initialization of the output register for a dual-port RAMB16: INIT_A, INIT_B, SRVAL_A, and SRVAL_B. The INIT_A attribute specifies the output register value at power on for port A and the INIT_B attribute specifies the value for port B. You can use the SRVAL_A attribute to define the state resulting from assertion of the SSR (set/reset) input on port A. You use the SRVAL_B attribute to define the state resulting from assertion of the SSR input on port B.

The INIT_A, INIT_B, SRVAL_A, and SRVAL_B attributes specify the initialization value as a hexadecimal string. The value is dependent upon the port width. For example, for a RAMB16_S1_S4 with port A width equal to 1 and port B width equal to 4, the port A output register contains 1 bit and the port B output register contains 4 bits. Therefore, the INIT_A or SRVAL_A value can only be specified as a 1 or 0. For port B, the output register contains 4 bits. In this case, you can use INIT_B or SRVAL_B to specify a hexadecimal value from 0 through F to initialize the 4 bits of the output register.

For those ports that include parity bits, the parity portion of the output register is specified in the high order bit position of the INIT_A, INIT_B, SRVAL_A, or SRVAL_B value.

The INIT and SRVAL attributes default to zero if they are not set by the user.

See the *Constraints Guide* for more information on these attributes.

Write Mode Selection

The WRITE_MODE_A attribute controls the memory and output contents of port A for a dual-port RAMB16. The WRITE_MODE_B attribute does the same for port B. By default, both WRITE_MODE_A and WRITE_MODE_B are set to WRITE_FIRST. This means that input is read, written to memory, and then passed to output. You can set the write mode for port A and / or port B to READ_FIRST to read the memory contents, pass the memory contents to the outputs, and then write the input to memory. Or, you can set the write mode to NO_CHANGE to have the input written to memory without changing the output. The "Port A and Port B Conflict Resolution" section describes how read / write conflicts are resolved when both port A and port B are attempting to read / write to the same memory cells.

Port A and Port B Conflict Resolution

Virtex-II and Virtex-II PRO block SelectRAM is True Dual-Port RAM that allows both ports to simultaneously access the same memory cell. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. For a list of specifics of conflict resolution for port and memory cell write operations that have either a clock common to both ports or synchronous clocks on each port, see *Virtex-II User Guide, Chapter 2, Design Considerations, Using BlockSelectRAM Memory, Conflict Resolution.*

The following tables summarize the collision detection behavior of the dual-port RAMB16 based on the WRITE_MODE_A and WRITE_MODE_B settings.

Table 9-6 WRITE_MODE_A=NO_CHANGE and WRITE_MODE_B=NO_CHANGE

WEA	WEB	CLKA	CLKB	DIA	DIB	DIPA	DIPB	DOA	DOB	DOPA	DOPB	Data RAM	Parity Ram
0	0	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	No Chg	No Chg
1	0	↑	↑	DIA	DIB	DIPA	DIPB	No Chg	X	No Chg	X	DIA	DIPA
0	1	↑	↑	DIA	DIB	DIPA	DIPB	X	No Chg	X	No Chg	DIB	DIPB
1	1	↑	↑	DIA	DIB	DIPA	DIPB	No Chg	No Chg	No Chg	No Chg	X	X

Table 9-7 WRITE_MODE_A=READ_FIRST and WRITE_MODE_B=READ_FIRST

WEA	WEB	CLKA	CLKB	DIA	DIB	DIPA	DIPB	DOA	DOB	DOPA	DOPB	Data RAM	Parity Ram
0	0	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	No Chg	No Chg
1	0	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	DIA	DIPA
0	1	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	DIB	DIPB
1	1	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	X	X

Table 9-8 WRITE_MODE_A=WRITE_FIRST and WRITE_MODE_B=WRITE_FIRST

WEA	WEB	CLKA	CLKB	DIA	DIB	DIPA	DIPB	DOA	DOB	DOPA	DOPB	Data RAM	Parity Ram
0	0	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	No Chg	No Chg
1	0	↑	↑	DIA	DIB	DIPA	DIPB	DIA	X	DIPA	X	DIA	DIPA

Table 9-8 WRITE_MODE_A=WRITE_FIRST and WRITE_MODE_B=WRITE_FIRST

WEA	WEB	CLKA	CLKB	DIA	DIB	DIPA	DIPB	DOA	DOB	DOPA	DOPB	Data RAM	Parity Ram
0	1	↑	↑	DIA	DIB	DIPA	DIPB	X	DIB	X	DIPB	DIB	DIPB
1	1	↑	↑	DIA	DIB	DIPA	DIPB	X	X	X	X	X	X

Table 9-9 WRITE_MODE_A=NO_CHANGE and WRITE_MODE_B=READ_FIRST

WEA	WEB	CLKA	CLKB	DIA	DIB	DIPA	DIPB	DOA	DOB	DOPA	DOPB	Data RAM	Parity Ram
0	0	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	No Chg	No Chg
1	0	↑	↑	DIA	DIB	DIPA	DIPB	No Chg	X	No Chg	X	DIA	DIPA
0	1	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	DIB	DIPB
1	1	↑	↑	DIA	DIB	DIPA	DIPB	No Chg	X	No Chg	X	DIB	DIPB

Table 9-10 WRITE_MODE_A=NO_CHANGE and WRITE_MODE_B=READ_FIRST

WEA	WEB	CLKA	CLKB	DIA	DIB	DIPA	DIPB	DOA	DOB	DOPA	DOPB	Data RAM	Parity Ram
0	0	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	No Chg	No Chg
1	0	↑	↑	DIA	DIB	DIPA	DIPB	No Chg	X	No Chg	X	DIA	DIPA
0	1	↑	↑	DIA	DIB	DIPA	DIPB	X	DIB	X	DIPB	DIB	DIPB
1	1	↑	↑	DIA	DIB	DIPA	DIPB	No Chg	X	No Chg	X	X	X

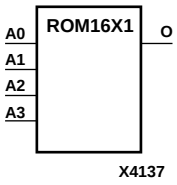
Table 9-11 WRITE_MODE_A=NO_CHANGE and WRITE_MODE_B=READ_FIRST

WEA	WEB	CLKA	CLKB	DIA	DIB	DIPA	DIPB	DOA	DOB	DOPA	DOPB	Data RAM	Parity Ram
0	0	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	No Chg	No Chg
1	0	↑	↑	DIA	DIB	DIPA	DIPB	RAM	RAM	RAM	RAM	DIA	DIPA
0	1	↑	↑	DIA	DIB	DIPA	DIPB	X	DIB	X	DIPB	DIB	DIPB
1	1	↑	↑	DIA	DIB	DIPA	DIPB	X	DIB	X	DIPB	DIA	DIPA

ROM16X1

16-Deep by 1-Wide ROM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



ROM16X1 is a 16-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 4-bit address (A3 – A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of four hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. For example, the INIT=10A7 parameter produces the data stream:

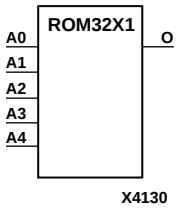
```
0001 0000 1010 0111
```

An error occurs if the INIT=*value* is not specified. See the appropriate CAE tool interface user guide for details.

ROM32X1

32-Deep by 1-Wide ROM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



ROM32X1 is a 32-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 5-bit address (A4 – A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of eight hexadecimal digits that are written into the ROM from the most-significant digit A=1FH to the least-significant digit A=00H. For example, the INIT=10A78F39 parameter produces the data stream:

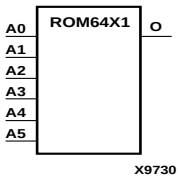
```
0001 0000 1010 0111 1000 1111 0011 1001
```

An error occurs if the INIT=*value* is not specified. See the appropriate CAE tool interface user guide for details.

ROM64X1

64-Deep by 1-Wide ROM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



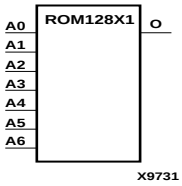
ROM64X1 is a 64-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 4-bit address (A5 – A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of four hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H.

An error occurs if the INIT=*value* is not specified. See the appropriate CAE tool interface user guide for details.

ROM128X1

128-Deep by 1-Wide ROM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



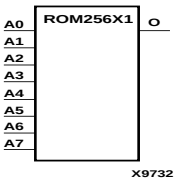
ROM128X1 is a 16-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 4-bit address (A6 – A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of four hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H.

An error occurs if the INIT=*value* is not specified. See the appropriate CAE tool interface user guide for details.

ROM256X1

256-Deep by 1-Wide ROM

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



ROM256X1 is a 16-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 4-bit address (A7– A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of four hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H.

An error occurs if the INIT=*value* is not specified. See the appropriate CAE tool interface user guide for details.

Chapter 10

SOP3-4 to XORCY_L

SOP3-4

Sum of Products

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
SOP3, SOP3B1A, SOP3B1B, SOP3B2A, SOP3B2B, SOP3B3 SOP4, SOP4B1, SOP4B2A, SOP4B2B, SOP4B3, SOP4B4	Macro	Macro	Macro	Macro	Macro	Macro

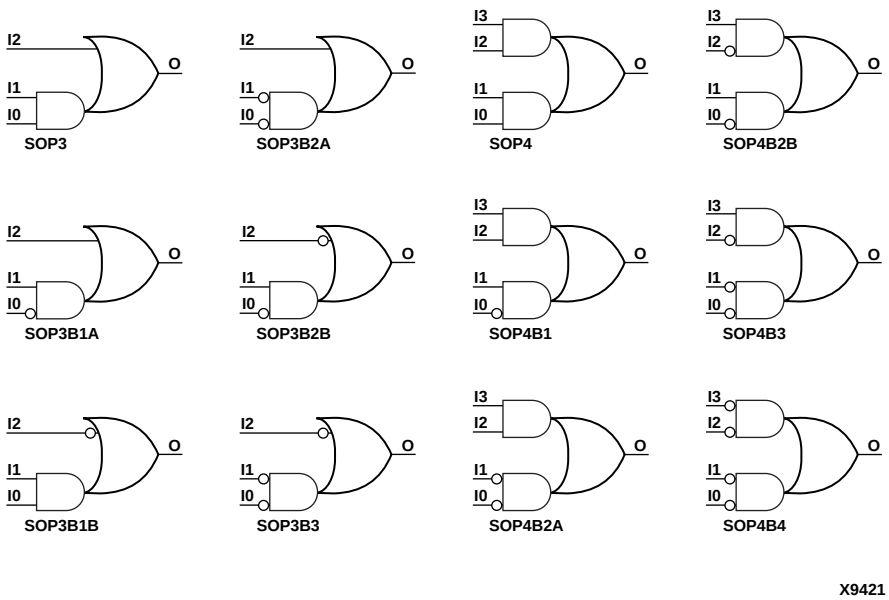


Figure 10-1 SOP Gate Representations

Sum Of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions or the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

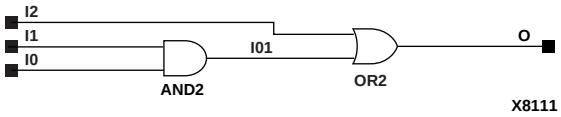


Figure 10-2 SOP3 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

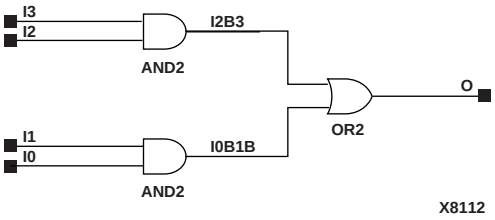


Figure 10-3 SOP4 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E

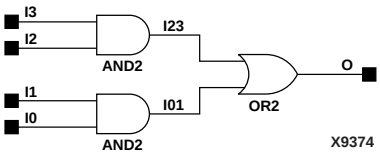
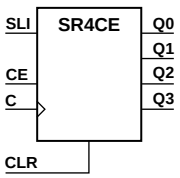


Figure 10-4 SOP4 Implementation Virtex-II, Virtex-II PRO

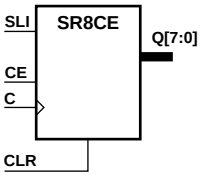
SR4CE, SR8CE, SR16CE

4-, 8-, 16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear

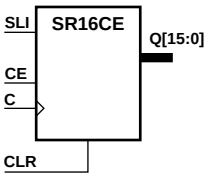
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



X4145



X4151



X4157

SR4CE, SR8CE, and SR16CE are 4-, 8-, and 16-bit shift registers, respectively, with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The CLR input, when High, overrides all other inputs and resets the data outputs (Q) Low. When CE is High and CLR is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent Low-to-High clock transitions, when CE is High and CLR is Low, data is shifted to the next highest bit position as new data is loaded into Q0 (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output (Q3 for SR4CE, Q7 for SR8CE, or Q15 for SR16CE) of one stage to the SLI input of the next stage and connecting clock, CE, and CLR in parallel.

The register is asynchronously cleared, outputs Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs	
CLR	CE	SLI	C	Q0	Qz – Q1
1	X	X	X	0	0
0	0	X	X	No Chg	No Chg
0	1	1	↑	1	qn-1
0	1	0	↑	0	qn-1

z = 3 for SR4CE; z = 7for SR8CE; z = 15 for SR16CE

qn-1 = state of referenced output one setup time prior to active clock transition

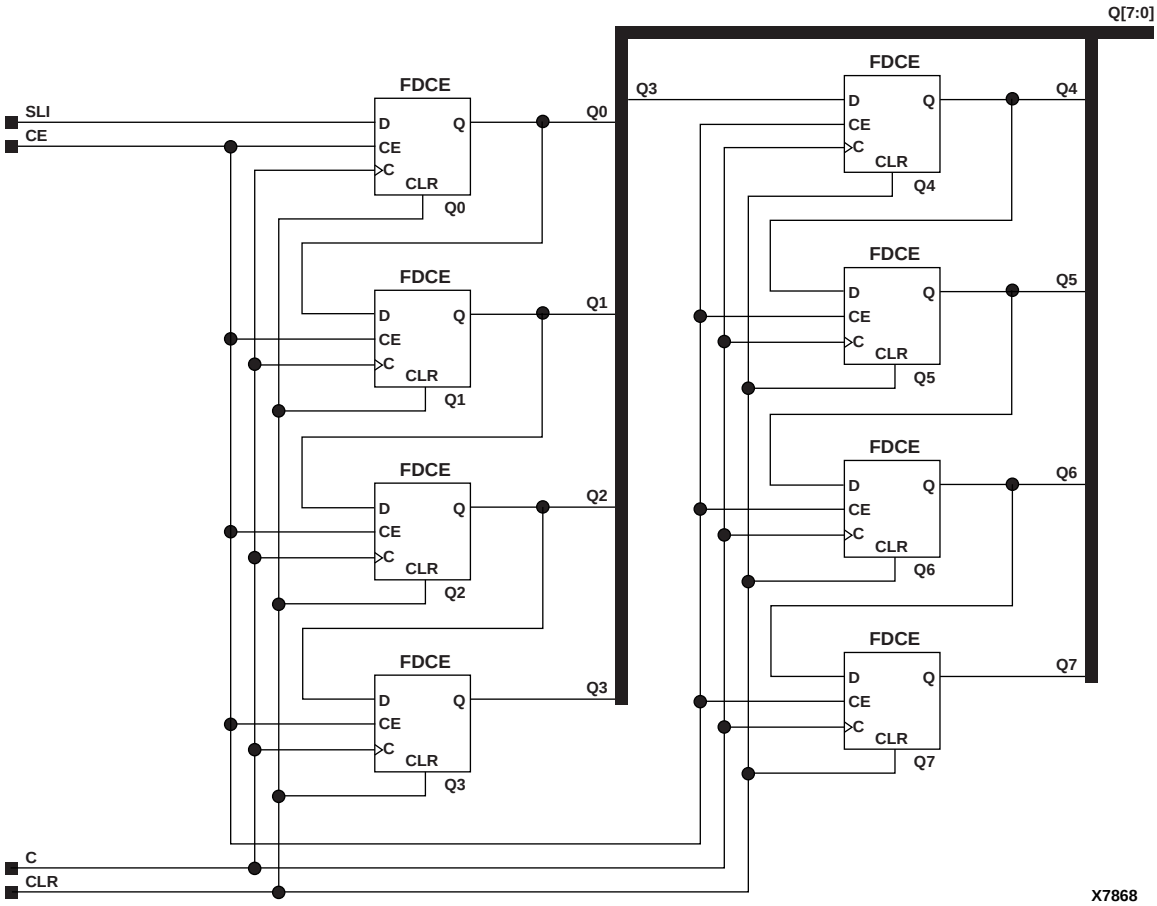
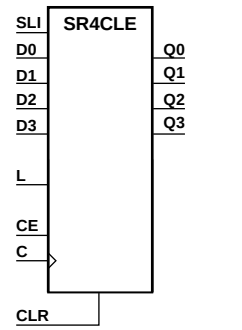


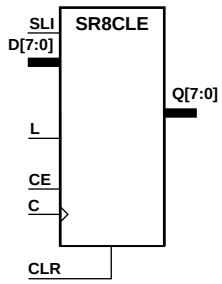
Figure 10-5 SR8CE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

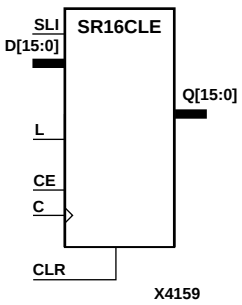
SR4CLE, SR8CLE, SR16CLE

4-, 8-, 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







SR4CLE, SR8CLE, and SR16CLE are 4-, 8-, and 16-bit shift registers, respectively, with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR).The register ignores clock transitions when L and CE are Low. The asynchronous CLR, when High, overrides all other inputs and resets the data outputs (Q) Low. When L is High and CLR is Low, data on the Dn – D0 inputs is loaded into the corresponding Qn – Q0 bits of the register. When CE is High and L and CLR are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and CLR are Low, the data is shifted to the next highest bit position as new data is loaded into Q0 (SLI→Q0, Q0→Q1, Q1→Q2, and so forth).

Registers can be cascaded by connecting the last Q output (Q3 for SR4CLE, Q7 for SR8CLE, or Q15 for SR16CLE) of one stage to the SLI input of the next stage and connecting clock, CE, L, and CLR inputs in parallel.

The register is asynchronously cleared, outputs Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs						Outputs	
CLR	L	CE	SLI	Dn – D0	C	Q0	Qz – Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn – D0	↑	d0	dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Chg	No Chg

z = 3 for SR4CLE; z = 7 for SR8CLE; z = 15 for SR16CLE

dn = state of referenced input one setup time prior to active clock transition

qn-1 = state of referenced output one setup time prior to active clock transition

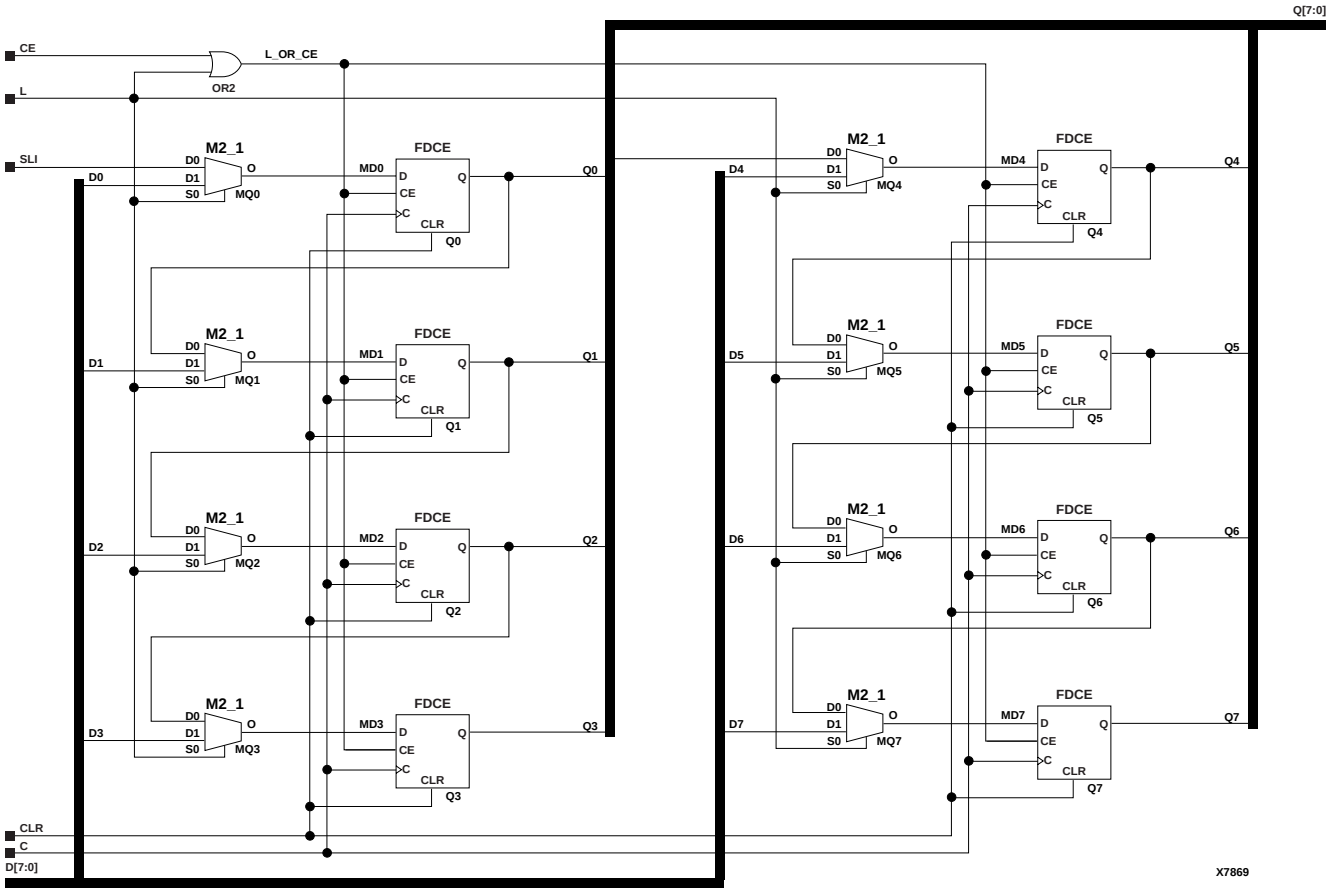
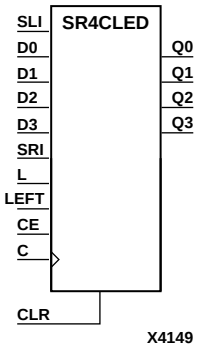


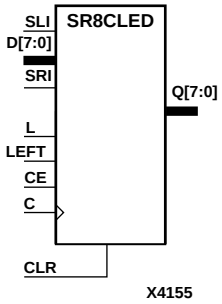
Figure 10-6 SR8CLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

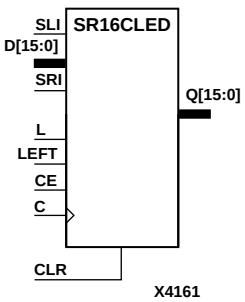
SR4CLED, SR8CLED, SR16CLED

4-, 8-, 16-Bit Shift Registers with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







SR4CLED, SR8CLED, and SR16CLED are 4-, 8-, and 16-bit shift registers, respectively, with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left / right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when CE and L are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low. When L is High and CLR is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and CLR are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into Q0 during the Low-to-High clock transition and shifted left (to Q1, Q2, and so forth) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last Q output (Q3 for SR4CLED, Q7 for SR8CLED, or Q15 for SR16CLED) during the Low-to-High clock transition and shifted right (to Q2, Q1,... for SR4CLED; to Q6, Q5,... for SR8CLED; and to Q14, Q13,... for SR16CLED) during subsequent clock transitions. The truth tables for SR4CLED, SR8CLED, and SR16CLED indicate the state of the Q outputs under all input conditions for SR4CLED, SR8CLED, and SR16CLED.

The register is asynchronously cleared, outputs Low, when power is applied.

For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Table 10-1 SR4CLED Truth Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D3 – D0	C	Q0	Q3	Q2 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D3– D0	↑	d0	d3	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition

Table 10-2 SR8CLED Truth Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D7 – D0	C	Q0	Q7	Q6 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D7 – D0	↑	d0	d7	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Table 10-3 SR16CLED Truth Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D15 – D0	C	Q0	Q15	Q14 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D15 – D0	↑	d0	d15	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

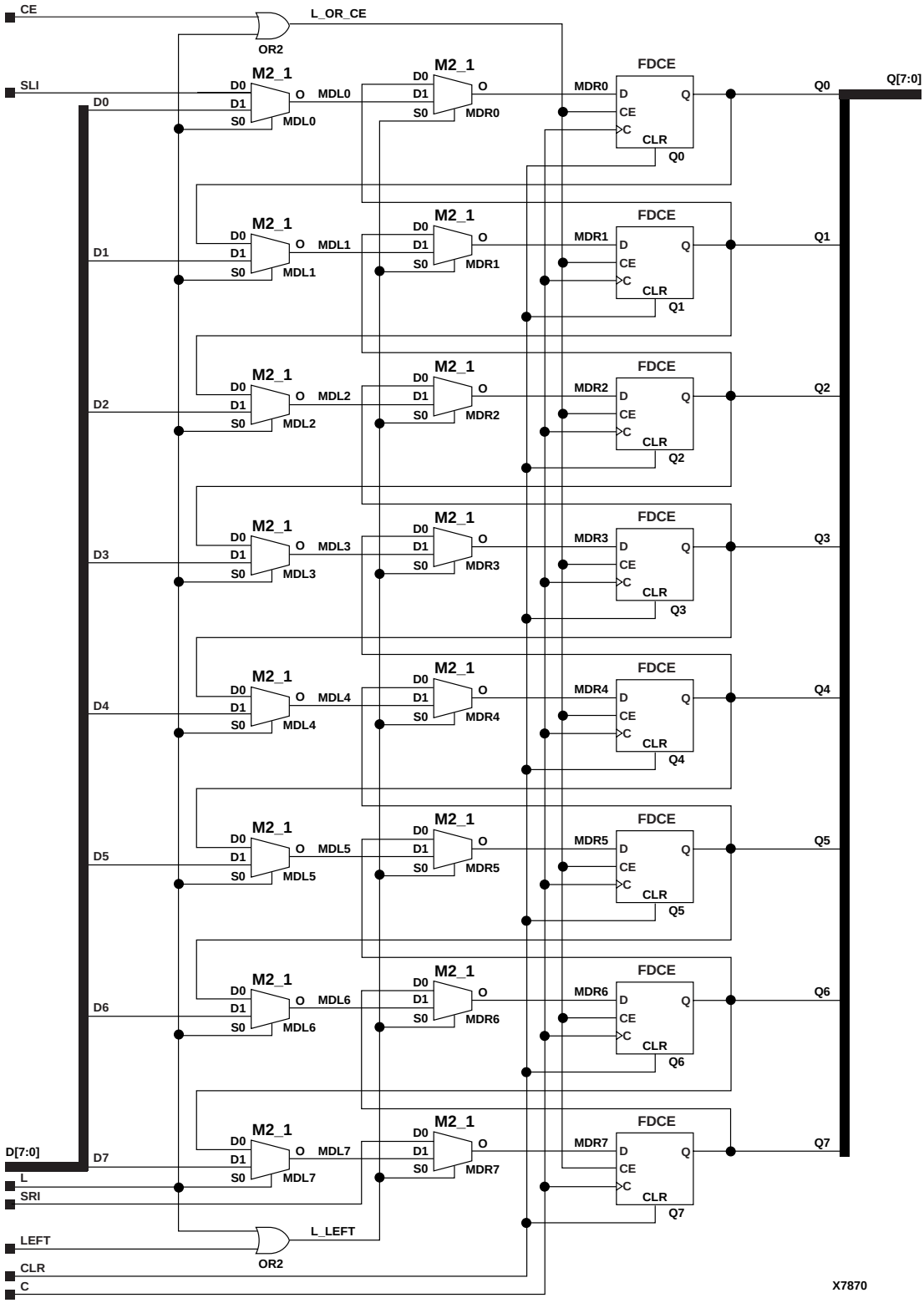


Figure 10-7 SR8CLED Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

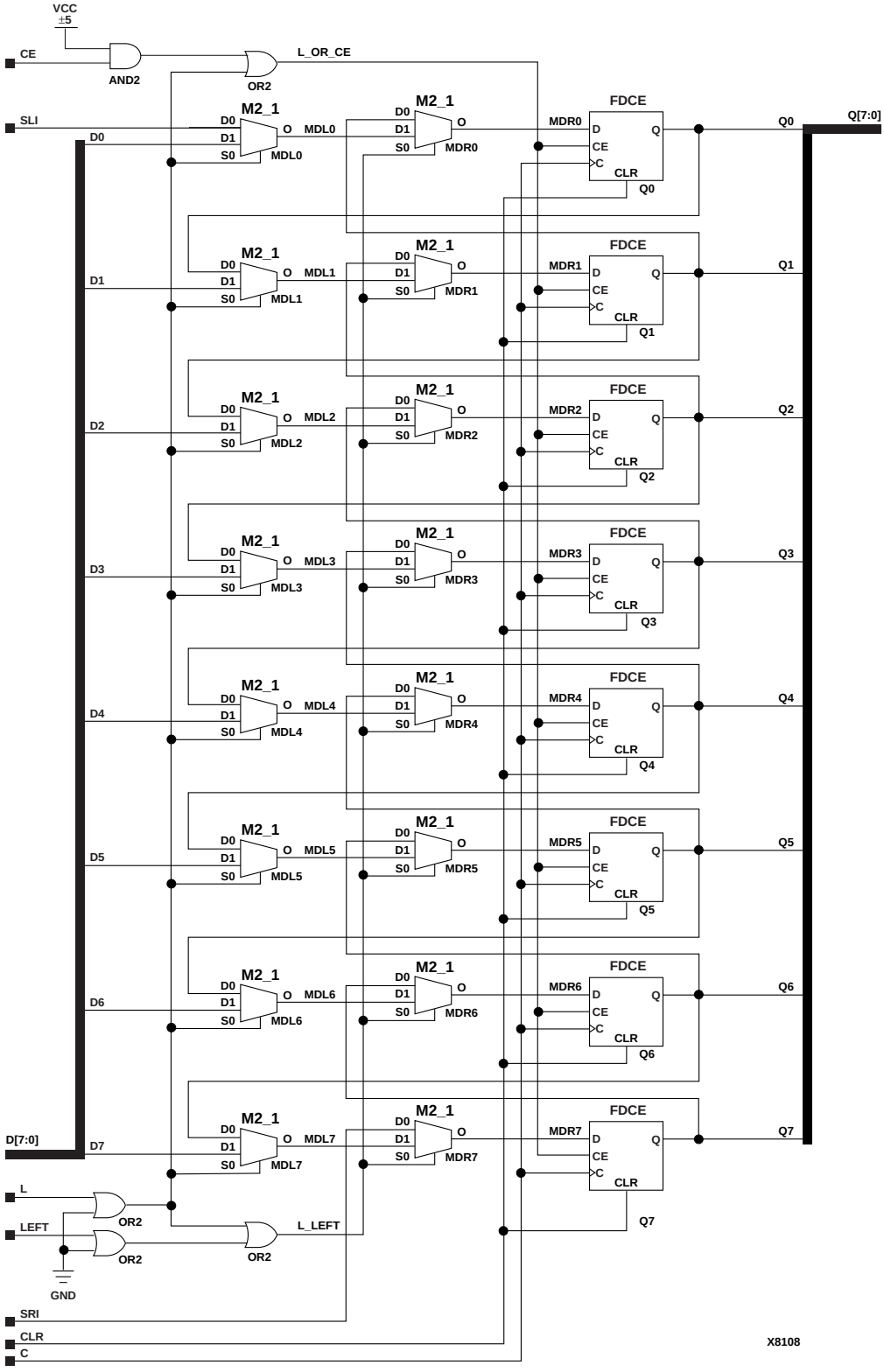
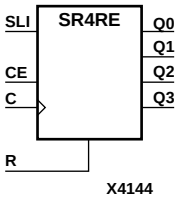


Figure 10-8 SR8CLED Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

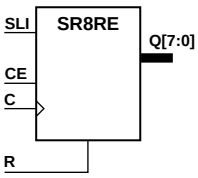
SR4RE, SR8RE, SR16RE

4-, 8-, 16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset

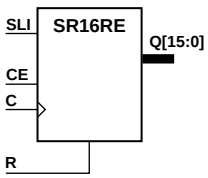
Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro



X4144



X4150



X4156

SR4RE, SR8RE, and SR16RE are 4-, 8-, and 16-bit shift registers, respectively, with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When CE is High and R is Low, the data on the SLI is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent Low-to-High clock transitions, when CE is High and R is Low, data is shifted to the next highest bit position as new data is loaded into Q0 (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output (Q3 for SR4RE, Q7 for SR8RE, or Q15 for SR16RE) of one stage to the SLI input of the next stage and connecting clock, CE, and R in parallel.

The register is asynchronously cleared, outputs Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs				Outputs	
R	CE	SLI	C	Q0	Qz – Q1
1	X	X	↑	0	0
0	0	X	X	No Chg	No Chg
0	1	1	↑	1	qn-1
0	1	0	↑	0	qn-1

z = 3 for SR4RE; z = 7 for SR8RE; z = 15 for SR16RE

qn-1 = state of referenced output one setup time prior to active clock transition

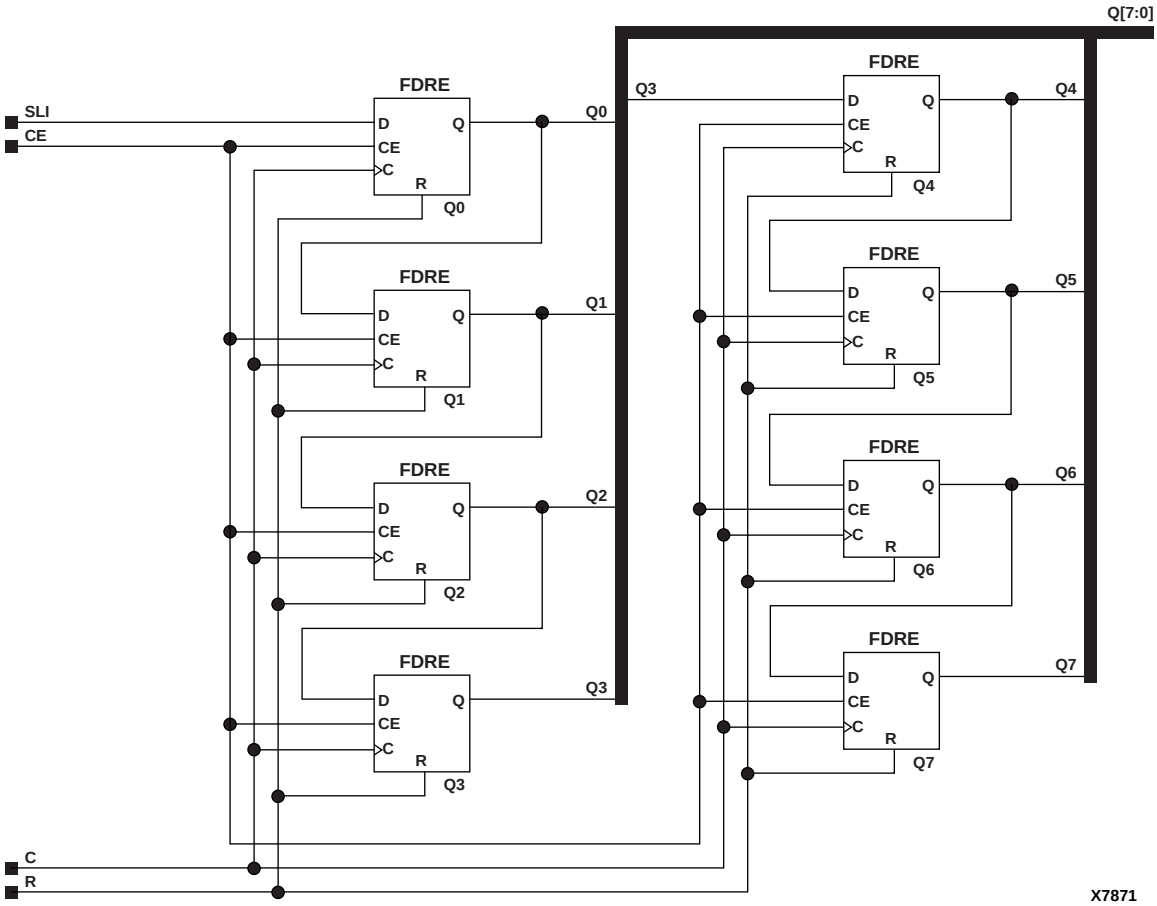
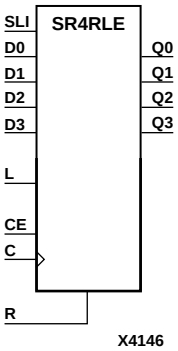


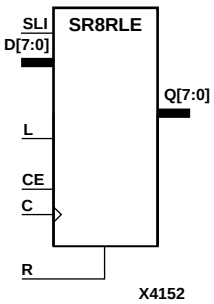
Figure 10-9 SR8RE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

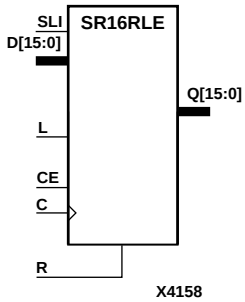
SR4RLE, SR8RLE, SR16RLE

4-, 8-, 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







SR4RLE, SR8RLE, and SR16RLE are 4-, 8-, and 16-bit shift registers, respectively, with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when L and CE are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and R are Low, the data is shifted to the next highest bit position as new data is loaded into Q0 (SLI→Q0, Q0→Q1, Q1→Q2, and so forth).

Registers can be cascaded by connecting the last Q output (Q3 for SR4RLE, Q7 for SR8RLE, or 15 for SR16RLE) of one stage to the SLI input of the next stage and connecting clock, CE, L, and R inputs in parallel.

The register is asynchronously cleared, outputs Low, when power is applied.

For XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set/reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Inputs						Outputs	
R	L	CE	SLI	Dz – D0	C	Q0	Qz – Q1
1	X	X	X	X	↑	0	0
0	1	X	X	Dz – D0	↑	d0	dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Chg	No Chg

z = 3 for SR4RLE; z = 7 for SR8RLE; z = 15 for SR16RLE

dn = state of referenced input one setup time prior to active clock transition

qn-1 = state of referenced output one setup time prior to active clock transition

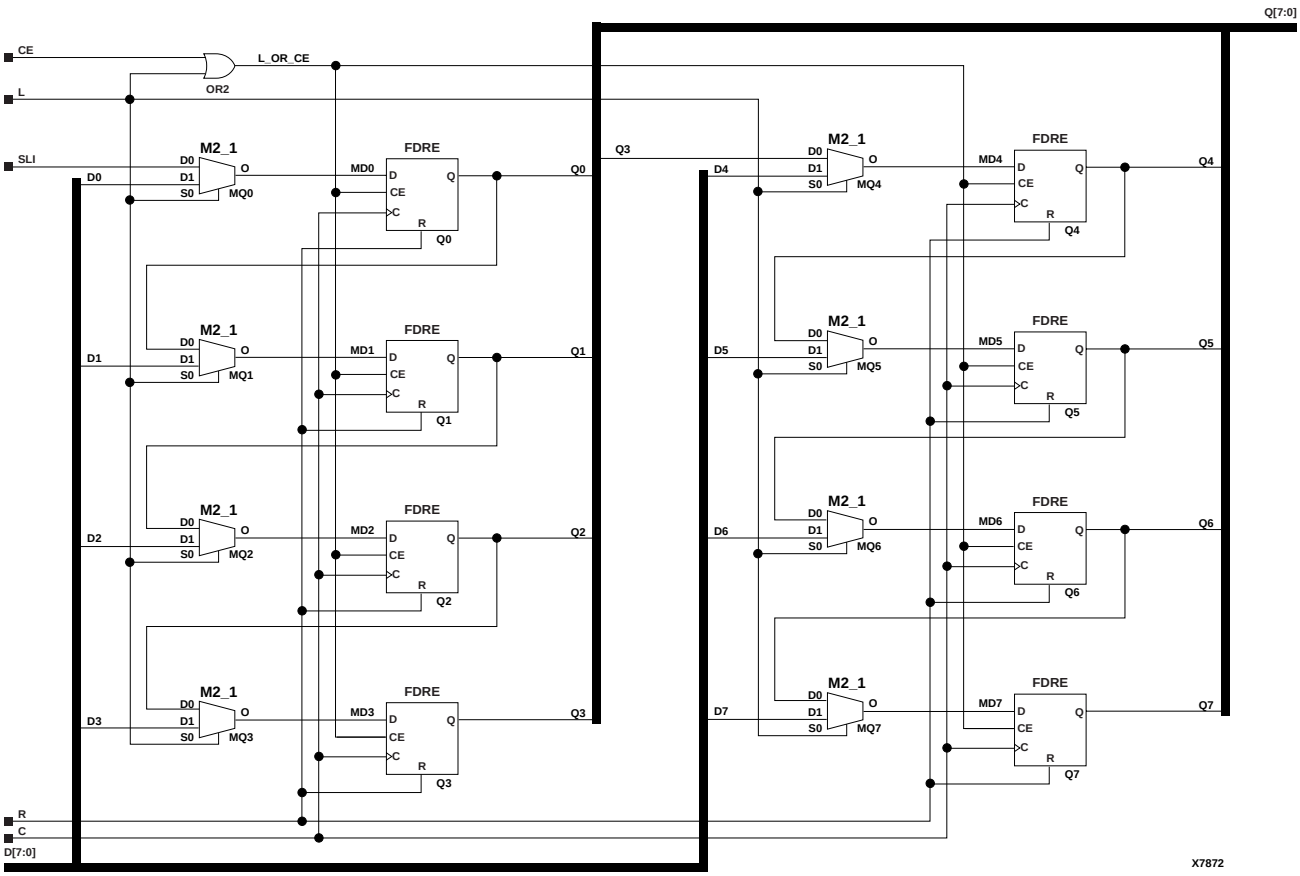
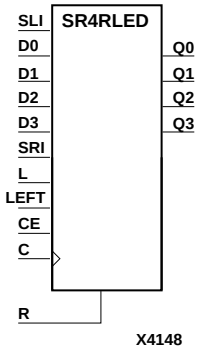


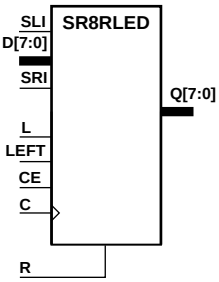
Figure 10-10 SR8RLE Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

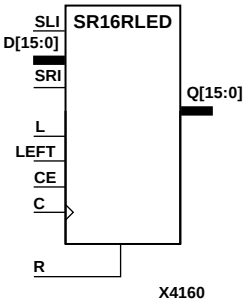
SR4RLED, SR8RLED, SR16RLED

4-, 8-, 16-Bit Shift Registers with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Macro	Macro	Macro	Macro	Macro	Macro







SR4RLED, SR8RLED, and SR16RLED are 4-, 8-, and 16-bit shift registers, respectively, with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left / right (LEFT), and synchronous reset (R). The register ignores clock transitions when CE and L are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on SLI is loaded into Q0 during the Low-to-High clock transition and shifted left (to Q1, Q2, and so forth) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last Q output (Q3 for SR4RLED, Q7 for SR8RLED, or Q15 for SR16RLED) during the Low-to-High clock transition and shifted right (to Q2, Q1,... for SR4RLED; to Q6, Q5,... for SR8RLED; or to Q14, Q13,... for SR16RLED) during subsequent clock transitions. The truth table indicates the state of the Q outputs under all input conditions.

The register is asynchronously cleared, outputs Low, when power is applied.

For XC9500 / XV / XL, CoolRunner XPLA3, and CoolRunner-II, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, and Virtex-II PRO simulate power-on when global set / reset (GSR) is active.

GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN2, STARTUP_VIRTEX, or STARTUP_VIRTEX2 symbol.

Table 10-4 SR4RLED Truth Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D3 – D0	C	Q0	Q3	Q2 – Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D3 – D0	↑	d0	d3	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Table 10-5 SR8RLED Truth Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D7– D0	C	Q0	Q7	Q6 – Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D7 – D0	↑	d0	d7	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Table 10-6 SR16RLED Truth Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D15 – D0	C	Q0	Q15	Q14 – Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D15 – D0	↑	d0	d15	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

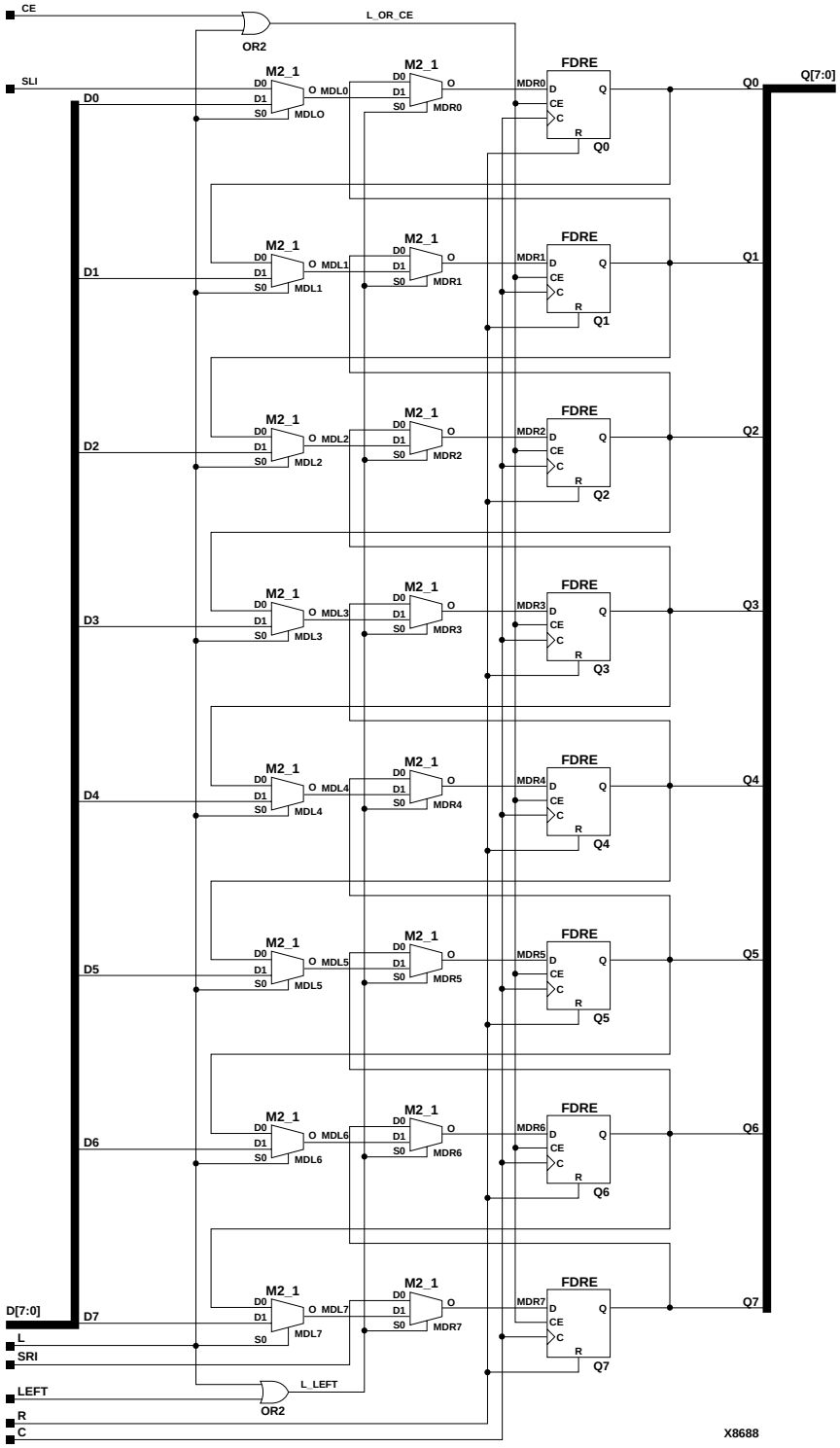
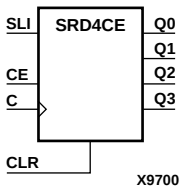


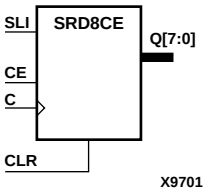
Figure 10-11 SR8RLED Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex-II, Virtex-II PRO

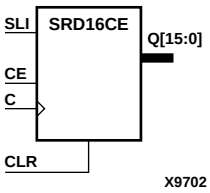
SRD4CE, SRD8CE, SRD16CE

4-, 8-, 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Registers with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	N / A	N / A	Macro







SRD4CE, SRD8CE, and SRD16CE are 4-, 8-, and 16-bit dual edge triggered shift registers, respectively, with a shift-left serial input (SLI), parallel outputs (Q), clock enable (CE) and asynchronous clear (CLR) inputs. The CLR input, when High, overrides all other inputs and resets the data outputs (Q) Low. When CE is High and CLR is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and CLR is Low, data is shifted to the next highest bit position as new data is loaded into Q0 (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output (Q3 for SRD4CE, Q7 for SRD8CE, or Q15 for SRD16CE) of one stage to the SLI input of the next stage and connecting clock, CE, and CLR in parallel.

The register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs	
CLR	CE	SLI	C	Q0	Qz – Q1
1	X	X	X	0	0
0	0	X	X	No Chg	No Chg
0	1	1	↑	1	qn-1
0	1	1	↓	1	qn-1
0	1	0	↑	0	qn-1
0	1	0	↓	0	qn-1

z = 3 for SRD4CE; z = 7for SRD8CE; z = 15 for SRD16CE

qn-1 = state of referenced output one setup time prior to active clock transition

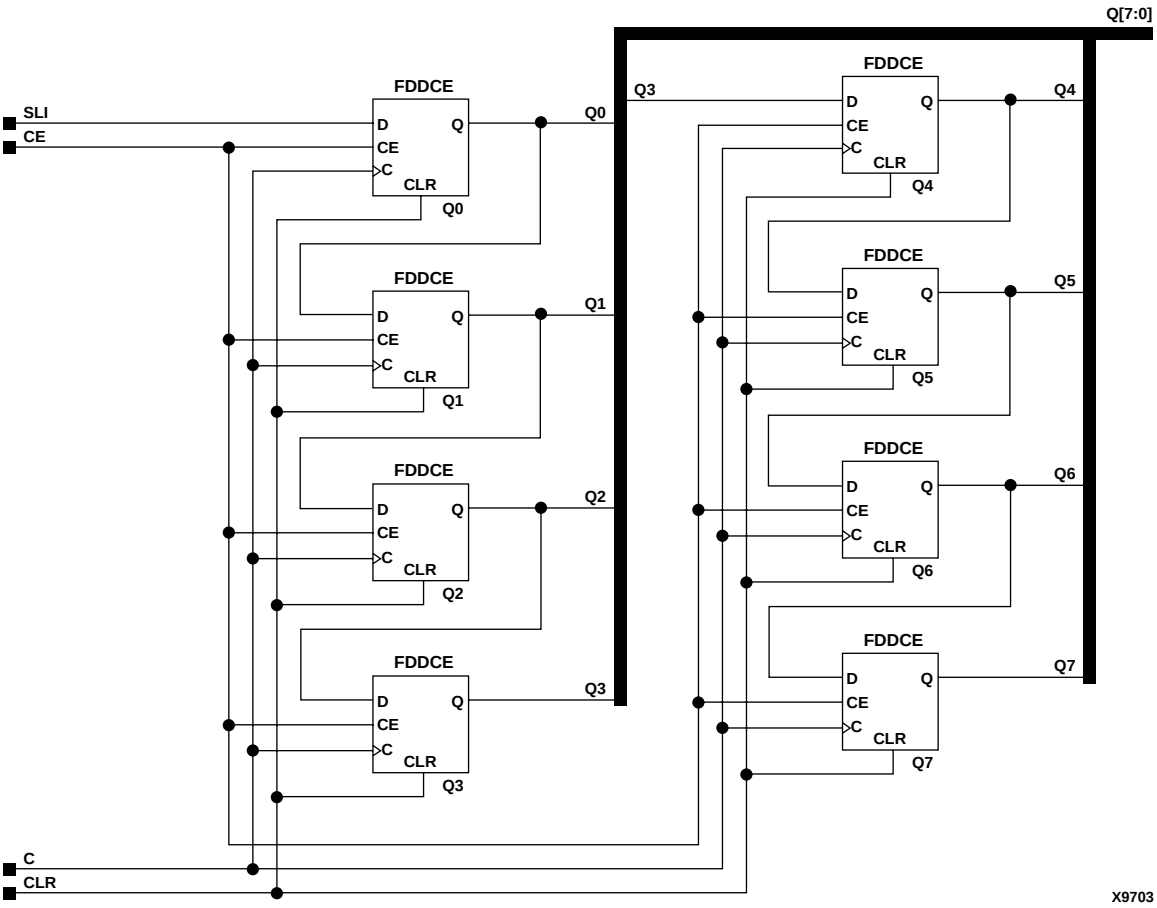
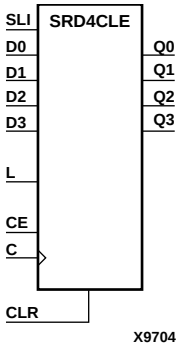


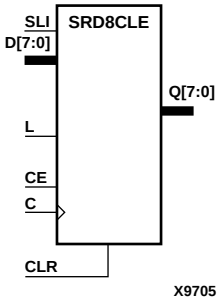
Figure 10-12 SRD8CE Implementation CoolRunner-II

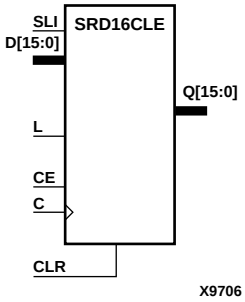
SRD4CLE, SRD8CLE, SRD16CLE

4-, 8-, 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Registers with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro







SRD4CLE, SRD8CLE, and SRD16CLE are 4-, 8-, and 16-bit dual edge triggered shift registers, respectively, with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR).The register ignores clock transitions when L and CE are Low. The asynchronous CLR, when High, overrides all other inputs and resets the data outputs (Q) Low. When L is High and CLR is Low, data on the Dn – D0 inputs is loaded into the corresponding Qn – Q0 bits of the register. When CE is High and L and CLR are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and CLR are Low, the data is shifted to the next highest bit position as new data is loaded into Q0 (SLI→Q0, Q0→Q1, Q1→Q2, and so forth).

Registers can be cascaded by connecting the last Q output (Q3 for SRD4CLE, Q7 for SRD8CLE, or Q15 for SRD16CLE) of one stage to the SLI input of the next stage and connecting clock, CE, L, and CLR inputs in parallel.

The register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs	
CLR	L	CE	SLI	Dn – D0	C	Q0	Qz – Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn – D0	↑	d0	dn
0	1	X	X	Dn – D0	↓	d0	dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	1	SLI	X	↓	SLI	qn-1
0	0	0	X	X	X	No Chg	No Chg

z = 3 for SRD4CLE; z = 7 for SRD8CLE; z = 15 for SRD16CLE

dn = state of referenced input one setup time prior to active clock transition

qn-1 = state of referenced output one setup time prior to active clock transition

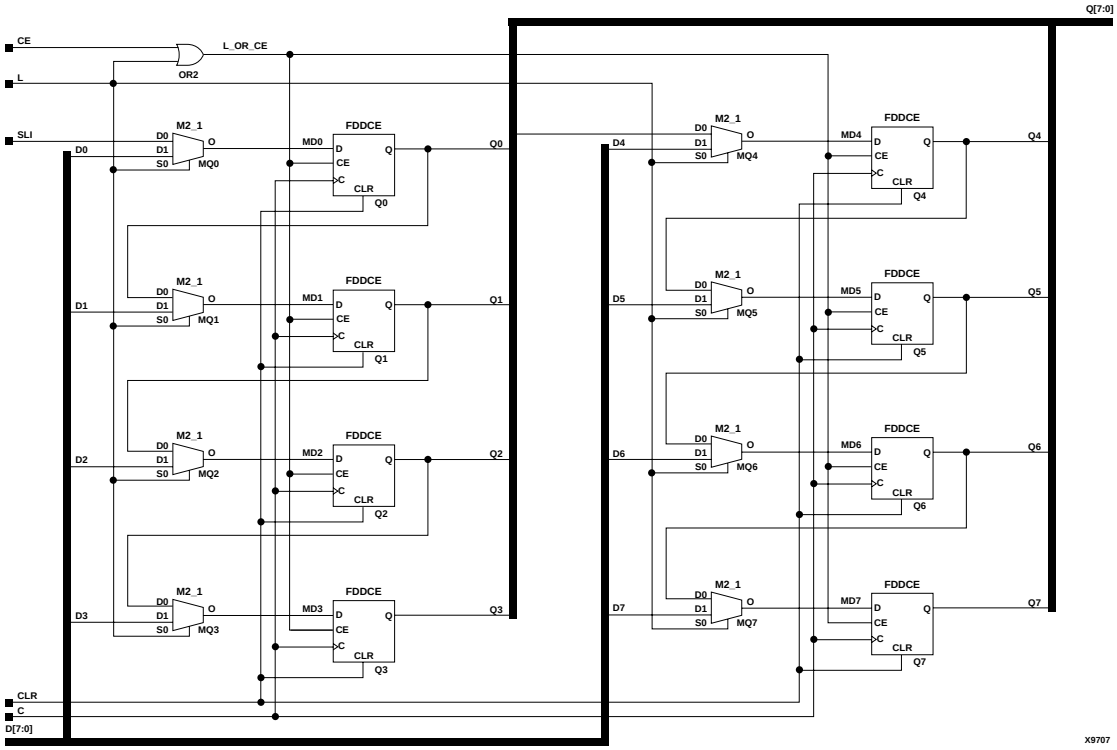
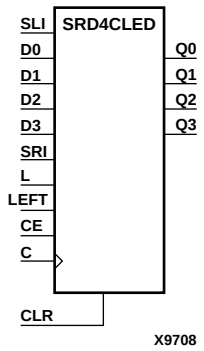


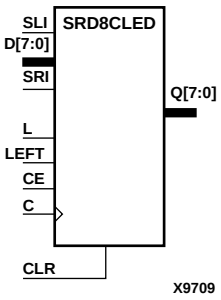
Figure 10-13 SRD8CLE Implementation CoolRunner-II

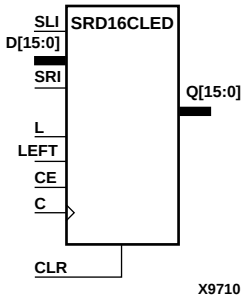
SRD4CLED, SRD8CLED, SRD16CLED

4-, 8-, 16-Bit Dual Edge Triggered Shift Registers with Clock Enable and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro







SRD4CLED, SRD8CLED, and SRD16CLED are 4-, 8-, and 16-bit dual edge triggered shift registers, respectively, with shift-left (SLI) and shift-right (SRDI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left / right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when CE and L are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low. When L is High and CLR is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and CLR are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left (to Q1, Q2, and so forth) during subsequent clock transitions. If LEFT is Low, data on the SRDI is loaded into the last Q output (Q3 for SRD4CLED, Q7 for SRD8CLED, or Q15 for SRD16CLED) during the Low-to-High or High-to-Low clock transition and shifted right (to Q2, Q1,... for SRD4CLED; to Q6, Q5,... for SRD8CLED; and to Q14, Q13,... for SRD16CLED) during subsequent clock transitions. The truth tables for SRD4CLED, SRD8CLED, and SRD16CLED indicate the state of the Q outputs under all input conditions for SRD4CLED, SRD8CLED, and SRD16CLED.

The register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Table 10-7 SRD4CLED Truth Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRDI	D3 – D0	C	Q0	Q3	Q2 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D3– D0	↑	d0	d3	dn
0	1	X	X	X	X	D3– D0	↓	d0	d3	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q2	qn-1
0	0	1	0	X	SRDI	X	↑	q1	SRI	qn+1
0	0	1	0	X	SRDI	X	↓	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition

Table 10-8 SRD8CLED Truth Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRDI	D7 – D0	C	Q0	Q7	Q6 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D7 – D0	↑	d0	d7	dn
0	1	X	X	X	X	D7 – D0	↓	d0	d7	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q6	qn-1
0	0	1	0	X	SRDI	X	↑	q1	SRI	qn+1
0	0	1	0	X	SRDI	X	↓	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Table 10-9 SRD16CLED Truth Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRDI	D15 – D0	C	Q0	Q15	Q14 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D15 – D0	↑	d0	d15	dn
0	1	X	X	X	X	D15 – D0	↓	d0	d15	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q14	qn-1
0	0	1	0	X	SRDI	X	↑	q1	SRI	qn+1
0	0	1	0	X	SRDI	X	↓	q1	SRI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

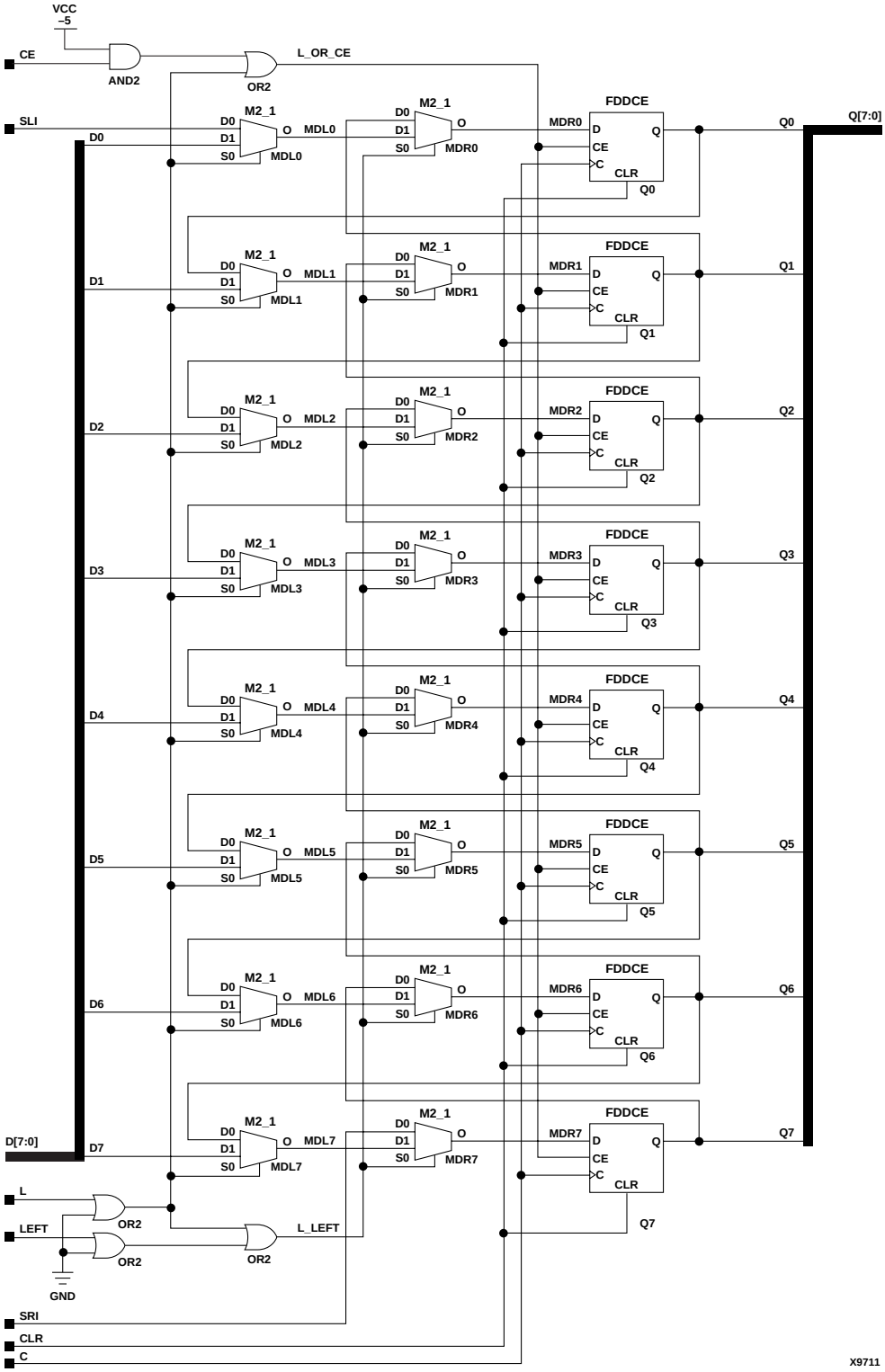
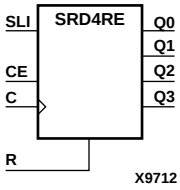


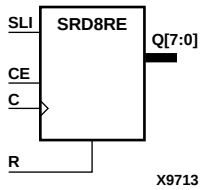
Figure 10-14 SRD8CLED Implementation CoolRunner-II

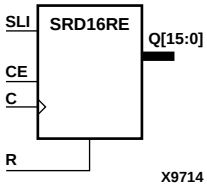
SRD4RE, SRD8RE, SRD16RE

4-, 8-, 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Registers with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro







SRD4RE, SRD8RE, and SRD16RE are 4-, 8-, and 16-bit dual edge triggered shift registers, respectively, with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When CE is High and R is Low, the data on the SLI is loaded into the first bit of the shift register during the Low-to-High clock or High-to-Low (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and R is Low, data is shifted to the next highest bit position as new data is loaded into Q0 (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output (Q3 for SRD4RE, Q7 for SRD8RE, or Q15 for SRD16RE) of one stage to the SLI input of the next stage and connecting clock, CE, and R in parallel.

The register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs	
R	CE	SLI	C	Q0	Qz – Q1
1	X	X	↑	0	0
1	X	X	↓	0	0
0	0	X	X	No Chg	No Chg
0	1	1	↑	1	qn-1
0	1	1	↓	1	qn-1
0	1	0	↑	0	qn-1
0	1	0	↓	0	qn-1

z = 3 for SRD4RE; z = 7 for SRD8RE; z = 15 for SRD16RE

qn-1 = state of referenced output one setup time prior to active clock transition

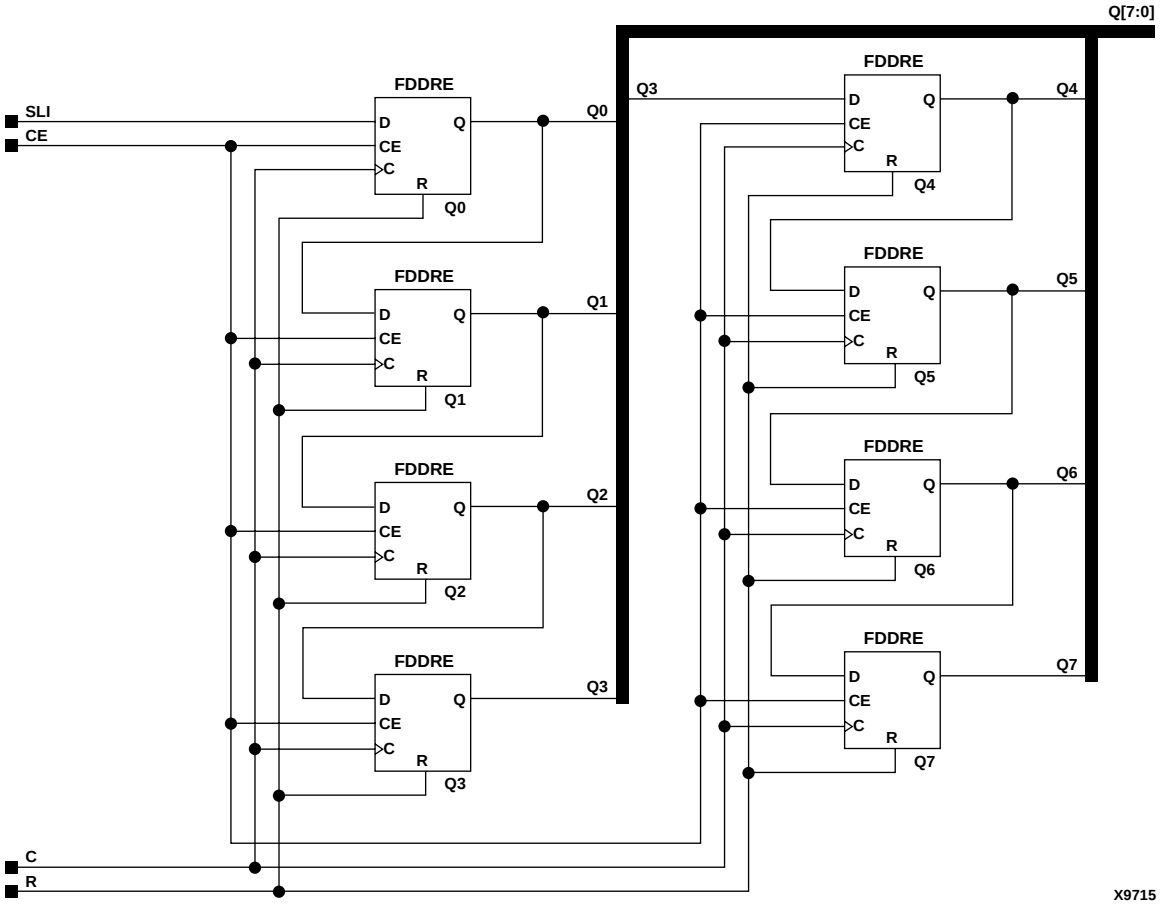
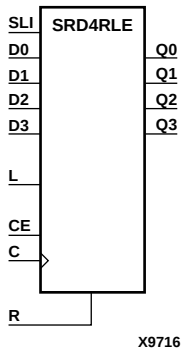


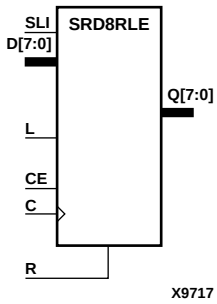
Figure 10-15 SRD8RE Implementation CoolRunner-II

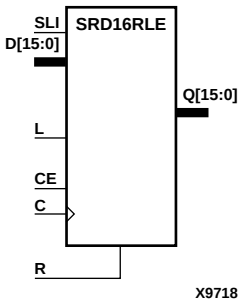
SRD4RLE, SRD8RLE, SRD16RLE

4-, 8-, 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Registers with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro







SRD4RLE, SRD8RLE, and SRD16RLE are 4-, 8-, and 16-bit dual edge triggered shift registers, respectively, with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when L and CE are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High or High-to-Low clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and R are Low, the data is shifted to the next highest bit position as new data is loaded into Q0 (SLI→Q0, Q0→Q1, Q1→Q2, and so forth).

Registers can be cascaded by connecting the last Q output (Q3 for SRD4RLE, Q7 for SRD8RLE, or 15 for SRD16RLE) of one stage to the SLI input of the next stage and connecting clock, CE, L, and R inputs in parallel.

The register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs	
R	L	CE	SLI	Dz – D0	C	Q0	Qz – Q1
1	X	X	X	X	↑	0	0
1	X	X	X	X	↓	0	0
0	1	X	X	Dz – D0	↑	d0	dn
0	1	X	X	Dz – D0	↓	d0	dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	1	SLI	X	↓	SLI	qn-1
0	0	0	X	X	X	No Chg	No Chg

z = 3 for SRD4RLE; z = 7 for SRD8RLE; z = 15 for SRD16RLE

dn = state of referenced input one setup time prior to active clock transition

qn-1 = state of referenced output one setup time prior to active clock transition

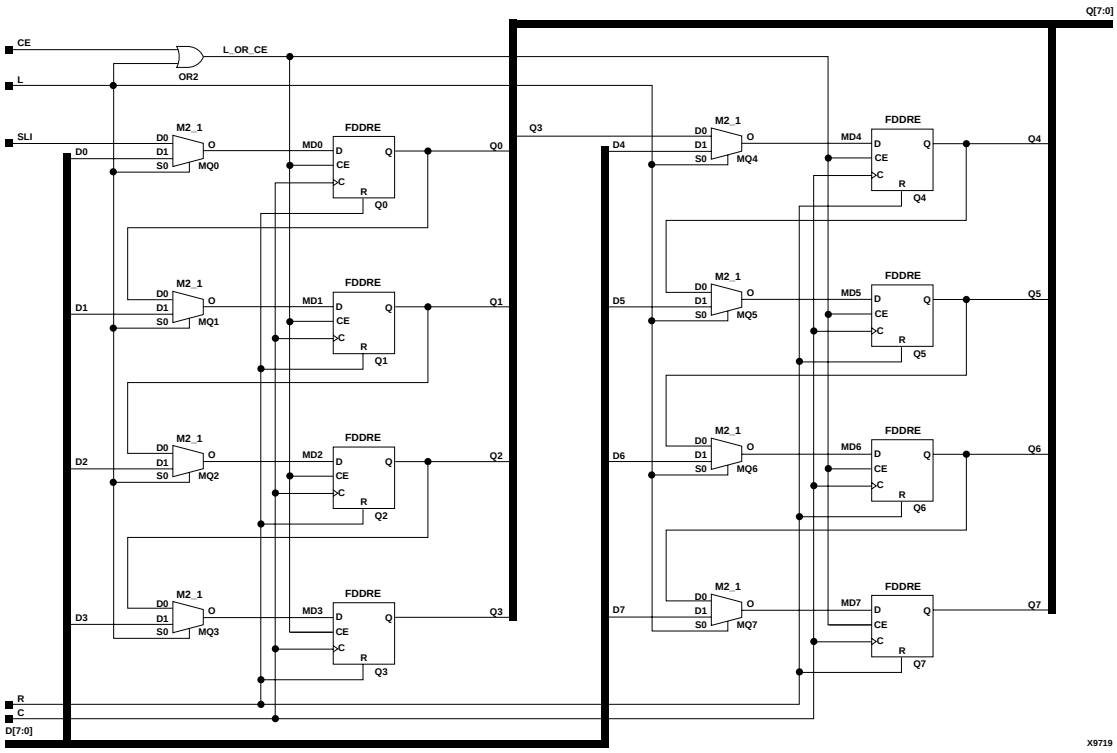
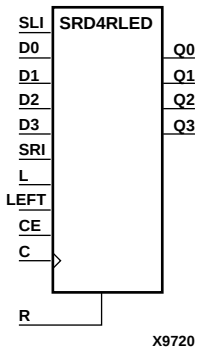


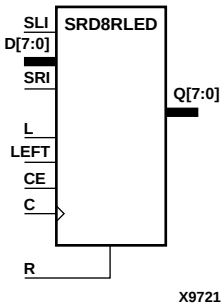
Figure 10-16 SRD8RLE Implementation CoolRunner-II

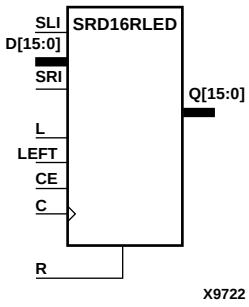
SRD4RLED, SRD8RLED, SRD16RLED

4-, 8-, 16-Bit Dual Edge Triggered Shift Registers with Clock Enable and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	N/A	N/A	Macro







SRD4RLED, SRD8RLED, and SRD16RLED are 4-, 8-, and 16-bit dual edge triggered shift registers, respectively, with shift-left (SLI) and shift-right (SRDI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs — clock enable (CE), load enable (L), shift left / right (LEFT), and synchronous reset (R). The register ignores clock transitions when CE and L are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left (to Q1, Q2, and so forth) during subsequent clock transitions. If LEFT is Low, data on the SRDI is loaded into the last Q output (Q3 for SRD4RLED, Q7 for SRD8RLED, or Q15 for SRD16RLED) during the Low-to-High or Hihg-to-Low clock transition and shifted right (to Q2, Q1,... for SRD4RLED; to Q6, Q5,... for SRD8RLED; or to Q14, Q13,... for SRD16RLED) during subsequent clock transitions. The truth table indicates the state of the Q outputs under all input conditions.

The register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Table 10-10 SRD4RLED Truth Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRDI	D3 – D0	C	Q0	Q3	Q2 – Q1
1	X	X	X	X	X	X	↑	0	0	0
1	X	X	X	X	X	X	↓	0	0	0
0	1	X	X	X	X	D3 – D0	↑	d0	d3	dn
0	1	X	X	X	X	D3 – D0	↓	d0	d3	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q2	qn-1
0	0	1	0	X	SRDI	X	↑	q1	SRDI	qn+1

Table 10-10 SRD4RLED Truth Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRDI	D3 – D0	C	Q0	Q3	Q2 – Q1
0	0	1	0	X	SRDI	X	↓	q1	SRDI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Table 10-11 SRD8RLED Truth Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRDI	D7– D0	C	Q0	Q7	Q6 – Q1
1	X	X	X	X	X	X	↑	0	0	0
1	X	X	X	X	X	X	↓	0	0	0
0	1	X	X	X	X	D7 – D0	↑	d0	d7	dn
0	1	X	X	X	X	D7 – D0	↓	d0	d7	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q6	qn-1
0	0	1	0	X	SRDI	X	↑	q1	SRDI	qn+1
0	0	1	0	X	SRDI	X	↓	q1	SRDI	qn+1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Table 10-12 SRD16RLED Truth Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRDI	D15 – D0	C	Q0	Q15	Q14 – Q1
1	X	X	X	X	X	X	↑	0	0	0
1	X	X	X	X	X	X	↓	0	0	0
0	1	X	X	X	X	D15 – D0	↑	d0	d15	dn
0	1	X	X	X	X	D15 – D0	↓	d0	d15	dn
0	0	0	X	X	X	X	X	No Chg	No Chg	No Chg
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q14	qn-1

dn = state of referenced input one setup time prior to active clock transition

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

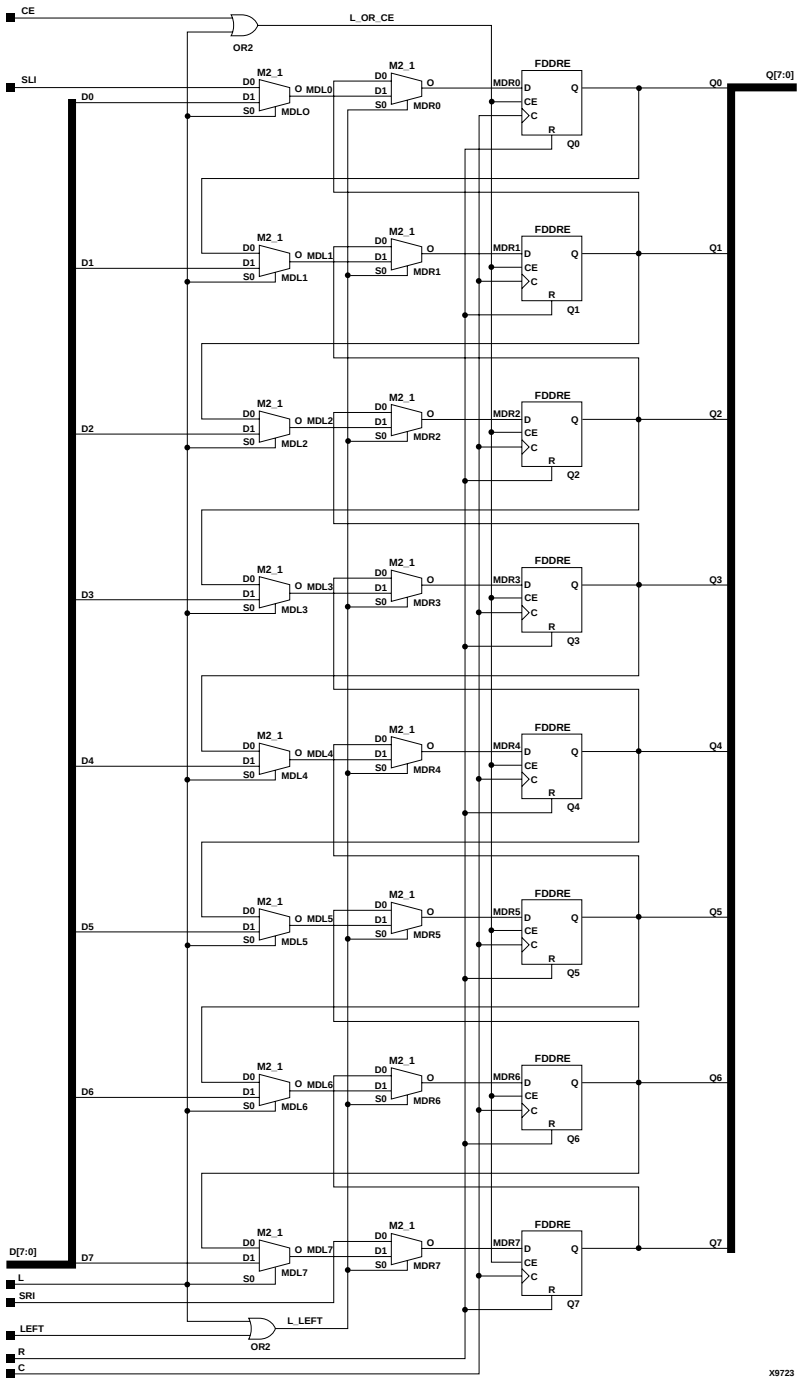
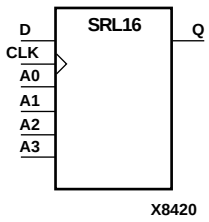


Figure 10-17 SRD8RLED Implementation CoolRunner-II

SRL16

16-Bit Shift Register Look-Up-Table (LUT)

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



SRL16 is a shift register look up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register. The shift register may be of a fixed, static length or it may be dynamically adjusted.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Static Length Mode

To get a fixed length shift register, drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits as determined from the following formula:

```
Length = (8*A3) +(4*A2) + (2*A1) + A0 +1
```

If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.

Dynamic Length Mode

The length of the shift register can be changed dynamically by changing the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits.

Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

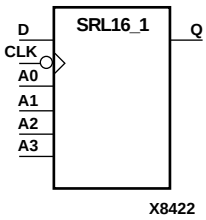
Inputs			Output
Am	CLK	D	Q
Am	X	X	Q(Am)
Am	↑	D	Q(Am-1)

m= 0, 1, 2, 3

SRL16_1

16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



SRL16_1 is a shift register look up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register. The shift register may be of a fixed, static length or it may be dynamically adjusted. See "Static Length Mode" and "Dynamic Length Mode" in the "SRL16" section.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

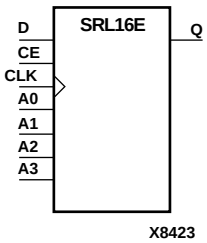
Inputs			Output
Am	CLK	D	Q
Am	X	X	Q(Am)
Am	↓	D	Q(Am-1)

m= 0, 1, 2, 3

SRL16E

16-Bit Shift Register Look-Up-Table (LUT) with Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



SRL16E is a shift register look up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register. The shift register may be of a fixed, static length or dynamically adjusted. See "Static Length Mode" and "Dynamic Length Mode" in the "SRL16" section.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions, when CE is High, data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

When CE is Low, the register ignores clock transitions.

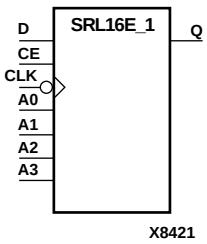
Inputs				Output
Am	CE	CLK	D	Q
Am	0	X	X	Q(Am)
Am	1	↑	D	Q(Am-1)

m= 0, 1, 2, 3

SRL16E_1

16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



SRL16E_1 is a shift register look up table (LUT) with clock enable (CE). The inputs A3, A2, A1, and A0 select the output length of the shift register. The shift register may be of a fixed, static length or dynamically adjusted. See "Static Length Mode" and "Dynamic Length Mode" in the "SRL16" section.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions, when CE is High, data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

When CE is Low, the register ignores clock transitions.

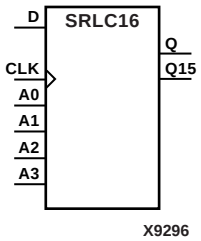
Inputs				Output
Am	CE	CLK	D	Q
Am	0	X	X	Q(Am)
Am	1	↓	D	Q(Am-1)

m= 0, 1, 2, 3

SRLC16

16-Bit Shift Register Look-Up-Table (LUT) with Carry

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



SRLC16 is a shift register look up table (LUT) with Carry. The inputs A3, A2, A1, and A0 select the output length of the shift register. The shift register may be of a fixed, static length or it may be dynamically adjusted.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

The Q15 output is available for the user to cascade multiple shift register LUTs to create larger shift registers.

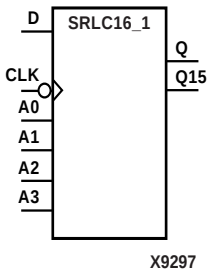
For information about the static length mode, see “Static Length Mode” in the SRL16 section.

For information about the dynamic length mode, see “Dynamic Length Mode” in the SRL16 section.

SRLC16_1

16-Bit Shift Register Look-Up-Table (LUT) with Carry and Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



SRLC16_1 is a shift register look up table (LUT) with carry and a negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register. The shift register may be of a fixed, static length or it may be dynamically adjusted. See “Static Length Mode” and “Dynamic Length Mode” in the "SRL16" section.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

The Q15 output is available for the user to cascade multiple shift register LUTs to create larger shift registers.

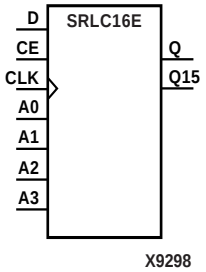
Inputs			Output	
Am	CLK	D	Q	Q15
Am	X	X	Q(Am)	No Chg
Am	↓	D	Q(Am-1)	Q14

m= 0, 1, 2, 3

SRLC16E

16-Bit Shift Register Look-Up-Table (LUT) with Carry and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



SRLC16E is a shift register look up table (LUT) with carry and clock enable. The inputs A3, A2, A1, and A0 select the output length of the shift register. The shift register may be of a fixed, static length or it may be dynamically adjusted.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

The Q15 output is available for the user to cascade multiple shift register LUTs to create larger shift registers.

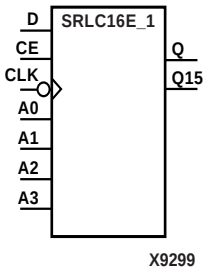
For information about the static length mode, see "Static Length Mode" in the SRL16 section.

For information about the dynamic length mode, see "Dynamic Length Mode" in the SRL16 section.

SRLC16E_1

16-Bit Shift Register Look-Up-Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



SRLC16E_1 is a shift register look up table (LUT) with carry, clock enable, and negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register. The shift register may be of a fixed, static length or it may be dynamically adjusted. See "SRLC16_1" and "Dynamic Length Mode" in the "SRL16" section.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

The Q15 output is available for the user to cascade multiple shift register LUTs to create larger shift registers.

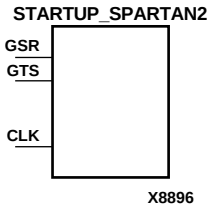
Inputs				Output	
Am	CE	CLK	D	Q	Q15
Am	0	X	X	Q(Am)	No Chg
Am	1	↓	D	Q(Am-1)	Q14

m= 0, 1, 2, 3

STARTUP_SPARTAN2

Spartan-II User Interface to Global Clock, Reset, and 3-State Controls

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	N/A	N/A	N/A	N/A	N/A



The STARTUP_SPARTAN2 primitive is used for Global Set/Reset, global 3-state control, and the user configuration clock. The Global Set/Reset (GSR) input, when High, sets or resets all flip-flops, all latches, and every block RAM (RAMB4) output register in the device, depending on the initialization state (S or R) of the component.

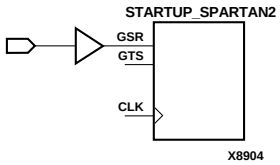
Note Block RAMB4 content, LUT RAMs, delay locked loop elements (CLKDLL, CLKDLLHF, BUFGDLL), and shift register LUTs (SRL16, SRL16_1, SRL16E, SRL16E_1) are not set/reset.

Following configuration, the global 3-state control (GTS), when High—and BSCAN is not enabled and executing an EXTEST instruction—forces all the IOB outputs into high impedance mode, which isolates the device outputs from the circuit but leaves the inputs active.

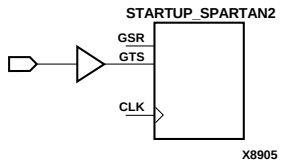
Note GTS= Global Tri State

Including the STARTUP_SPARTAN2 symbol in a design is optional. You must include the symbol under the following conditions.

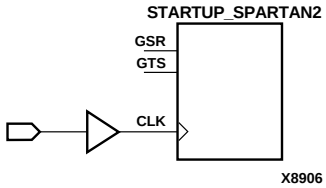
- To exert external control over global set/reset, connect the GSR pin to a top level port and an IBUF, as shown here.



- To exert external control over global 3-state, connect the GTS pin to a top level port and IBUF, as shown here.



- To synchronize startup to a user clock, connect the user clock signal to the CLK input, as shown here. Furthermore, “user clock” must be selected in the BitGen program.

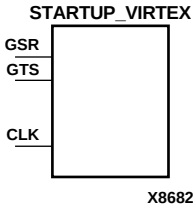


You can use location constraints to specify the pin from which GSR or GTS (or both) is accessed.

STARTUP_VIRTEX

Virtex and Virtex-E User Interface to Global Clock, Reset, and 3-State Controls

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	Primitive	N/A	N/A	N/A	N/A



The STARTUP_VIRTEX primitive is used for Global Set/Reset, global 3-state control, and the user configuration clock. The Global Set/Reset (GSR) input, when High, sets or resets all flip-flops, all latches, and every block RAM (RAMB4) output register in the device, depending on the initialization state (S or R) of the component. For Virtex-II and Virtex-II PRO, see "STARTUP_VIRTEX2".

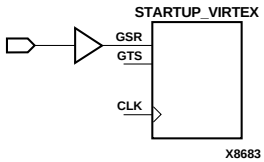
Note Block RAMB4 content, LUT RAMs, delay locked loop elements (CLKDLL, CLKDLLHF, BUFGDLL), and shift register LUTs (SRL16, SRL16_1, SRL16E, SRL16E_1) are not set/reset.

Following configuration, the global 3-state control (GTS), when High—and BSCAN is not enabled and executing an EXTEST instruction—forces all the IOB outputs into high impedance mode, which isolates the device outputs from the circuit but leaves the inputs active.

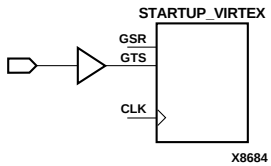
Note GTS= Global Tri State

Including the STARTUP_VIRTEX symbol in a design is optional. You must include the symbol under the following conditions.

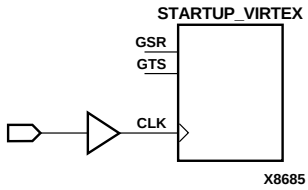
- To exert external control over global set/reset, connect the GSR pin to a top level port and an IBUF, as shown here.



- To exert external control over global 3-state, connect the GTS pin to a top level port and IBUF, as shown here.



- To synchronize startup to a user clock, connect the user clock signal to the CLK input, as shown here. Furthermore, "user clock" must be selected in the BitGen program.

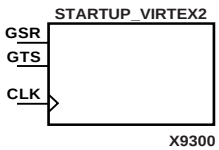


You can use location constraints to specify the pin from which GSR or GTS (or both) is accessed.

STARTUP_VIRTEX2

Virtex-II and Virtex-II PRO User Interface to Global Clock, Reset, and 3-State Controls

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	Primitive	N/A	N/A	N/A



The STARTUP_VIRTEX2 primitive is used for Global Set/Reset, global 3-state control, and the user configuration clock. The Global Set/Reset (GSR) input, when High, sets or resets all flip-flops, all latches, and every block RAMB16 output register in the device, depending on the initialization state (INIT=1 or 0) of the component. For Virtex and Virtex-E, see "STARTUP_VIRTEX".

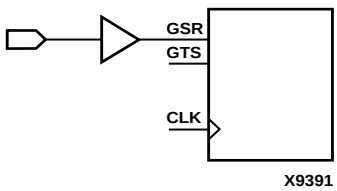
Note Block RAM content, LUT RAMs, the Digital Clock Manager (DCM), and shift register LUTs (SRL16, SRL16_1, SRL16E, SRL16E_1, SRLC16, SRLC16_1, SRLC16E, and SRLC16E_1) are not set/reset.

Following configuration, the global 3-state control (GTS), when High—and BSCAN is not enabled and executing an EXTEST instruction—forces all the IOB outputs into high impedance mode, which isolates the device outputs from the circuit but leaves the inputs active.

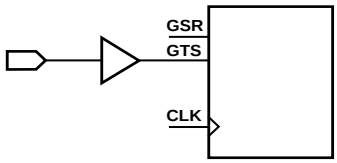
Note GTS= Global Tri State

Including the STARTUP_VIRTEX2 symbol in a design is optional. You must include the symbol under the following conditions.

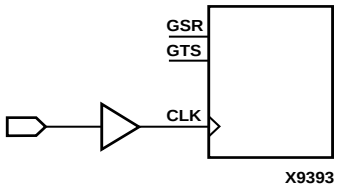
- To exert external control over global set/reset, connect the GSR pin to a top level port and an IBUF, as shown here.



- To exert external control over global 3-state, connect the GTS pin to a top level port and IBUF, as shown here.



- To synchronize startup to a user clock, connect the user clock signal to the CLK input, as shown here. Furthermore, "user clock" must be selected in the BitGen program.

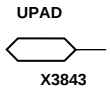


You can use location constraints to specify the pin from which GSR or GTS (or both) is accessed.

UPAD

Connects the I/O Node of an IOB to the Internal PLD Circuit

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



A UPAD allows the use of any unbonded IOBs in a device. It is used the same way as a IOPAD except that the signal output is not visible on any external device pins.

VCC

VCC-Connection Signal Tag

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

X8721

The VCC signal tag or parameter forces a net or input function to a logic High level. A net tied to VCC cannot have any other source.

When the placement and routing software encounters a net or input function tied to VCC, it removes any logic that is disabled by the VCC signal. The VCC signal is only implemented when the disabled logic cannot be removed.

XNOR2-9

2- to 9-Input XNOR Gates with Non-Inverted Inputs

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
XNOR2, XNOR3, XNOR4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR5	Primitive	Primitive	Primitive	Macro	Macro	Macro
XNOR6, XNOR7, XNOR8, XNOR9	Macro	Macro	Macro	Macro	Macro	Macro

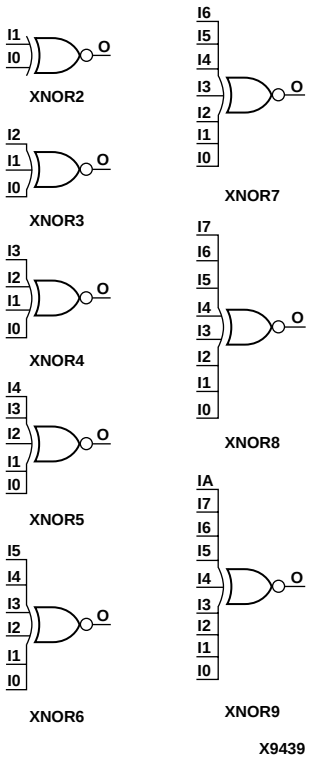


Figure 10-18 XNOR Gate Representations

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

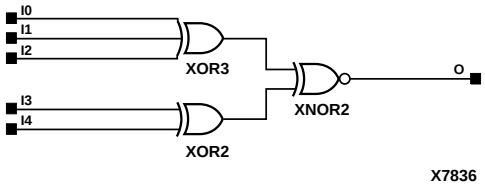


Figure 10-19 XNOR5 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

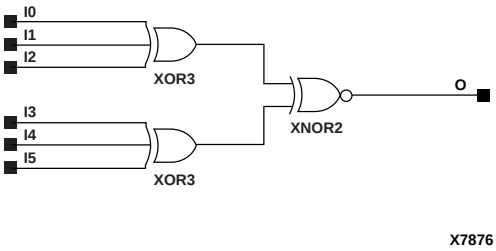


Figure 10-20 XNOR6 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

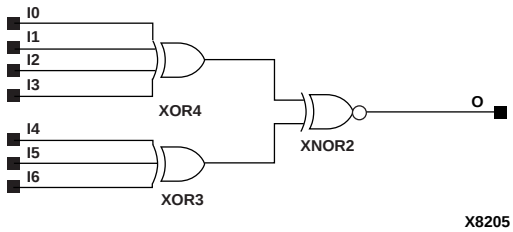


Figure 10-21 XNOR7 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

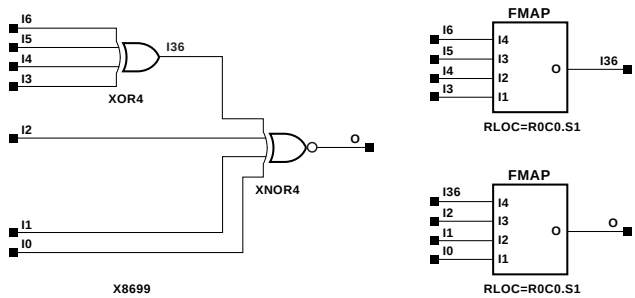


Figure 10-22 XNOR7 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

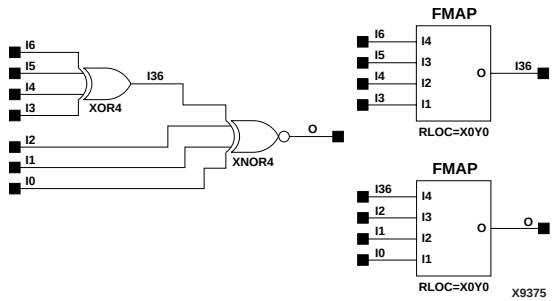


Figure 10-23 XNOR7 Implementation Virtex-II, Virtex-II PRO

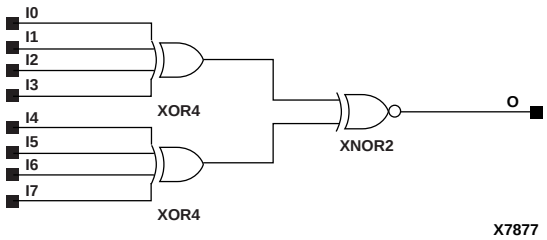


Figure 10-24 XNOR8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

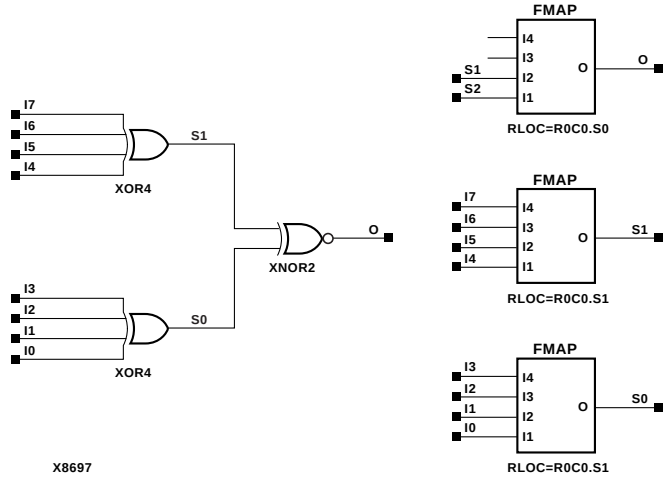


Figure 10-25 XNOR8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

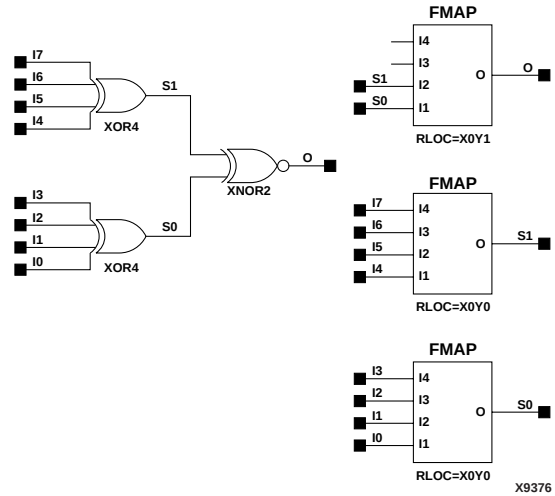


Figure 10-26 XNOR8 Implementation Virtex-II, Virtex-II PRO

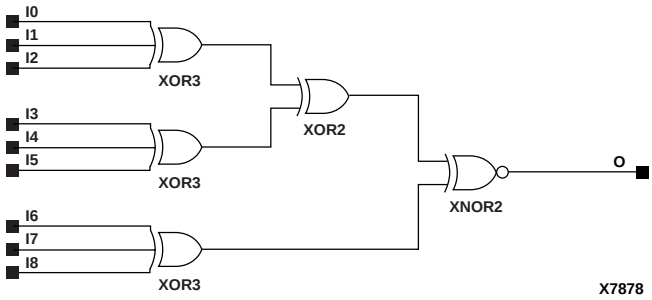


Figure 10-27 XNOR9 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

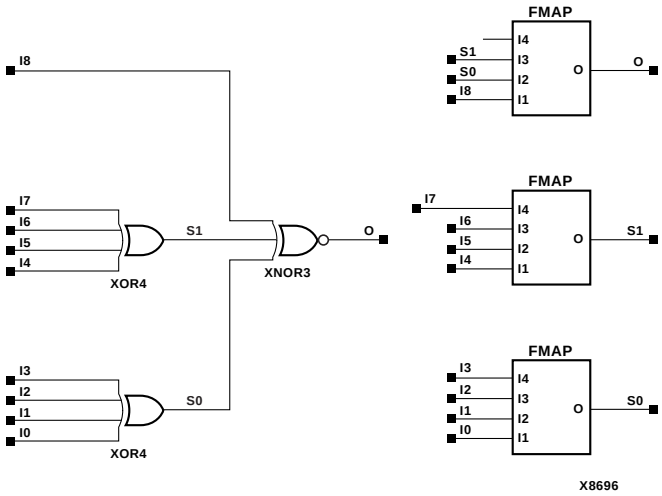


Figure 10-28 XNOR9 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

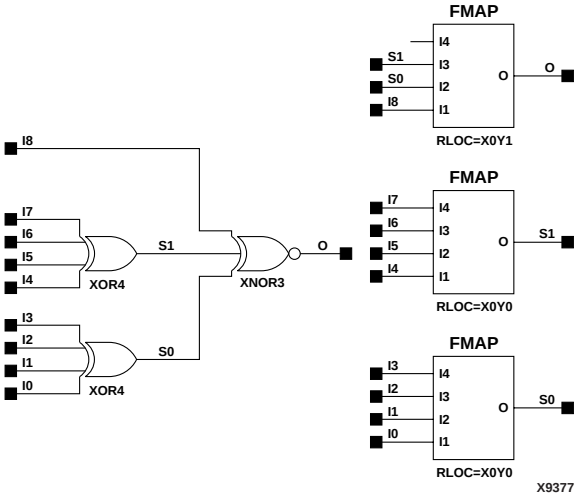


Figure 10-29 XNOR9 Implementation Virtex-II, Virtex-II PRO

XOR2-9

2- to 9-Input XOR Gates with Non-Inverted Inputs

Element	Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
XOR2, XOR3, XOR4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XOR5	Primitive	Primitive	Primitive	Macro	Macro	Macro
XOR6, XOR7, XOR8, XOR9	Macro	Macro	Macro	Macro	Macro	Macro

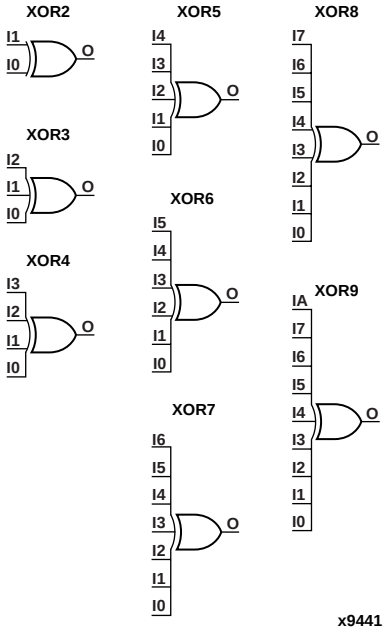


Figure 10-30 XOR Gate Representations

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

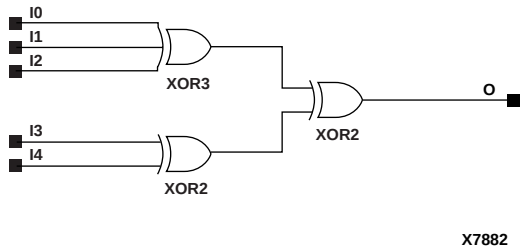


Figure 10-31 XOR5 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

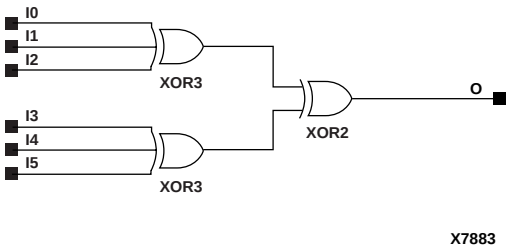


Figure 10-32 XOR6 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

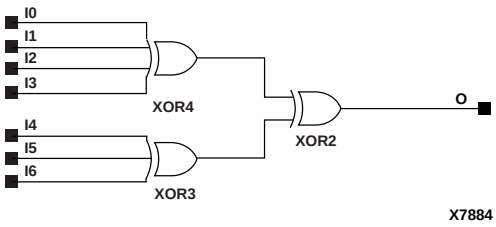


Figure 10-33 XOR7 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

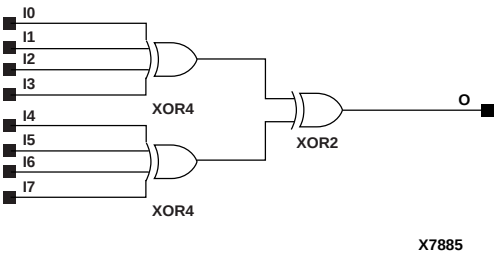


Figure 10-34 XOR8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

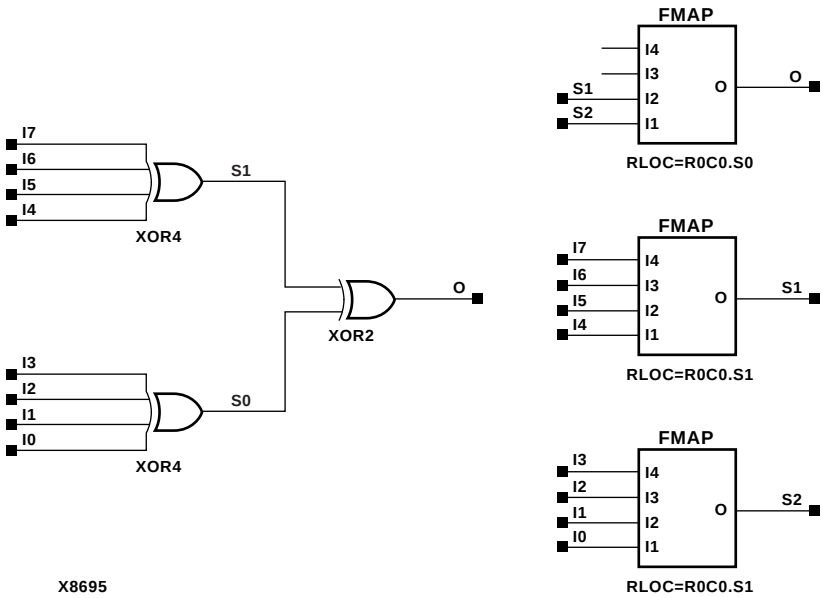


Figure 10-35 XOR8 Implementation Spartan-II, Spartan-IIE, Virtex, Virtex-E

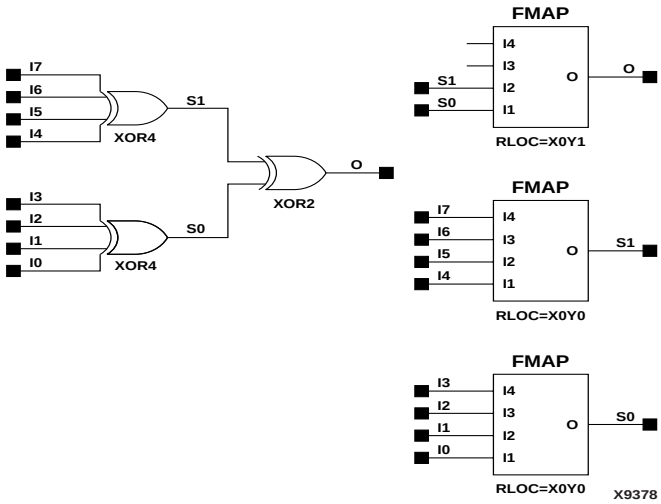


Figure 10-36 XOR8 Implementation Virtex-II, Virtex-II PRO

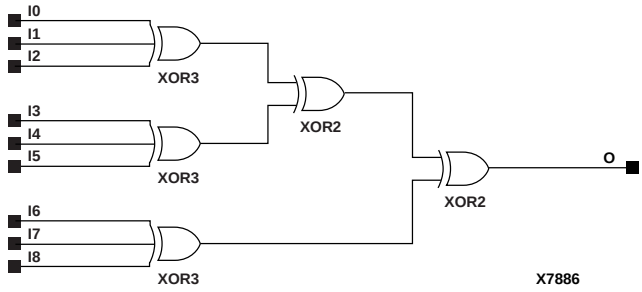
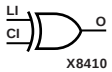


Figure 10-37 XOR9 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

XORCY

XOR for Carry Logic with General Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



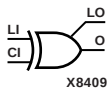
XORCY is a special XOR with general O output used for generating faster and smaller arithmetic functions.

Its O output is a general interconnect. See also “XORCY_D” and “XORCY_L.”

XORCY_D

XOR for Carry Logic with Dual Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



XORCY_D is a special XOR used for generating faster and smaller arithmetic functions.

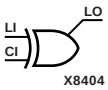
XORCY_D has two functionally identical outputs, O and LO. The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice.

See also "XORCY" and "XORCY_L."

XORCY_L

XOR for Carry Logic with Local Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
Primitive	Primitive	Primitive	N/A	N/A	N/A



XORCY_L is a special XOR with local LO output used for generating faster and smaller arithmetic functions. The LO output is used to connect to another output within the same CLB slice.

See also "XORCY" and "XORCY_D."

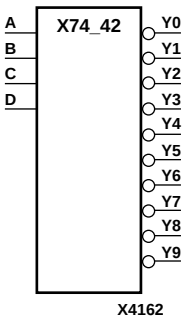
Chapter 11

X74_42 to X74_521

X74_42

4- to 10-Line BCD-to-Decimal Decoder with Active-Low Outputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_42 decodes the 4-bit BCD number on the data inputs (A – D). Only one of the ten outputs (Y9 – Y0) is active (Low) at a time, which reflects the decimal equivalent of the BCD number on inputs A – D. All outputs are inactive (High) during any one of six illegal states, as shown in the truth table.

Inputs				Outputs
D	C	B	A	Selected (Low) Output
0	0	0	0	Y0
0	0	0	1	Y1
0	0	1	0	Y2
0	0	1	1	Y3
0	1	0	0	Y4
0	1	0	1	Y5
0	1	1	0	Y6
0	1	1	1	Y7
1	0	0	0	Y8
1	0	0	1	Y9
1	0	1	0	All Outputs High
1	0	1	1	All Outputs High
1	1	0	0	All Outputs High
1	1	0	1	All Outputs High
1	1	1	0	All Outputs High
1	1	1	1	All Outputs High

Selected output is Low (0) and all others are High

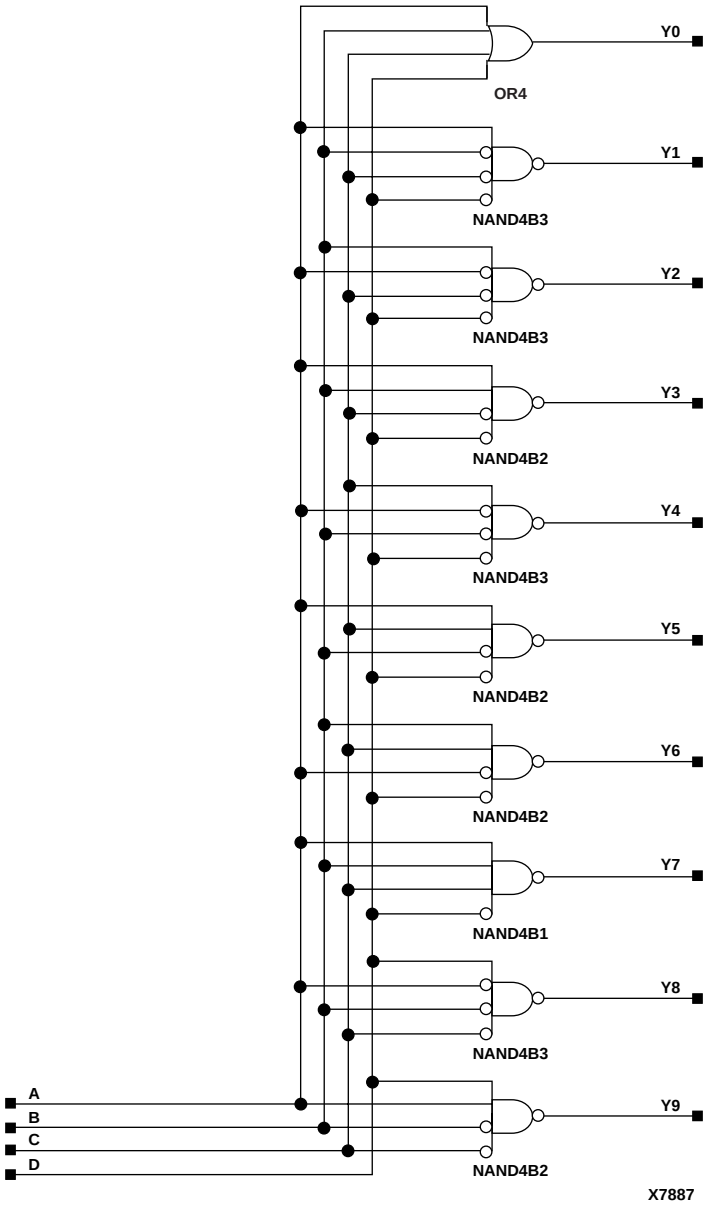
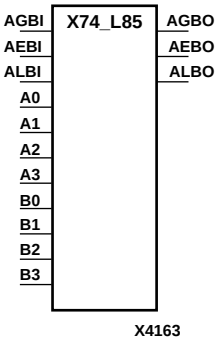


Figure 11-1 X74_42 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_L85

4-Bit Expandable Magnitude Comparator

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_L85 is a 4-bit magnitude comparator that compares two 4-bit binary-weighted words A3 – A0 and B3 – B0, where A3 and B3 are the most significant bits. The greater-than output, AGBO, is High when A>B. The less-than output, ALBO, is High when A<B, and the equal output, AEBO, is High when A=B. The expansion inputs, AGBI, ALBI, and AEBI, are the least significant bits. Words of greater length can be compared by cascading the comparators. The AGBO, ALBO, and AEBO outputs of the stage handling less-significant bits are connected to the corresponding AGBI, ALBI, and AEBI inputs of the next stage handling more-significant bits. For proper operation, the stage handling the least significant bits must have AGBI and ALBI tied Low and AEBI tied High.

Inputs							Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	AGBI	ALBI	AEBI	AGBO	ALBO	AEBO
A3>B3	X	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	0	1	0
A3=B3	A2>B2	X	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	0	1	0
A3=B3	A2=B2	A1>B1	X	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	1	0	1	1
A3=B3	A2=B2	A1=B1	A0=B0	1	0	1	1	0	1
A3=B3	A2=B2	A1=B1	A0=B0	1	1	1	1	1	1
A3=B3	A2=B2	A1=B1	A0=B0	1	1	0	1	1	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	0	0	0	0

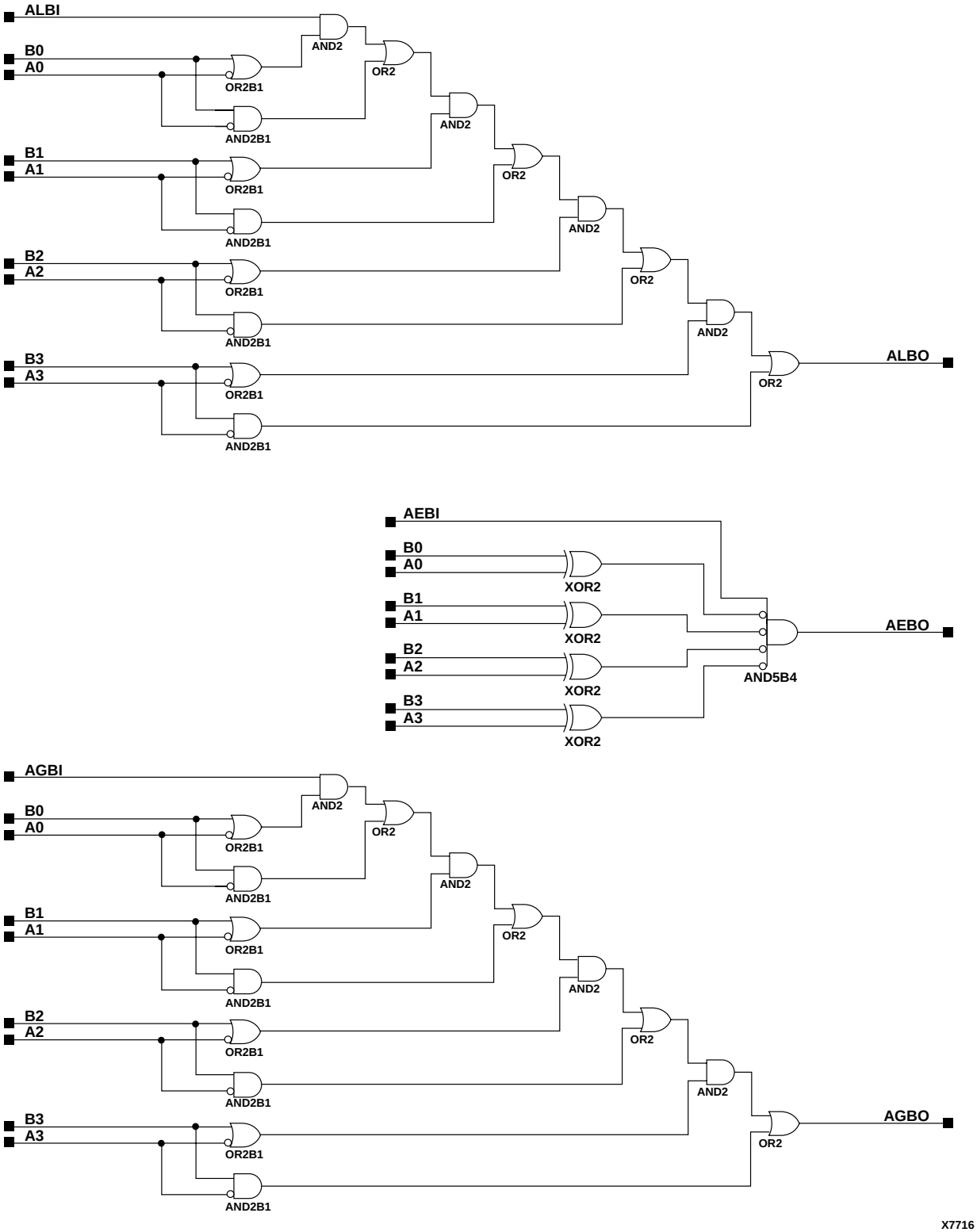
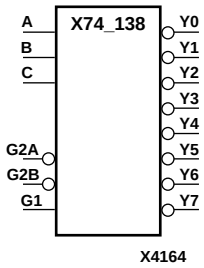


Figure 11-2 X74_L85 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_138

3- to 8-Line Decoder/Demultiplexer with Active-Low Outputs and Three Enables

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro



X74_138 is an expandable decoder/demultiplexer with one active-High enable input (G1), two active-Low enable inputs (G2A and G2B), and eight active-Low outputs (Y7 – Y0). When G1 is High and G2A and G2B are Low, one of the eight active-Low outputs is selected with a 3-bit binary address on address inputs A, B, and C. The non-selected outputs are High. When G1 is Low or when G2A or G2B is High, all outputs are High.

X74_138 can be used as an 8-output active-Low demultiplexer by tying the data input to one of the enable inputs.

Inputs						Outputs							
C	B	A	G1	G2A	G2B	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	0	0	1	0	0	1	1	1	1	1	1	1	0
0	0	1	1	0	0	1	1	1	1	1	1	0	1
0	1	0	1	0	0	1	1	1	1	1	0	1	1
0	1	1	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	0	0	1	1	0	1	1	1	1	1
1	1	0	1	0	0	1	0	1	1	1	1	1	1
1	1	1	1	0	0	0	1	1	1	1	1	1	1
X	X	X	0	X	X	1	1	1	1	1	1	1	1
X	X	X	X	1	X	1	1	1	1	1	1	1	1
X	X	X	X	X	1	1	1	1	1	1	1	1	1

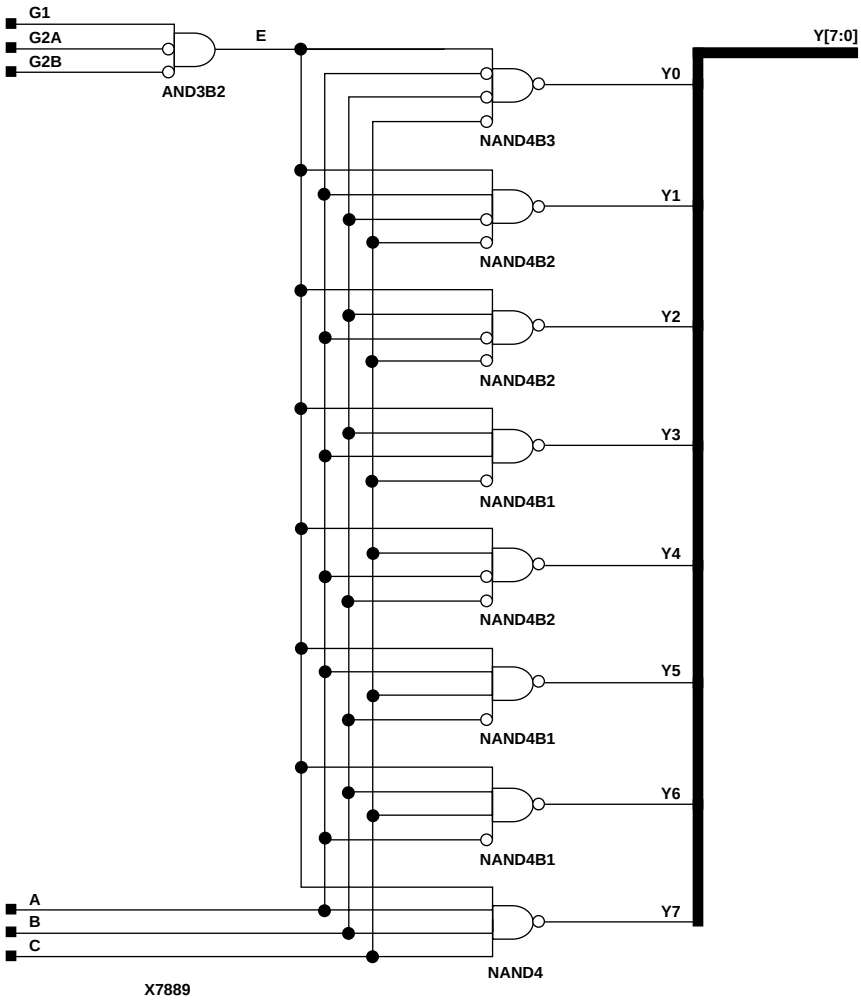
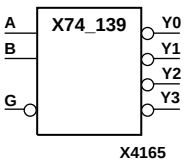


Figure 11-3 X74_138 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_139

2- to 4-Line Decoder/Demultiplexer with Active-Low Outputs and Active-Low Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_139 implements one half of a standard 74139 dual 2- to 4-line decoder / demultiplexer. When the active-Low enable input (G) is Low, one of the four active-Low outputs (Y3 – Y0) is selected with the 2-bit binary address on the A and B address input lines. B is the High-order address bit. The non-selected outputs are High. Also, when G is High all outputs are High.

X74_139 can be used as a 4-output active-Low demultiplexer by tying the data input to G.

Inputs			Outputs			
G	B	A	Y3	Y2	Y1	Y0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

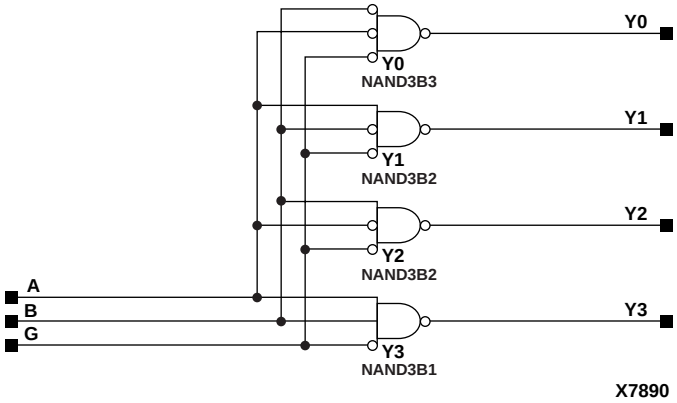
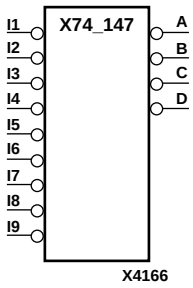


Figure 11-4 X74_139 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_147

10- to 4-Line Priority Encoder with Active-Low Inputs and Outputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_147 is a 10-line-to-BCD-priority encoder that accepts data from nine active-Low inputs (I9 – I1) and produces a binary-coded decimal (BCD) representation on the four active-Low outputs A, B, C, and D. The data inputs are weighted, so when more than one input is active, only the one with the highest priority is encoded, with I9 having the highest priority. Only nine inputs are provided, because the implied “zero” condition requires no data input. “Zero” is encoded when all data inputs are High.

Inputs									Outputs			
I9	I8	I7	I6	I5	I4	I3	I2	I1	D	C	B	A
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	0	X	1	1	0	1
1	1	1	1	1	1	0	X	X	1	1	0	0
1	1	1	1	1	0	X	X	X	1	0	1	1
1	1	1	1	0	X	X	X	X	1	0	1	0
1	1	1	0	X	X	X	X	X	1	0	0	1
1	1	0	X	X	X	X	X	X	1	0	0	0
1	0	X	X	X	X	X	X	X	0	1	1	1
0	X	X	X	X	X	X	X	X	0	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1

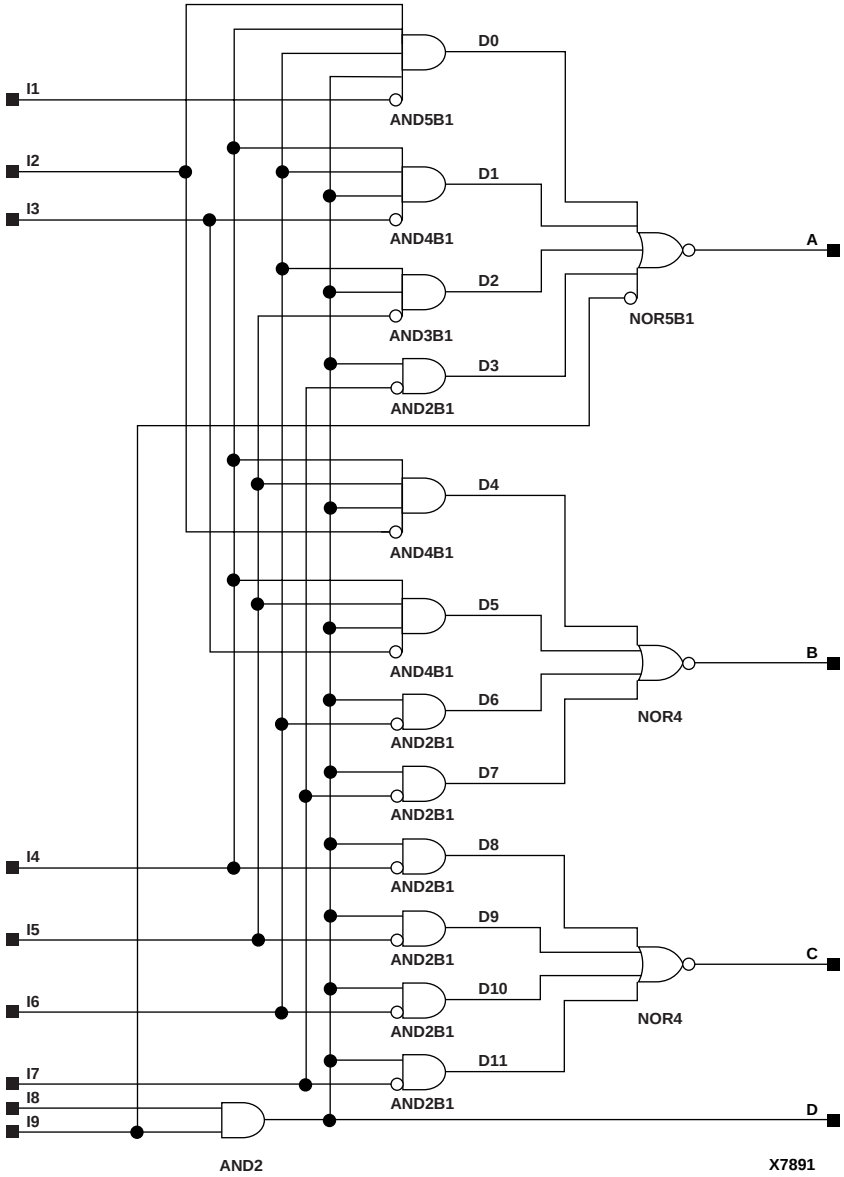
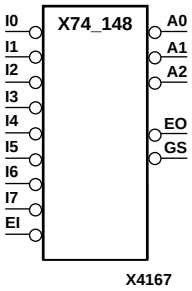


Figure 11-5 X74_147 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_148

8- to 3-Line Cascadable Priority Encoder with Active-Low Inputs and Outputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_148 8-input priority encoder accepts data from eight active-Low inputs (I7 – I0) and produces a binary representation on the three active-Low outputs (A2 – A0). The data inputs are weighted, so when more than one of the inputs is active, only the input with the highest priority is encoded, I7 having the highest priority. The active-Low group signal (GS) is Low whenever one of the data inputs is Low and the active-Low enable input (EI) is Low.

The active-Low enable input (EI) and active-Low enable output (EO) are used to cascade devices and retain priority control. The EO of the highest priority stage is connected to the EI of the next-highest priority stage. When EI is High, the data outputs and EO are High. When EI is Low, the encoder output represents the highest-priority Low data input, and the EO is High. When EI is Low and all the data inputs are High, the EO output is Low to enable the next-lower priority stage.

Inputs									Outputs				
EI	I7	I6	I5	I4	I3	I2	I1	I0	A2	A1	A0	GS	EO
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	0	1	1	1	0	1
0	1	1	1	1	1	1	0	X	1	1	0	0	1
0	1	1	1	1	1	0	X	X	1	0	1	0	1
0	1	1	1	1	0	X	X	X	1	0	0	0	1
0	1	1	1	0	X	X	X	X	0	1	1	0	1
0	1	1	0	X	X	X	X	X	0	1	0	0	1
0	1	0	X	X	X	X	X	X	0	0	1	0	1
0	0	X	X	X	X	X	X	X	0	0	0	0	1

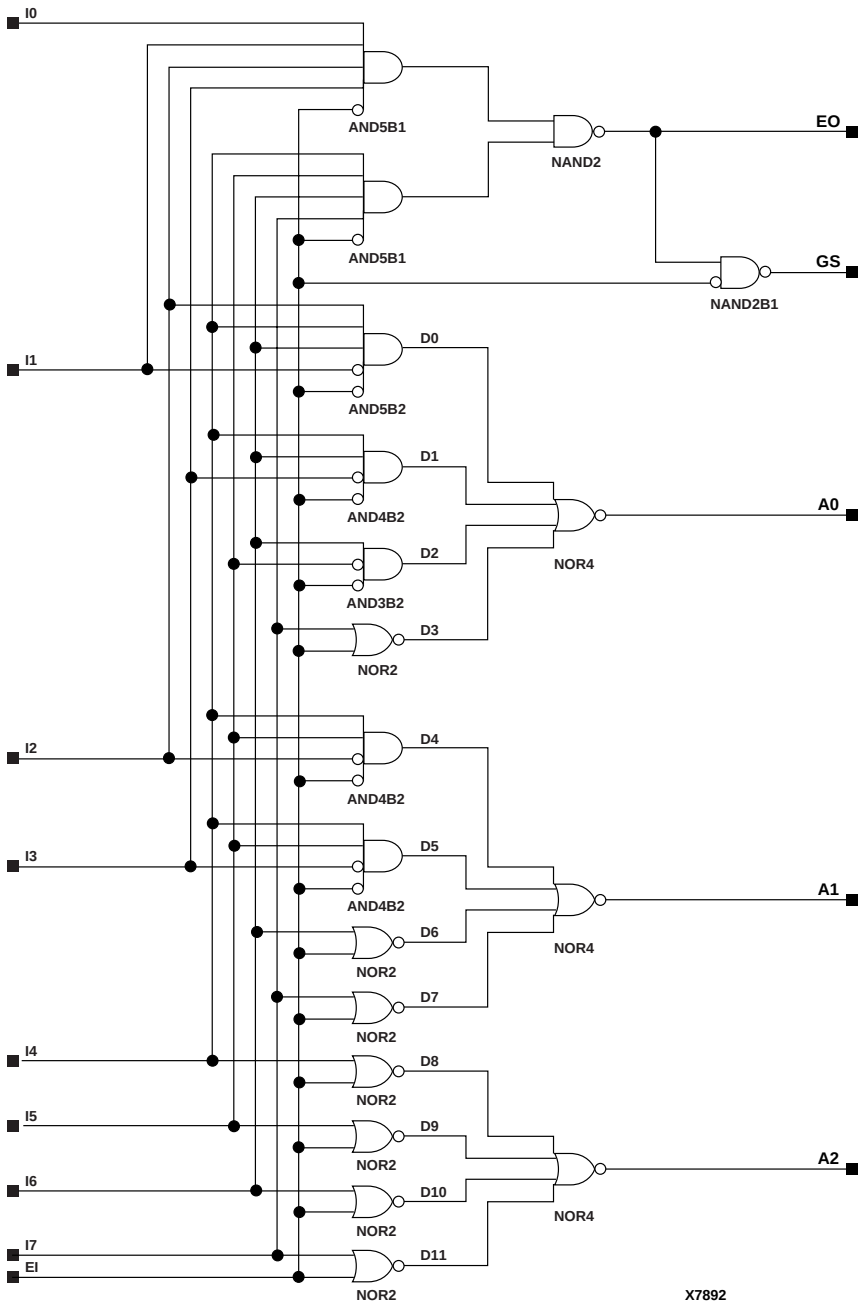
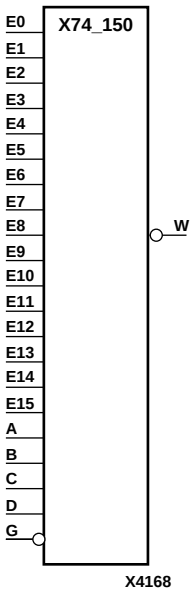


Figure 11-6 X74_148 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_150

16-to-1 Multiplexer with Active-Low Enable and Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



When the active-Low enable input (G) is Low, the X74_150 multiplexer chooses one data bit from 16 sources (E15 – E0) under the control of select inputs A, B, C, and D. The active-Low output (W) reflects the inverse of the selected input, as shown in the truth table. When the enable input (G) is High, the output (W) is High.

Inputs					Outputs
D	G	C	B	A	Selected Input Appears (Inverted) on W
1	X	X	X	X	1
0	0	0	0	0	$\overline{E0}$
0	0	0	0	1	$\overline{E1}$
0	0	0	1	0	$\overline{E2}$
0	0	0	1	1	$\overline{E3}$
0	0	1	0	0	$\overline{E4}$
0	0	1	0	1	$\overline{E5}$
0	0	1	1	0	$\overline{E6}$
0	0	1	1	1	$\overline{E7}$
0	1	0	0	0	$\overline{E8}$
0	1	0	0	1	$\overline{E9}$
0	1	0	1	0	$\overline{E10}$
0	1	0	1	1	$\overline{E11}$
0	1	1	0	0	$\overline{E12}$
0	1	1	0	1	$\overline{E13}$
0	1	1	1	0	$\overline{E14}$
0	1	1	1	1	$\overline{E15}$

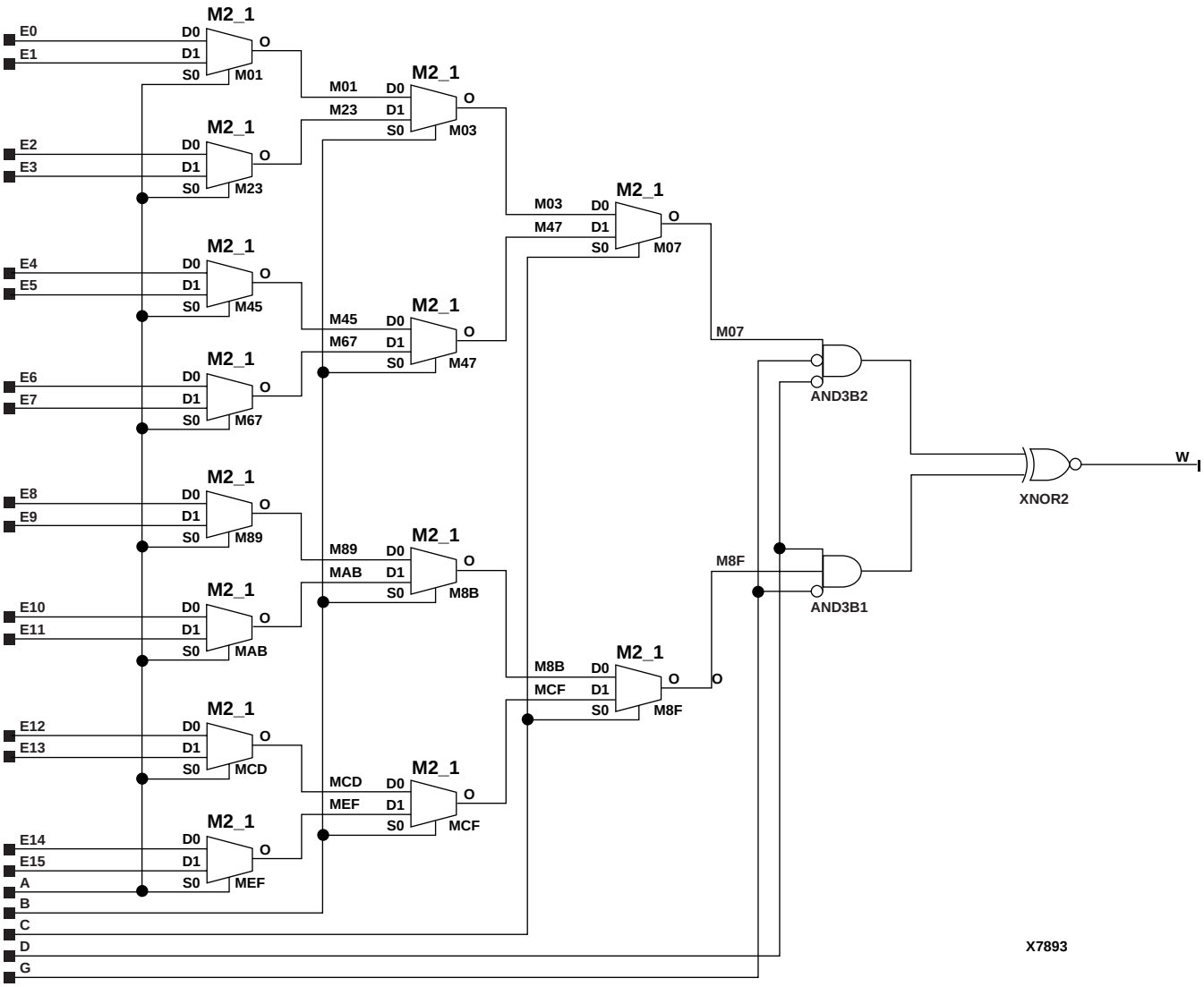
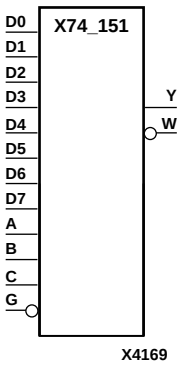


Figure 11-7 X74_150 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_151

8-to-1 Multiplexer with Active-Low Enable and Complementary Outputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



When the active-Low enable (G) is Low, the X74_151 multiplexer chooses one data bit from eight sources (D7 – D0) under control of the select inputs A, B, and C. The output (Y) reflects the state of the selected input, and the active-Low output (W) reflects the inverse of the selected input as shown in the truth table. When G is High, the Y output is Low, and the W output is High.

Inputs				Outputs	
G	C	B	A	Y	W
1	X	X	X	0	1
0	0	0	0	D0	$\overline{D0}$
0	0	0	1	D1	$\overline{D1}$
0	0	1	0	D2	$\overline{D2}$
0	0	1	1	D3	$\overline{D3}$
0	1	0	0	D4	$\overline{D4}$
0	1	0	1	D5	$\overline{D5}$
0	1	1	0	D6	$\overline{D6}$
0	1	1	1	D7	$\overline{D7}$

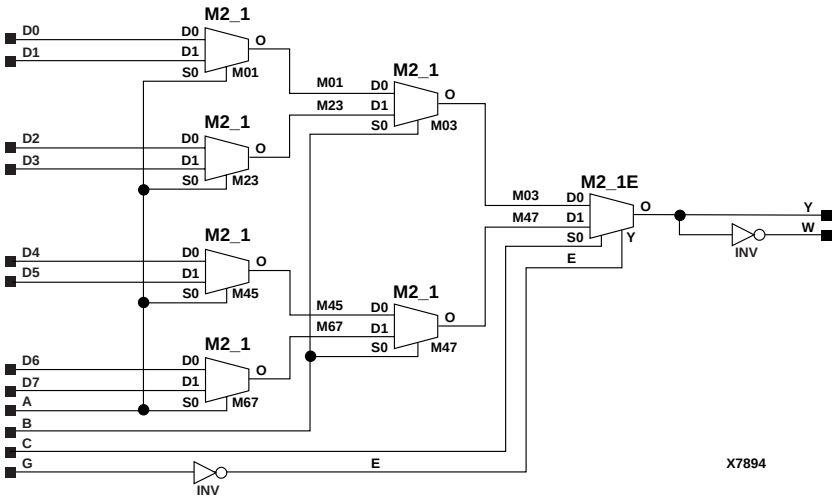
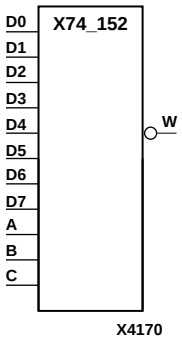


Figure 11-8 X74_151 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_152

8-to-1 Multiplexer with Active-Low Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_152 multiplexer chooses one data bit from eight sources (D7 – D0) under control of the select inputs A, B, and C. The active-Low output (W) reflects the inverse of the selected data input, as shown in the truth table.

Inputs			Outputs
C	B	A	W
0	0	0	$\overline{D0}$
0	0	1	$\overline{D1}$
0	1	0	$\overline{D2}$
0	1	1	$\overline{D3}$
1	0	0	$\overline{D4}$
1	0	1	$\overline{D5}$
1	1	0	$\overline{D6}$
1	1	1	$\overline{D7}$

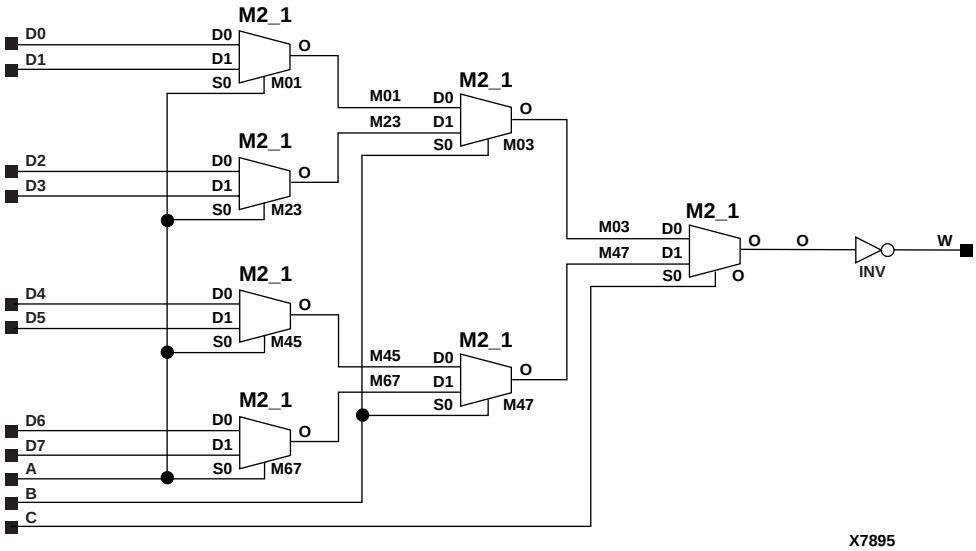
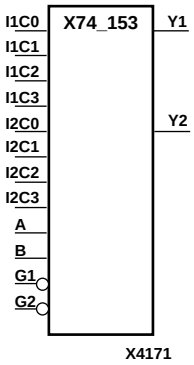


Figure 11-9 X74_152 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_153

Dual 4-to-1 Multiplexer with Active-Low Enables and Common Select Input

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



When the active-Low enable inputs G1 and G2 are Low, the data output Y1, reflects the data input chosen by select inputs A and B from data inputs I1C3 – I1C0. The data output Y2 reflects the data input chosen by select inputs A and B from data inputs I2C3 – I2C0. When G1 or G2 is High, the corresponding output, Y1 or Y2 respectively, is Low.

Inputs				Outputs	
G1	G2	B	A	Y1	Y2
1	1	X	X	0	0
1	0	0	0	0	I2C0
1	0	0	1	0	I2C1
1	0	1	0	0	I2C2
1	0	1	1	0	I2C3
0	1	0	0	I1C0	0
0	1	0	1	I1C1	0
0	1	1	0	I1C2	0
0	1	1	1	I1C3	0
0	0	0	0	I1C0	I2C0
0	0	0	1	I1C1	I2C1
0	0	1	0	I1C2	I2C2
0	0	1	1	I1C3	I2C3

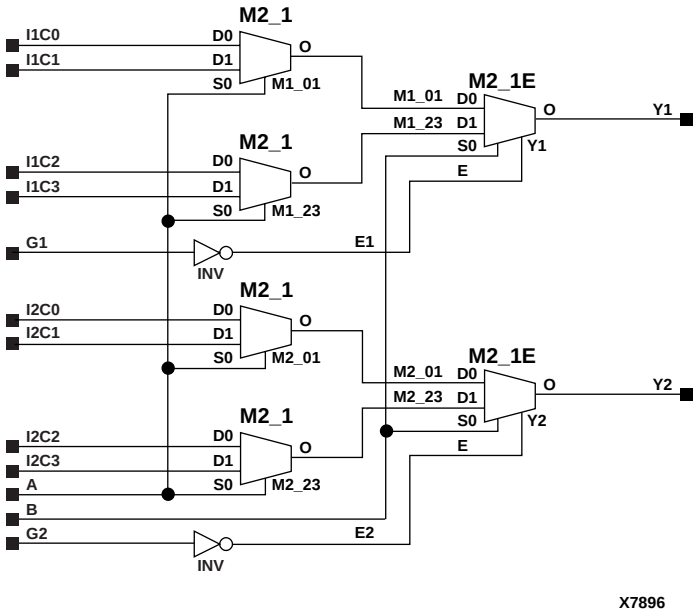
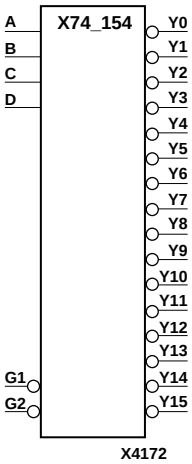


Figure 11-10 X74_153 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_154

4- to 16-Line Decoder/Demultiplexer with Two Enables and Active-Low Outputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



When the active-Low enable inputs G1 and G2 of the X74_154 decoder / demultiplexer are Low, one of 16 active-Low outputs, Y15 – Y0, is selected under the control of four binary address inputs A, B, C, and D. The non-selected inputs are High. Also, when either input G1 or G2 is High, all outputs are High.

The X74_154 can be used as a 16-to-1 demultiplexer by tying the data input to one of the G inputs and tying the other G input Low.

Inputs						Outputs							
G1	G2	D	C	B	A	Y15	Y14	Y13	Y12	Y11	Y10	Y9	... Y0
1	X	X	X	X	X	1	1	1	1	1	1	1	... 1
X	1	X	X	X	X	1	1	1	1	1	1	1	... 1
0	0	1	1	1	1	0	1	1	1	1	1	1	... 1
0	0	1	1	1	0	1	0	1	1	1	1	1	... 1
0	0	1	1	0	1	1	1	0	1	1	1	1	... 1
-	-	-	-	-	-	-	-	-	-	-	-	-	... -
-	-	-	-	-	-	-	-	-	-	-	-	-	... -
-	-	-	-	-	-	-	-	-	-	-	-	-	... -
0	0	0	0	0	0	1	1	1	1	1	1	1	... 0

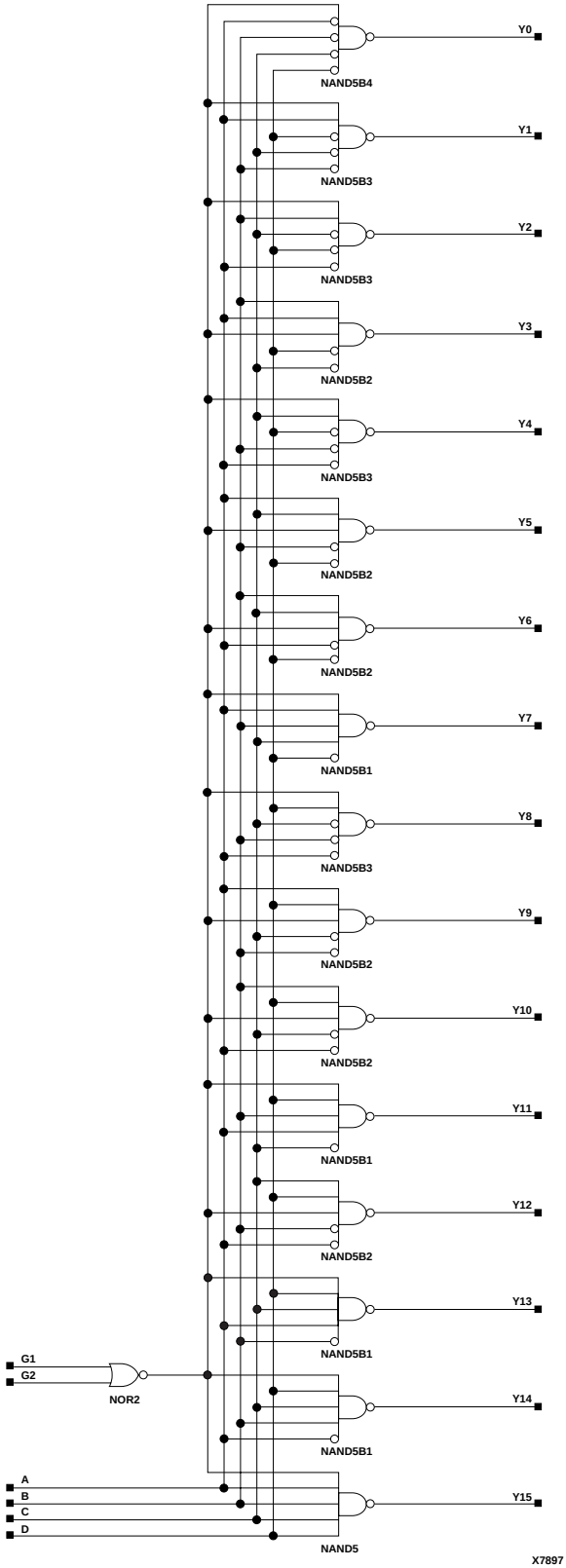
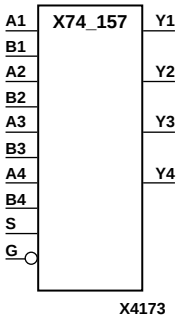


Figure 11-11 X74_154 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_157

Quadruple 2-to-1 Multiplexer with Common Select and Active-Low Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



When the active-Low enable input (G) of the X74_157 multiplexer is Low, a 4-bit word is selected from one of two sources (A3 – A0 or B3 – B0) under the control of the select input (S) and is reflected on the four outputs (Y4 – Y1). When S is Low, the outputs reflect A3 – A0; when S is High, the outputs reflect B3 – B0. When G is High, the outputs are Low.

Inputs				Outputs
G	S	B	A	Y
1	X	X	X	0
0	1	1	X	1
0	1	0	X	0
0	0	X	1	1
0	0	X	0	0

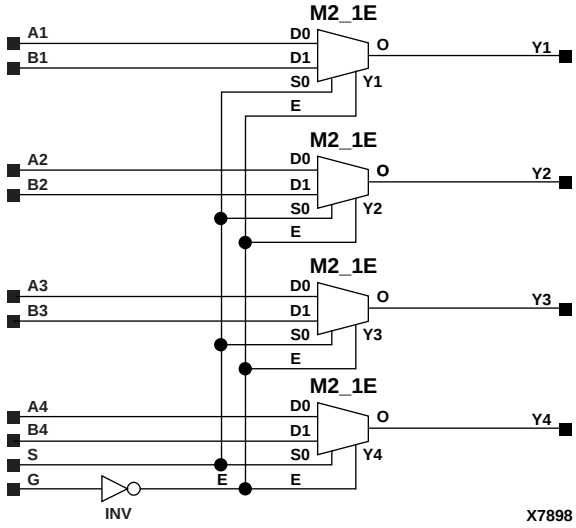
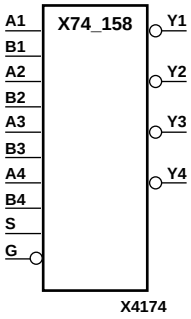


Figure 11-12 X74_157 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_158

Quadruple 2-to-1 Multiplexer with Common Select, Active-Low Enable, and Active-Low Outputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



When the active-Low enable (G) of the X74_158 multiplexer is Low, a 4-bit word is selected from one of two sources (A3 – A0 or B3 – B0) under the control of the common select input (S). The inverse of the selected word is reflected on the active-Low outputs (Y4 – Y1). When S is Low, $\overline{A3}$ – $\overline{A0}$ appear on the outputs; when S is High, $\overline{B3}$ – $\overline{B0}$ appear on the outputs. When G is High, the outputs are High.

Inputs				Outputs
G	S	B	A	Y
1	X	X	X	1
0	1	1	X	0
0	1	0	X	1
0	0	X	1	0
0	0	X	0	1

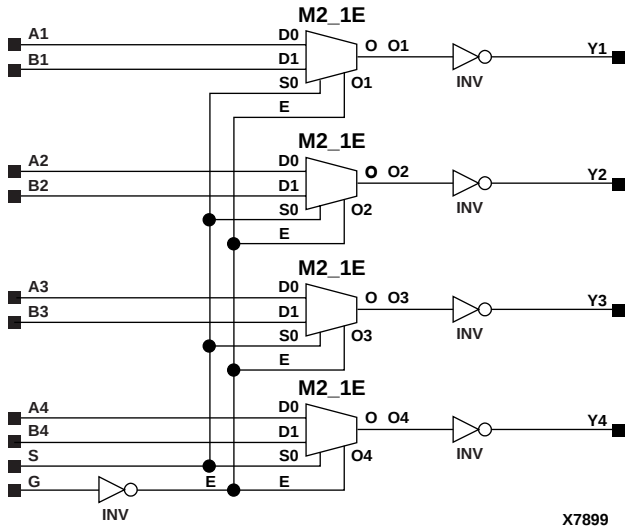
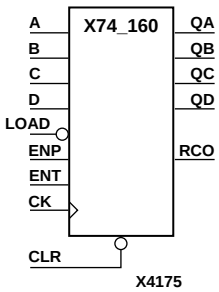


Figure 11-13 X74_158 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_160

4-Bit BCD Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_160 is a 4-stage, 4-bit, synchronous, loadable, resettable, cascadable, binary-coded decimal (BCD) counter. The active-Low asynchronous clear (CLR), when Low, overrides all other inputs and resets the data (QD, QC, QB, QA) and ripple carry-out (RCO) outputs Low. When the active-Low load enable input (LOAD) is Low and CLR is High, parallel clock enable (ENP), and trickle clock enable (ENT) are overridden and data on inputs A, B, C, and D are loaded into the counter during the Low-to-High clock transition. The data outputs (QD, QC, QB, QA) increment when ENP, ENT LOAD, and CLR are High during the Low-to-High clock transition. The counter ignores clock transitions when ENP or ENT are Low and LOAD is High. RCO is High when QD, QA, and ENT are High and QC and QB are Low.

Inputs						Outputs	
CLR	LOAD	ENP	ENT	D – A	CK	QD – QA	RCO
0	X	X	X	X	X	0	0
1	0	X	X	D – A	↑	d – a	RCO
1	1	0	X	X	X	No Chg	RCO
1	1	X	0	X	X	No Chg	0
1	1	1	1	X	↑	Inc	RCO

RCO = (QD•!QC•!QB•QA•ENT)

d – a = state of referenced input one set-up time prior to active clock transition

Carry-Lookahead Design

The carry-lookahead design allows cascading of large counters without extra gating. Both ENT and ENP must be High to count. ENT is fed forward to enable RCO, which produces a High output pulse with the approximate duration of the QA output. The following figure illustrates a carry-lookahead design.

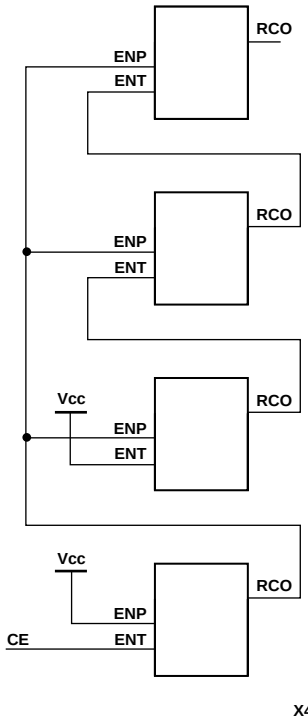


Figure 11-14 Carry-Lookahead Design

The RCO output of the first stage of the ripple carry is connected to the ENP input of the second stage and all subsequent stages. The RCO output of the second stage and all subsequent stages is connected to the ENT input of the next stage. The ENT of the second stage is always enabled / tied to VCC. CE is always connected to the ENT input of the first stage. This cascading method allows the first stage of the ripple carry to be built as a prescaler. In other words, the first stage is built to count very fast.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles.

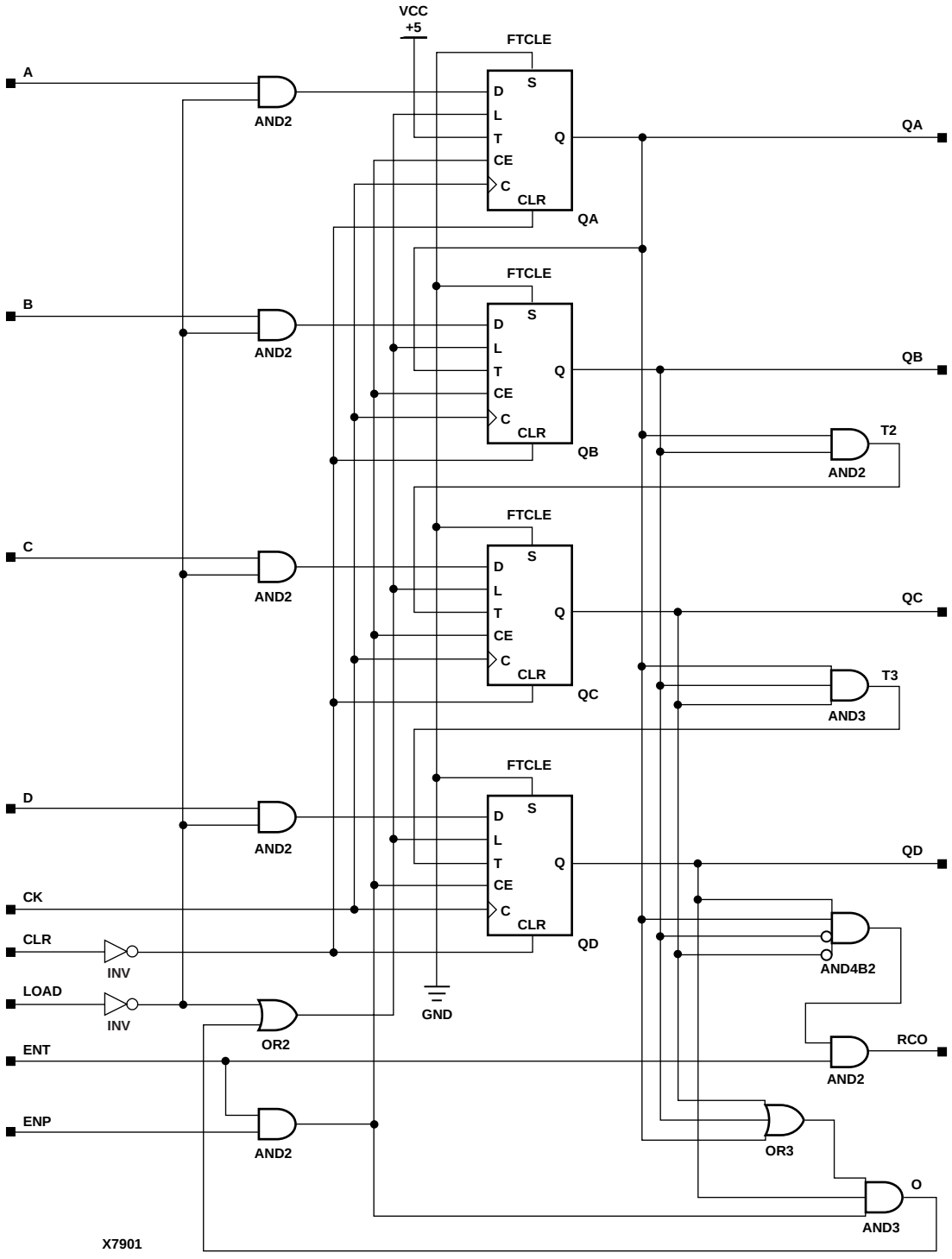
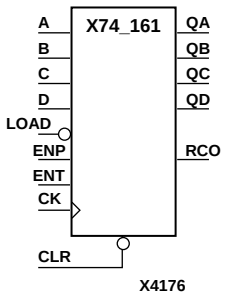


Figure 11-15 X74_160 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_161

4-Bit Binary Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_161 is a 4-stage, 4-bit, synchronous, loadable, resettable, cascadable binary counter. The active-Low asynchronous clear (CLR), when Low, overrides all other inputs and resets the data outputs (QD, QC, QB, QA) and the ripple carry-out output (RCO) Low. When the active-Low load enable (LOAD) is Low and CLR is High, parallel clock enable (ENP) and trickle clock enable (ENT) are overridden and the data on inputs A, B, C, and D is loaded into the counter during the Low-to-High clock (CK) transition. The data outputs (QD, QC, QB, QA) increment when LOAD, ENP, ENT, and CLR are High during the Low-to-High clock transition. ENP and ENT must both be High for the output to increment. RCO is High when QD – QA and ENT are High.

The carry-lookahead design accommodates large counters without extra gating. See "Carry-Lookahead Design" in the "X74_160" section for more information.

Inputs						Outputs	
CLR	LOAD	ENP	ENT	D – A	CK	QD – QA	RCO
0	X	X	X	X	X	0	0
1	0	X	X	D – A	↑	d – a	RCO
1	1	0	X	X	X	No Chg	RCO
1	1	X	0	X	X	No Chg	0
1	1	1	1	X	↑	Inc	RCO

RCO = (QD • QC • QB • QA • ENT)

d – a = state of referenced input one setup time prior to active clock transition

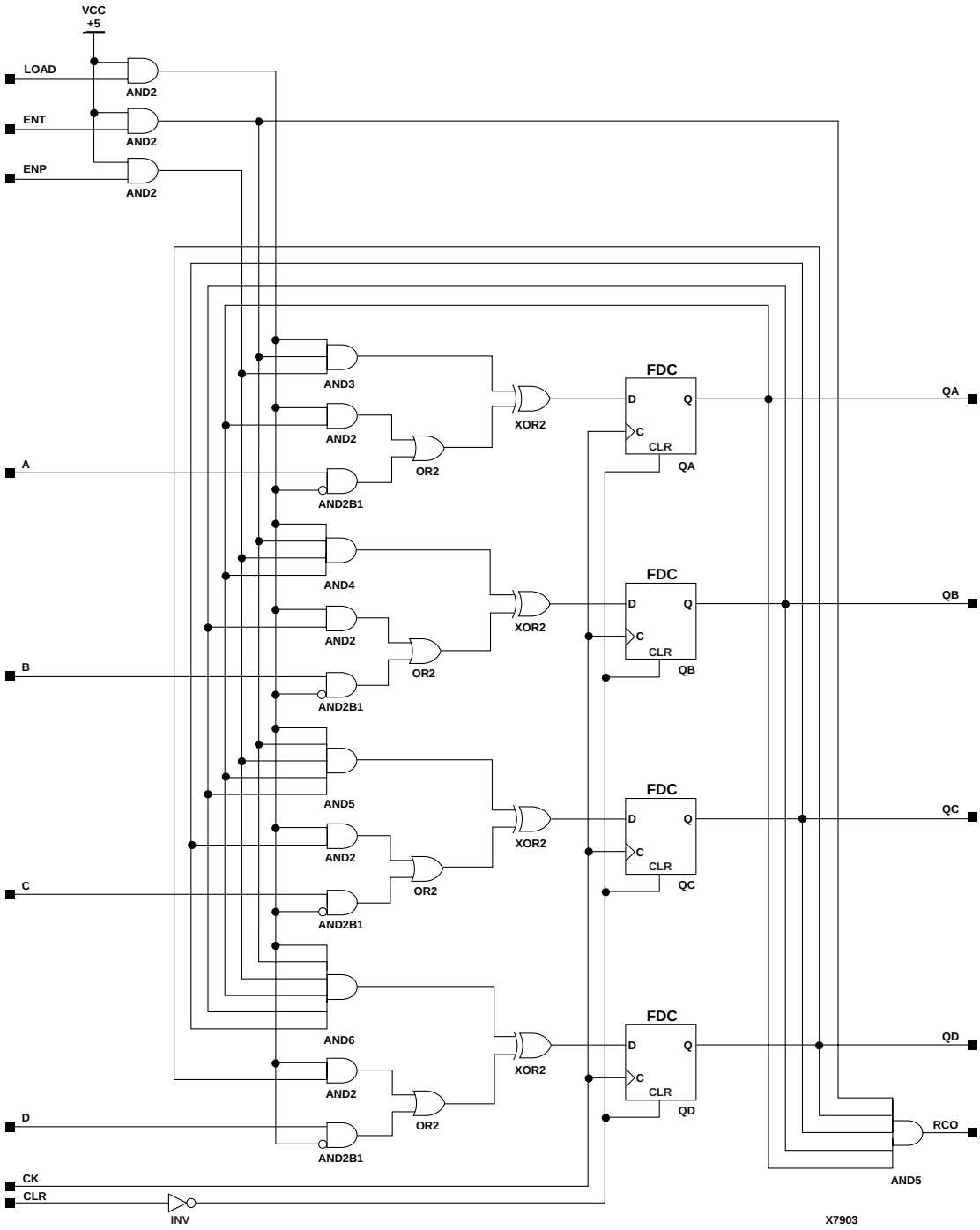
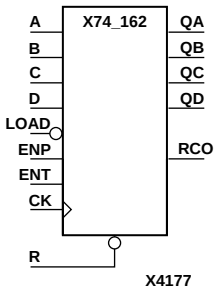


Figure 11-16 X74_161 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_162

4-Bit BCD Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_162 is a 4-stage, 4-bit, synchronous, loadable, resettable, cascadable binary-coded decimal (BCD) counter. The active-Low synchronous reset (R), when Low, overrides all other inputs and resets the data (QD, QC, QB, QA) and ripple carry-out (RCO) outputs Low during the Low-to-High clock (CK) transition. When the active-Low load enable input (LOAD) is Low and R is High, parallel clock enable (ENP) and trickle clock enable (ENT) are overridden and data on inputs A, B, C, and D is loaded into the counter during the Low-to-High clock transition. The data outputs (QD, QC, QB, QA) increment when ENP, ENT, LOAD, and R are High during the Low-to-High clock transition. ENP and ENT must both be High for the output to increment. RCO is High when QD, QA, and ENT are High and QC and QB are Low.

The carry-lookahead design accommodates cascading large counters without extra gating. See “Carry-Lookahead Design” in the “X74_160” section for more information.

Inputs						Outputs	
R	LOAD	ENP	ENT	D – A	CK	QD – QA	RCO
0	X	X	X	X	↑	0	0
1	0	X	X	D – A	↑	d – a	RCO
1	1	0	X	X	X	No Chg	RCO
1	1	X	0	X	X	No Chg	0
1	1	1	1	X	↑	Inc	RCO

RCO = (QD•!QC•!QB•QA•ENT)

d – a = state of referenced input one setup time prior to active clock transition

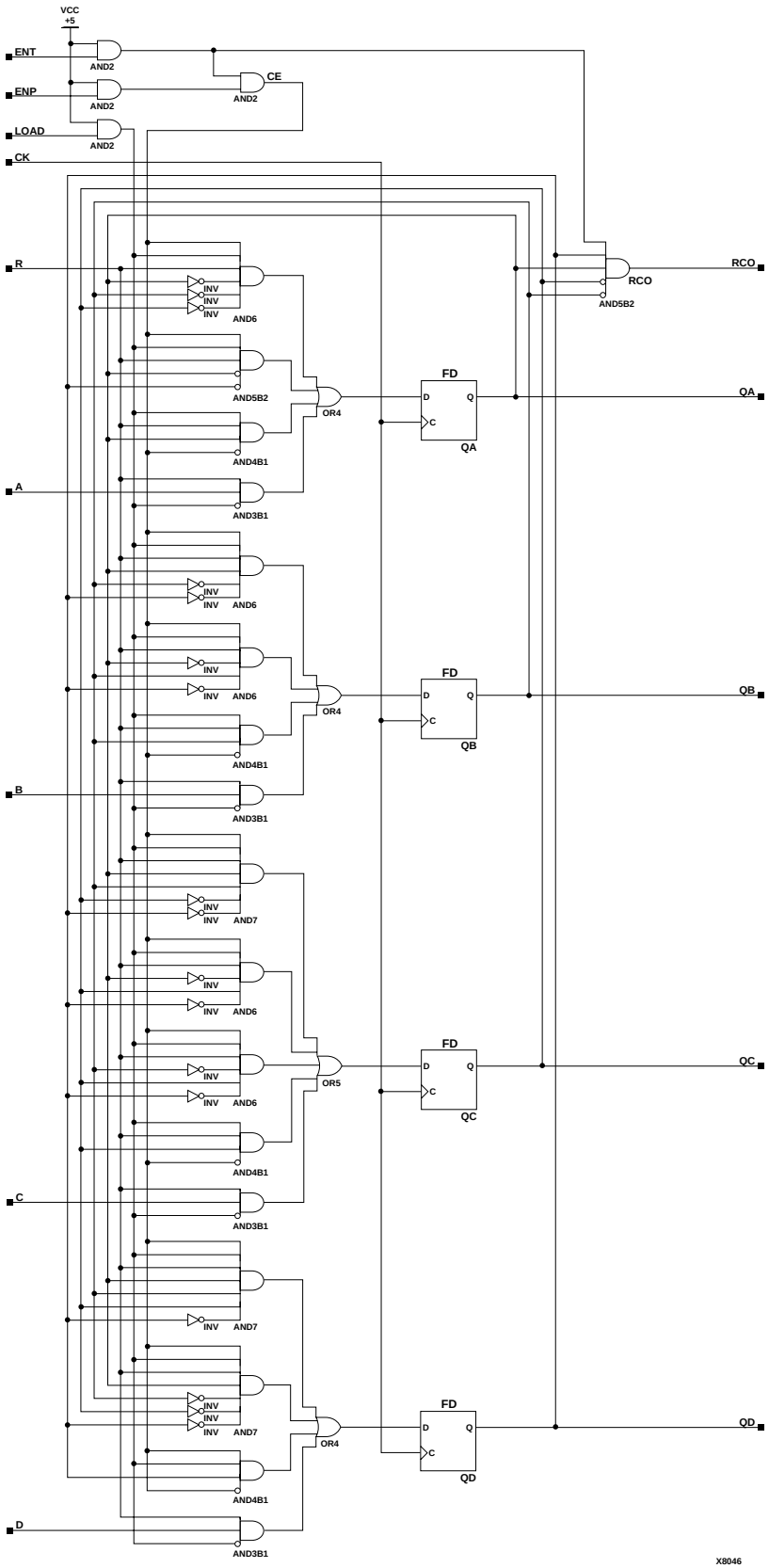
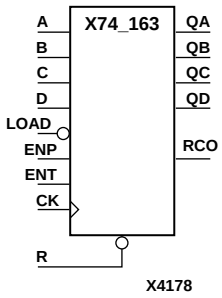


Figure 11-17 X74_162 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_163

4-Bit Binary Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Synchronous Reset

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_163 is a 4-stage, 4-bit, synchronous, loadable, resettable, cascadable binary counter. The active-Low synchronous reset (R), when Low, overrides all other inputs and resets the data outputs (QD, QC, QB, QA) and the ripple carry-out output (RCO) Low during the Low-to-High clock (CK) transition. When the active-Low load enable (LOAD) is Low and R is High, parallel clock enable (ENP) and trickle clock enable (ENT) are overridden and the data on inputs (A, B, C, D) is loaded into the counter during the Low-to-High clock (CK) transition. The outputs (QD, QC, QB, QA) increment when LOAD, ENP, ENT, and R are High during the Low-to-High clock transition. ENP and ENT must both be High for the output to increment; RCO is High when QD – QA and ENT are High.

The carry-lookahead design accommodates large counters without extra gating. See "Carry-Lookahead Design" in the "X74_160" section for more information.

Inputs						Outputs	
R	LOAD	ENP	ENT	D – A	CK	QD – QA	RCO
0	X	X	X	X	↑	0	0
1	0	X	X	D – A	↑	d – a	RCO
1	1	0	X	X	X	No Chg	RCO
1	1	X	0	X	X	No Chg	0
1	1	1	1	X	↑	Inc	RCO

RCO = (QD • QC • QB • QA • ENT)

d – a = state of referenced input one setup time prior to active clock transition

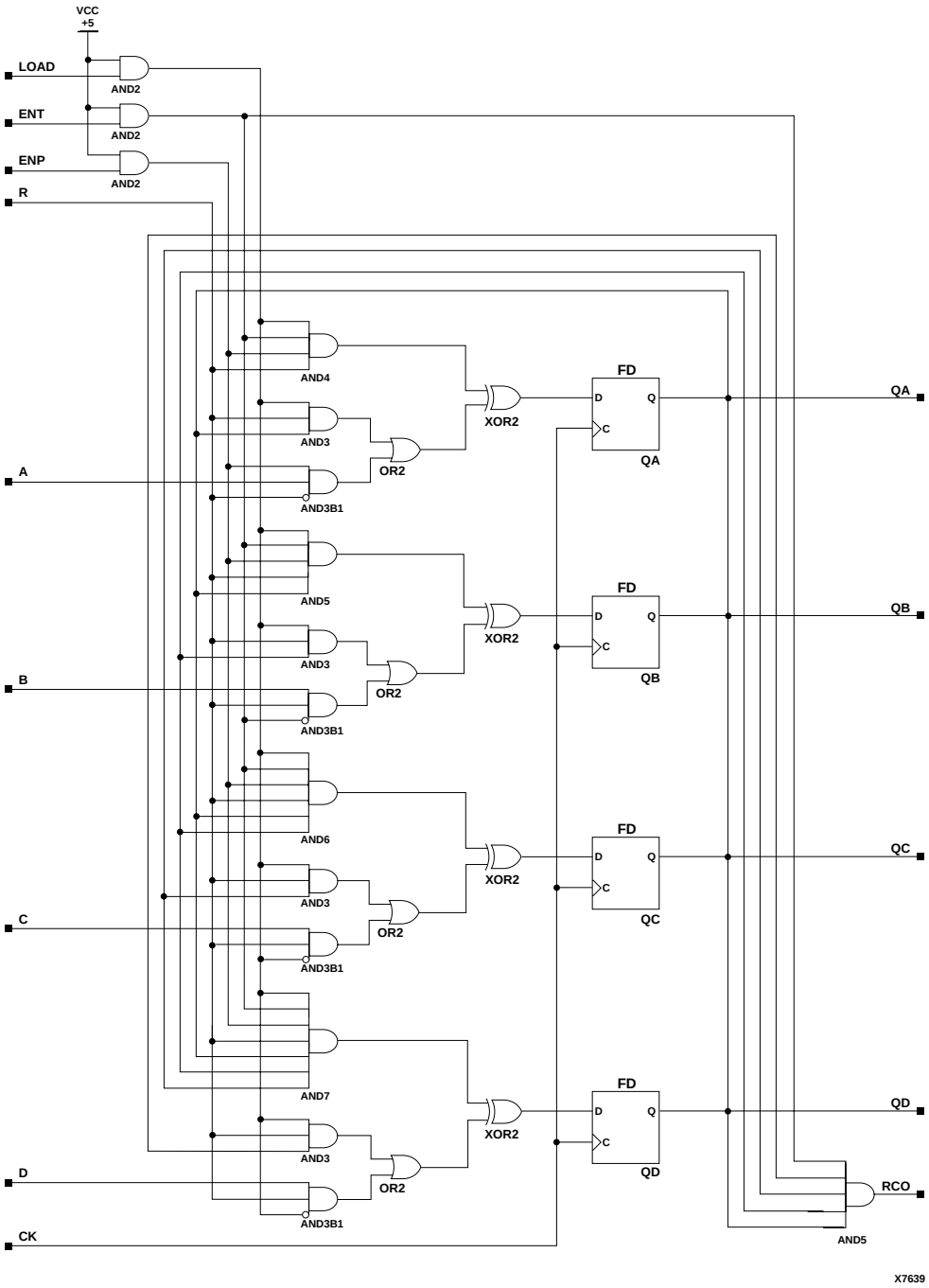
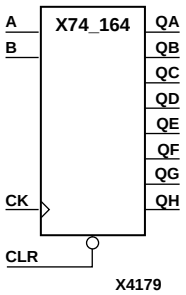


Figure 11-18 X74_163 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_164

8-Bit Serial-In Parallel-Out Shift Register with Active-Low Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_164 is an 8-bit, serial input (A and B), parallel output (QH – QA) shift register with an active-Low asynchronous clear (CLR) input. The asynchronous CLR, when Low, overrides the clock input and sets the data outputs (QH – QA) Low. When CLR is High, the AND function of the two data inputs (A and B) is loaded into the first bit of the shift register during the Low-to-High clock (CK) transition and appears on the QA output. During subsequent Low-to-High clock transitions, with CLR High, the data is shifted to the next-highest bit position as new data is loaded into QA (A and B→QA, QA→QB, QB→QC, and so forth).

Registers can be cascaded by connecting the QH output of one stage to the A input of the next stage, by tying B High, and by connecting the clock and CLR inputs in parallel.

Inputs				Outputs	
CLR	A	B	CK	QA	QB – QH
0	X	X	X	0	0
1	1	1	↑	1	qA – qG
1	0	X	↑	0	qA – qG
1	X	0	↑	0	qA – qG

qA – qG = state of referenced output one setup time prior to active clock transition

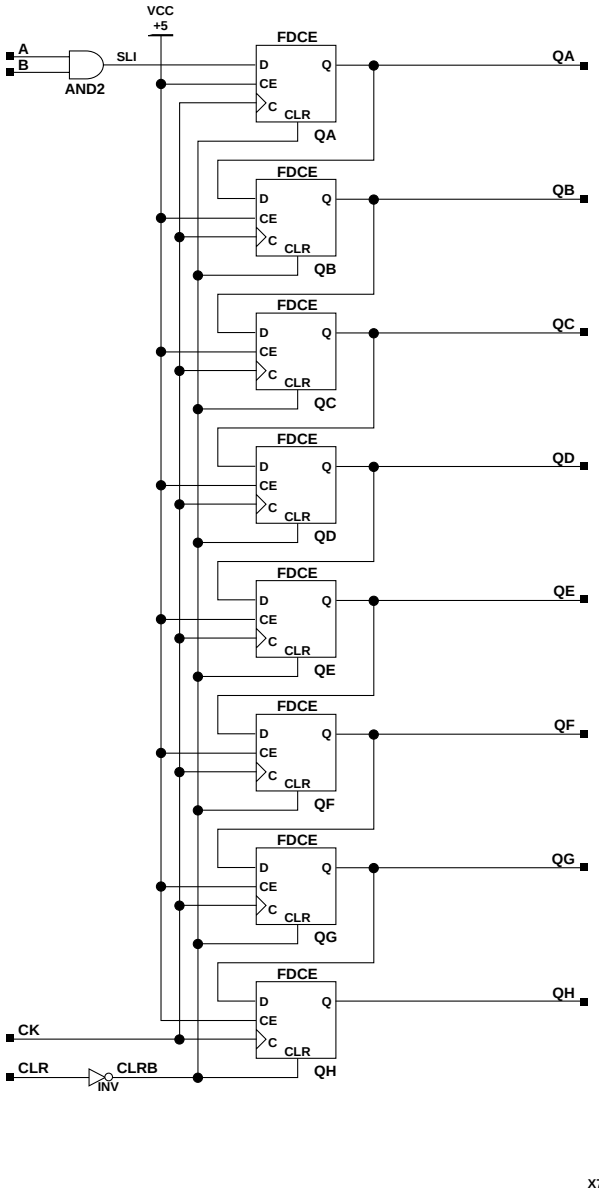
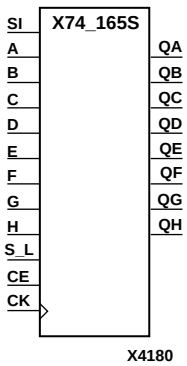


Figure 11-19 X74_164 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_165S

8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_165S is an 8-bit shift register with serial-input (SI), parallel- inputs (H – A), parallel-outputs (QH – QA), and two control inputs – clock enable (CE) and active-Low shift / load enable (S_L). When S_L is Low, data on the H – A inputs is loaded into the corresponding QH – QA bits of the register on the Low-to-High clock (CK) transition. When CE and S_L are High, data on the SI input is loaded into the first bit of the register during the Low-to-High clock transition. During subsequent Low-to-High clock transitions, with CE and S_L High, the data is shifted to the next-highest bit position (shift right) as new data is loaded into QA (SI→ QA, QA→QB, QB→QC, and so forth). The register ignores clock transitions when CE is Low and S_L is High.

Registers can be cascaded by connecting the QH output of one stage to the SI input of the next stage and connecting clock, CE, and S_L inputs in parallel.

Inputs					Outputs	
S_L	CE	SI	A – H	CK	QA	QB – QH
0	X	X	A – H	↑	qa	qb – qh
1	0	X	X	X	No Chg	No Chg
1	1	SI	X	↑	si	qA – qG

si = state of referenced input one setup time prior to active clock transition

qn = state of referenced output one setup time prior to active clock transition

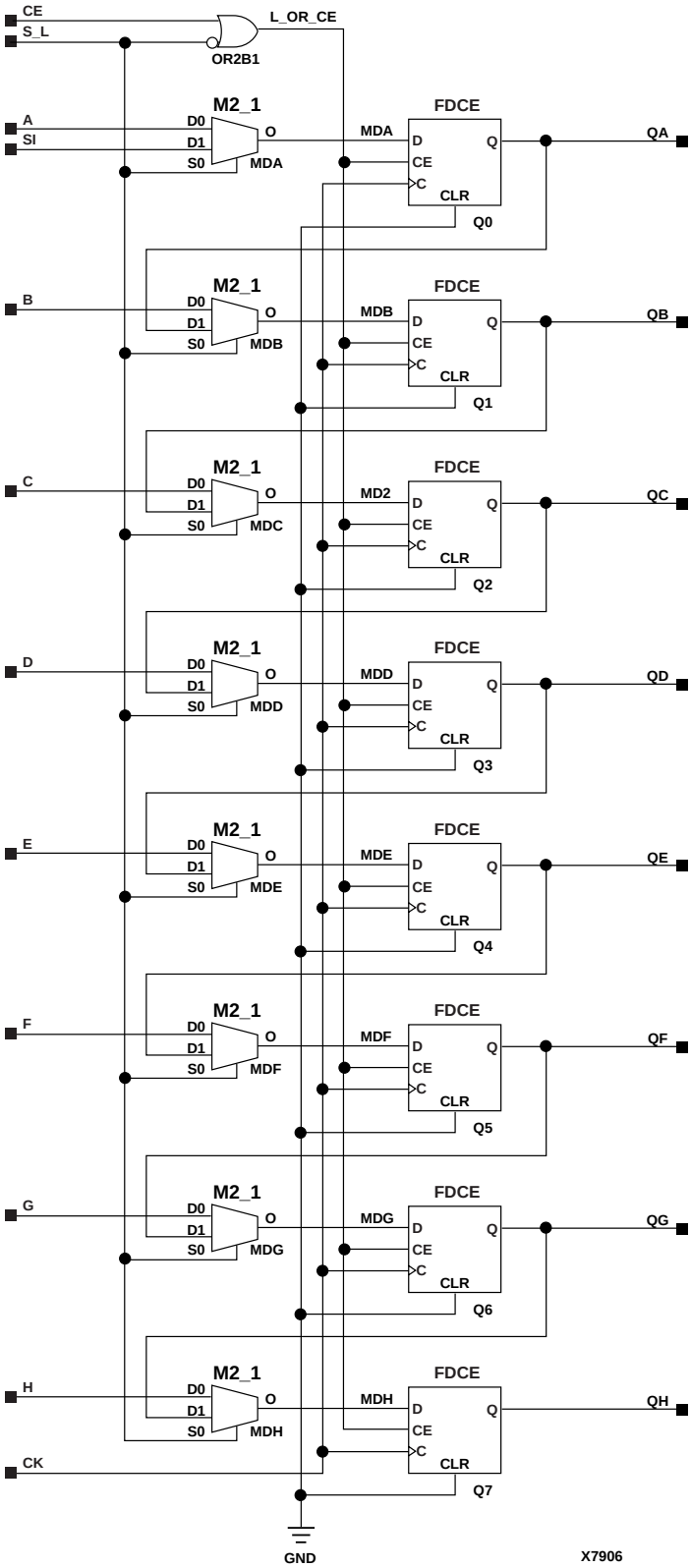
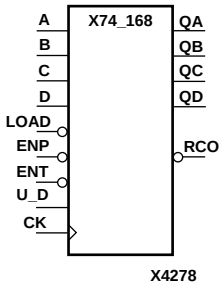


Figure 11-20 X74_165S Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_168

4-Bit BCD Bidirectional Counter with Parallel and Trickle Clock Enables and Active-Low Load Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_168 is a 4-stage, 4-bit, synchronous, loadable, cascadable, bidirectional binary-coded-decimal (BCD) counter. The data on the D – A inputs is loaded into the counter when the active-Low load enable (LOAD) is Low during the Low-to-High clock (CK) transition. The LOAD input, when Low, has priority over parallel clock enable (ENP), trickle clock enable (ENT), and the bidirectional (U_D) control. The outputs (QD – QA) increment when U_D and LOAD are High and ENP and ENT are Low during the Low-to-High clock transition. The outputs decrement when LOAD is High and ENP, ENT, and U_D are Low during the Low-to-High clock transition. The counter ignores clock transitions when LOAD and either ENP or ENT are High.

The active-Low ripple carry-out output (RCO) is Low when QD, QA, and U_D are High and QC, QB, and ENT are Low. RCO is also Low when all outputs, ENT and U_D are Low. The following figure illustrates a carry-lookahead design.

Inputs						Outputs	
LOAD	ENP	ENT	U_D	A – D	CK	QA – QD	RCO
0	X	X	X	A – D	↑	qa – qd	RCO
1	0	0	1	X	↑	Inc	RCO
1	0	0	0	X	↑	Dec	RCO
1	1	0	X	X	X	No Chg	RCO
1	X	1	X	X	X	No Chg	1

RCO = (Q3•!Q2•!Q1•Q0•U_D•!ENT) + (!Q3•!Q2•!Q1•!Q0•!U_D•!ENT)

qa – qd = state of referenced input one setup time prior to active clock transition

The active-Low ripple carry-out output (RCO) is Low when QD, QA, and U_D are High and QC, QB, and ENT are Low. RCO is also Low when all outputs, ENT and U_D are Low. The following figure illustrates a carry-lookahead design.

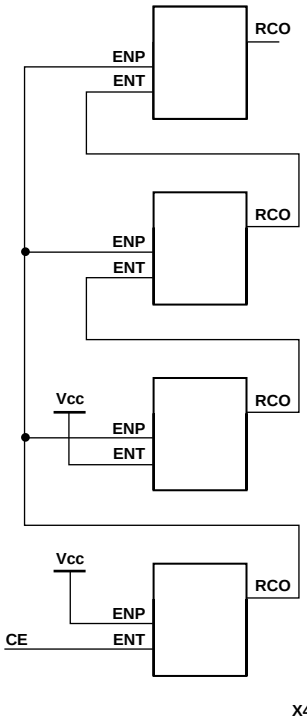


Figure 11-21 Carry-Lookahead Design

The RCO output of the first stage of the ripple carry is connected to the ENP input of the second stage and all subsequent stages. The RCO output of second stage and all subsequent stages is connected to the ENT input of the next stage. The ENT of the second stage is always enabled / tied to VCC. CE is always connected to the ENT input of the first stage. This cascading method allows the first stage of the ripple carry to be built as a prescaler. In other words, the first stage is built to count very fast.

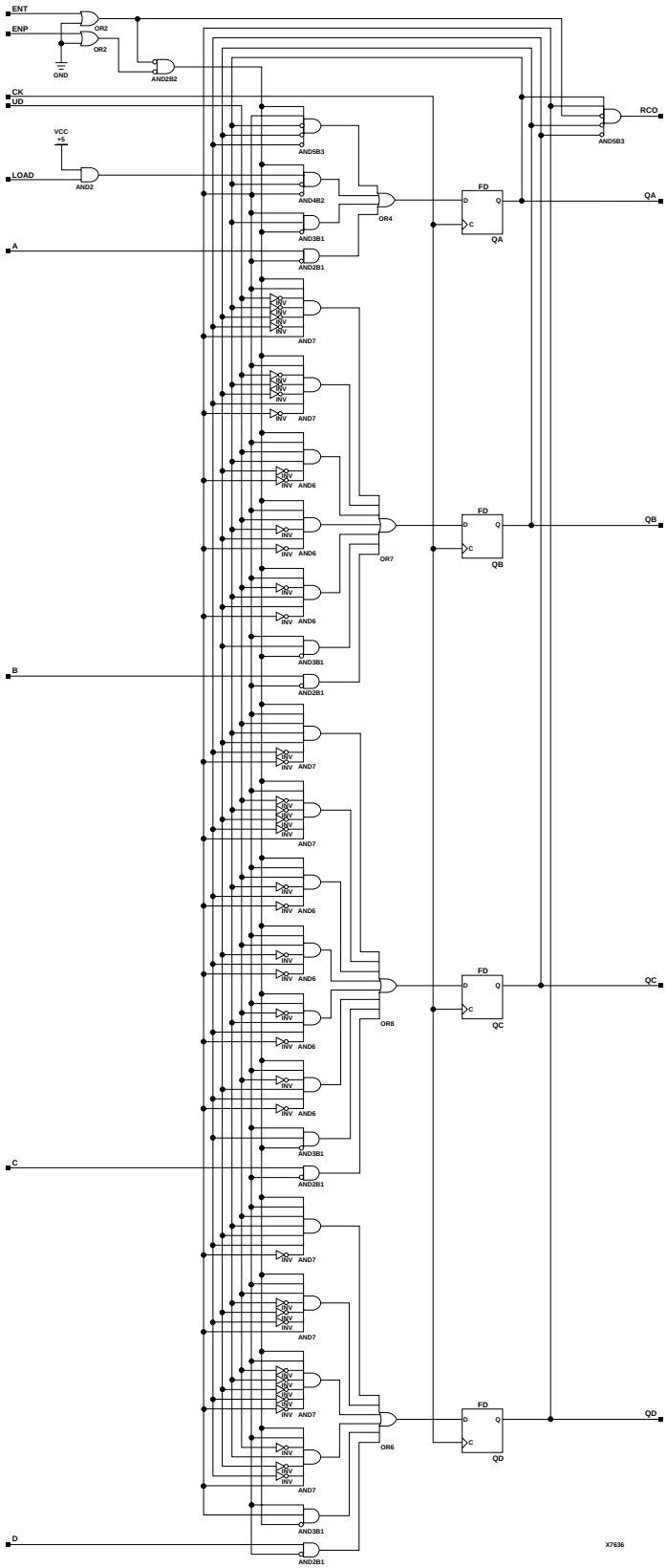
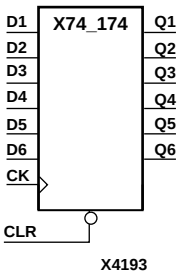


Figure 11-22 X74_168 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_174

6-Bit Data Register with Active-Low Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



The active-Low asynchronous clear input (CLR), when Low, overrides the clock and resets the six data outputs (Q6 – Q1) Low. When CLR is High, the data on the six data inputs (D6 – D1) is transferred to the corresponding data outputs on the Low-to-High clock (CK) transition.

Inputs			Outputs
CLR	D6 – D1	CK	Q6 – Q1
0	X	X	0
1	D6 – D1	↑	d6 – d1

dn = state of referenced input one setup time prior to active clock transition

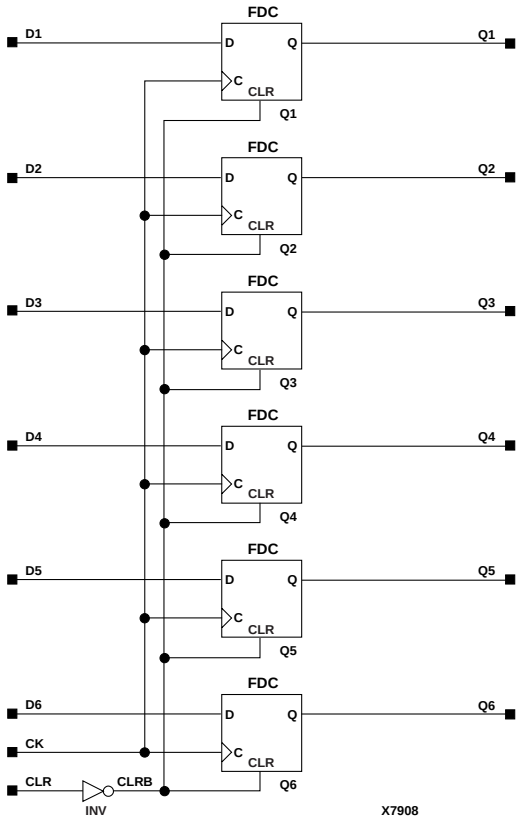
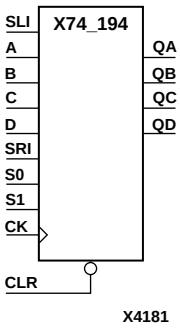


Figure 11-23 X74_174 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_194

4-Bit Loadable Bidirectional Serial/Parallel-In Parallel-Out Shift Register

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_194 is a 4-bit shift register with shift-right serial input (SRI), shift-left serial input (SLI), parallel inputs (D – A), parallel outputs (QD – QA), two control inputs (S1, S0), and active-Low asynchronous clear (CLR). The shift register performs the following functions.

Clear	When CLR is Low, all other inputs are ignore and outputs QD – QA go to logic state zero.
Load	When S1 and S0 are High, the data on inputs D –A is loaded into the corresponding output bits QD –QA during the Low-to-High clock (CK) transition.
Shift Right	When S1 is Low and S0 is High, the data is to the next-highest bit position (right) as new data is loaded into QA(SRI→QA,QA→QB, QB→QC, and so forth).
Shift Left	When S1 is High and S0 is Low, the data is shifted to the next-lowest bit position (left) as new data is loaded into QD (SLI→QD,QD→QC,QC→QB, and so forth).

Registers can be cascaded by connecting the QD output of one stage to the SRI input of the next stage, the QA output of one stage to the SLI input of the next stage, and connecting clock, S1, S0, and CLR inputs in parallel.

Inputs							Outputs			
CLR	S1	S0	SRI	SLI	A – D	CK	QA	QB	QC	QD
0	X	X	X	X	X	X	0	0	0	0
1	0	0	X	X	X	X	No Chg	No Chg	No Chg	No Chg
1	1	1	X	X	A – D	↑	a	b	c	d
1	0	1	SRI	X	X	↑	sri	qa	qb	qc
1	1	0	X	SLI	X	↑	qb	qc	qd	sli

Lowercase letters represent state of referenced input or output one setup time prior to active clock transition

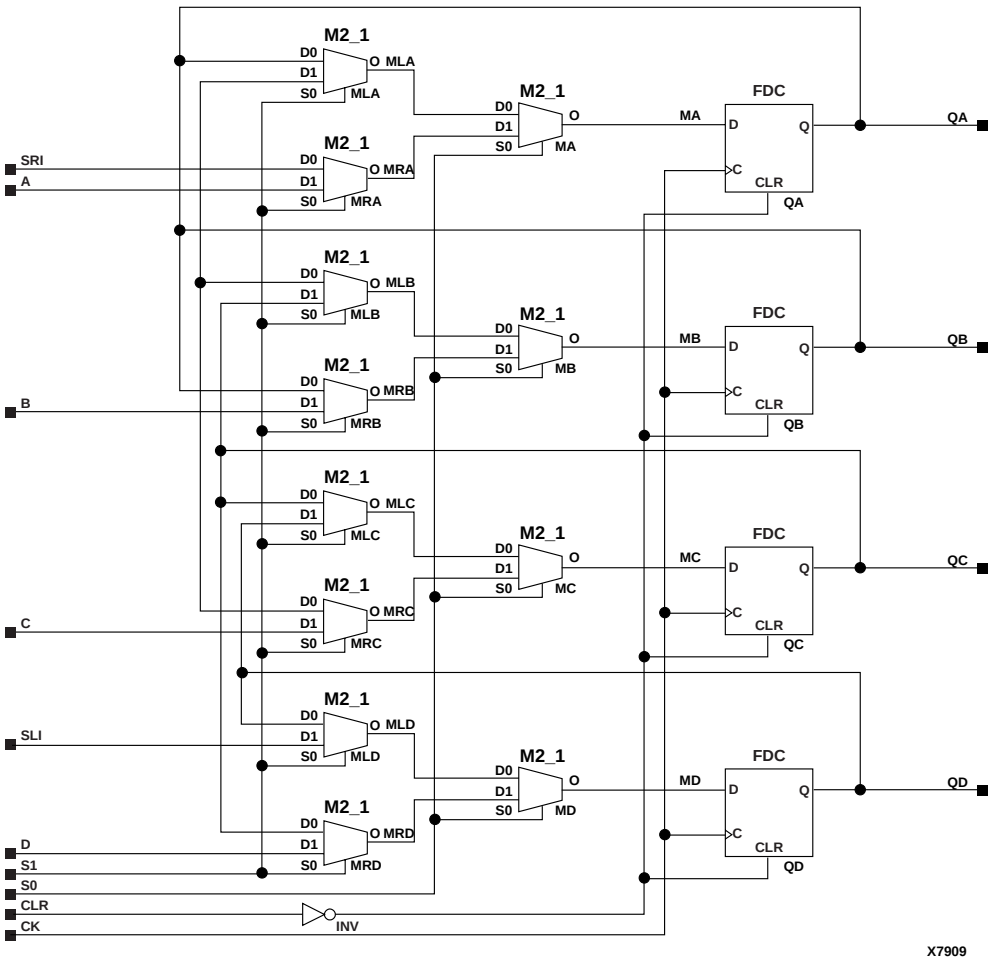
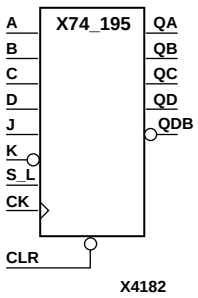


Figure 11-24 X74_194 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_195

4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N/A	N/A	N/A	Macro	Macro	Macro



X74_195 is a 4-bit shift register with shift-right serial inputs (J, active High, and K, active Low), parallel inputs (D – A), parallel outputs (QD – QA) and QDB, shift/load control input (S_L), and active-Low asynchronous clear (CLR). Asynchronous CLR, when Low, overrides all other inputs and resets data outputs QD – QA Low and QDB High. When S_L is Low and CLR is High, data on the D – A inputs is loaded into the corresponding QD – QA bits of the register during the Low-to-High clock (CK) transition. When S_L and CLR are High, the first bit of the register (QA) responds to the J and K inputs during the Low-to-High clock transition, as shown in the truth table. During subsequent Low-to-High clock transitions, with S_L and CLR High, the data is shifted to the next-highest bit position (shift right) as new data is loaded into QA (J, K→QA, QA→QB, QB→QC, and so forth).

Registers can be cascaded by connecting the QD and QDB outputs of one stage to the J and K inputs, respectively, of the next stage and connecting clock, S_L and CLR inputs in parallel.

Inputs						Outputs				
CLR	S_L	J	K	A – D	CK	QA	QB	QC	QD	QDB
0	X	X	X	X	X	0	0	0	0	1
1	0	X	X	A – D	↑	a	b	c	d	d
1	1	0	0	X	↑	0	qa	qb	qc	qc
1	1	1	1	X	↑	1	qa	qb	qc	qc
1	1	0	1	X	↑	qa	qa	qb	qc	qc
1	1	1	0	X	↑	qa	qa	qb	qc	qc

Lowercase letters represent state of referenced input or output one setup time prior to active clock transition

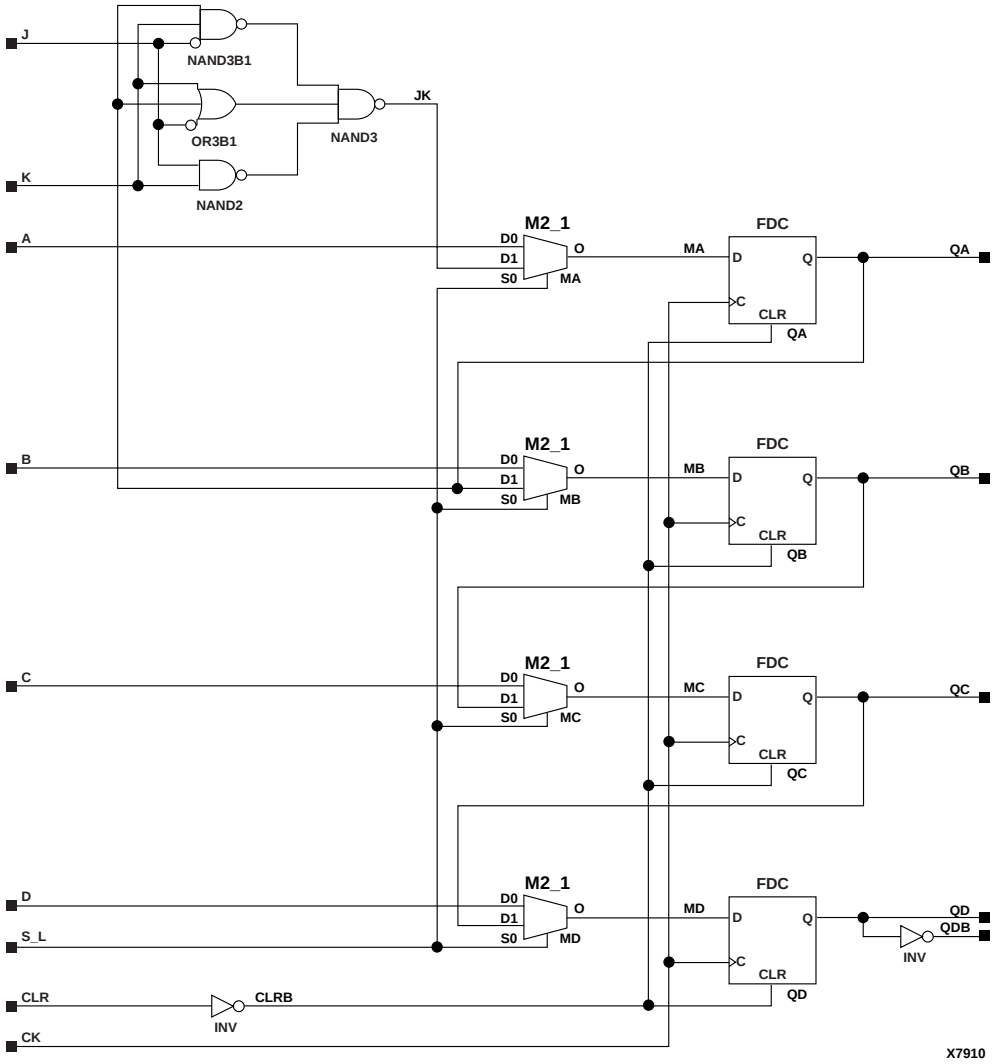
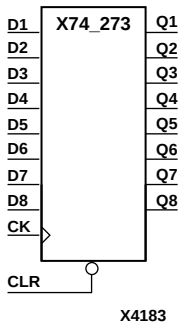


Figure 11-25 X74_195 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_273

8-Bit Data Register with Active-Low Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_273 is an 8-bit data register with active-Low asynchronous clear. The active-Low asynchronous clear (CLR), when Low, overrides all other inputs and resets the data outputs (Q8 – Q1) Low. When CLR is High, the data on the data inputs (D8 – D1) is transferred to the corresponding data outputs (Q8 – Q1) during the Low-to-High clock transition (CK).

Inputs			Outputs
CLR	D8 – D1	CK	Q8 – Q1
0	X	X	0
1	D8 – D1	↑	d8 – d1

dn = state of referenced input one setup time prior to active clock transition

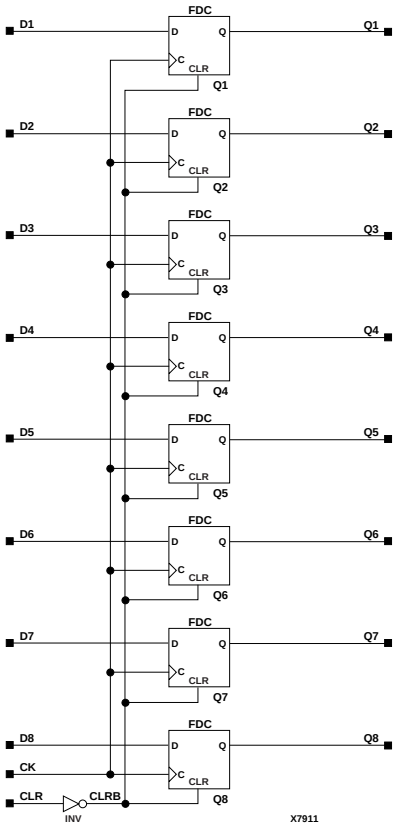
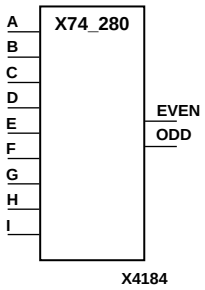


Figure 11-26 X74_273 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_280

9-Bit Odd/Even Parity Generator/Checker

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_280 parity generator / checker compares up to nine data inputs (I – A) and provides both even (EVEN) and odd parity (ODD) outputs. The EVEN output is High when an even number of inputs is High. The ODD output is High when an odd number of inputs is High.

Expansion to larger word sizes is accomplished by tying the ODD outputs of up to nine parallel components to the data inputs of one more X74_280; all other inputs are tied to ground.

Inputs	Outputs	
Number of Ones on A – I	EVEN	ODD
0, 2, 4, 6, or 8	1	0
1, 3, 5, 7, or 9	0	1

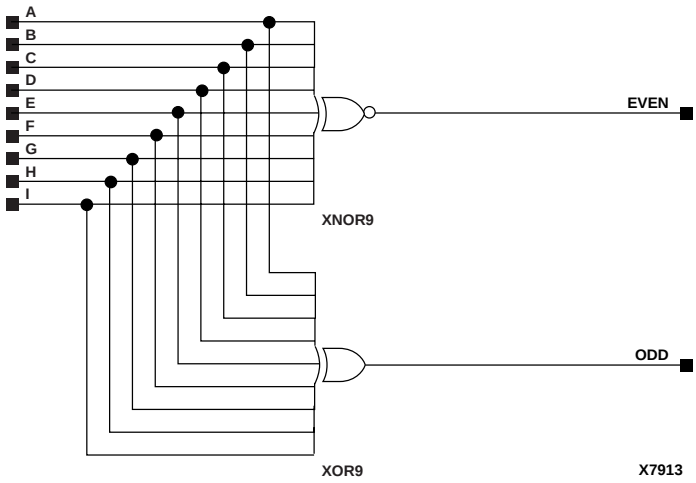
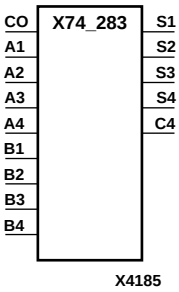


Figure 11-27 X74_280 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_283

4-Bit Full Adder with Carry-In and Carry-Out

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_283, a 4-bit full adder with carry-in and carry-out, adds two 4-bit words (A4 – A1 and B4 – B1) and a carry-in (C0) and produces a binary sum output (S4 – S1) and a carry-out (C4).

```
16(C4)+8(S4)+4(S3)+2(S2)+S1=8(A4+B4)+4(A3+B3)+2(A2+B2)+(A1+B
1)+C0

(where “+” = addition)
```

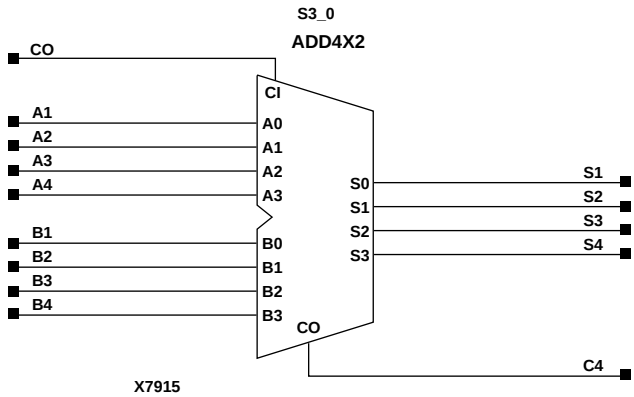
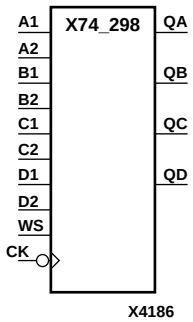


Figure 11-28 X74_283 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_298

Quadruple 2-Input Multiplexer with Storage and Negative-Edge Clock

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_298 selects 4-bits of data from two sources (D1 – A1 or D2 – A2) under the control of a common word select input (WS). When WS is Low, D1 – A1 is chosen, and when WS is High, D2 – A2 is chosen. The selected data is transferred into the output register (QD – QA) during the High-to-Low transition of the negative-edge triggered clock (CK).

Inputs				Outputs
WS	A1 – D1	A2 – D2	CK	QA – QD
0	A1 – D1	X	↓	a1 – d1
1	X	A2 – D2	↓	a2 – d2

an – dn = state of referenced input one setup time prior to active clock transition

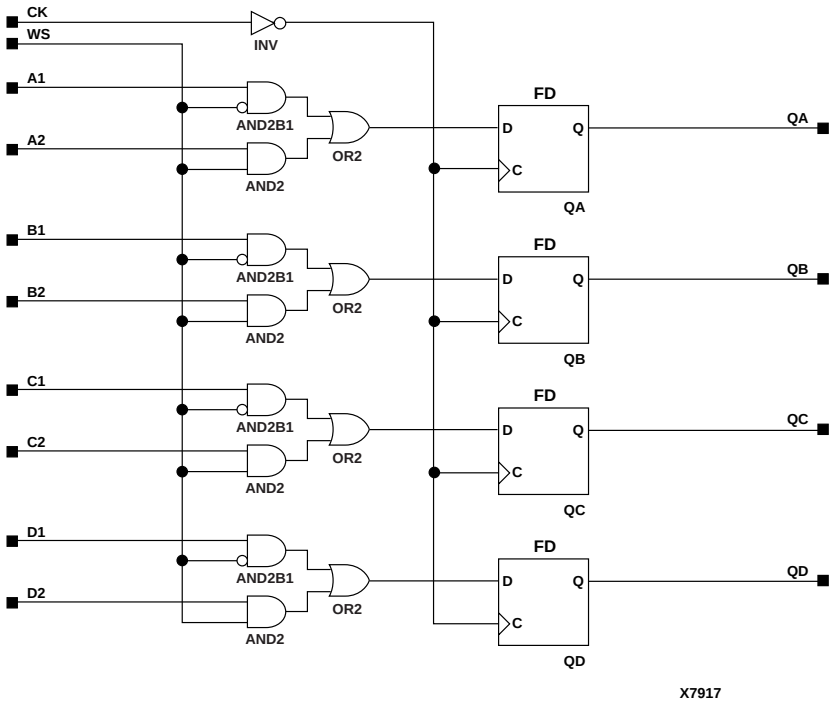
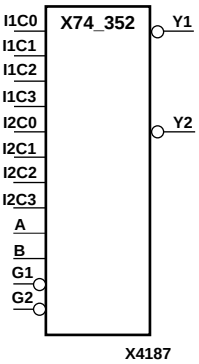


Figure 11-29 X74_298 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_352

Dual 4-to-1 Multiplexer with Active-Low Enables and Outputs

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_352 comprises two 4-to-1 multiplexers with separate enables (G1 and G2) but with common select inputs (A and B). When an active-Low enable (G1 or G2) is Low, the multiplexer chooses one data bit from the four sources associated with the particular enable (I1C3 – I1C0 for G1 and I2C3 – I2C0 for G2) under the control of the common select inputs (A and B). The active-Low outputs (Y1 and Y2) reflect the inverse of the selected data as shown in truth table. Y1 is associated with G1 and Y2 is associated with G2. When an active-Low enable is High, the associated output is High.

Inputs							Outputs
G	B	A	IC0	IC1	IC2	IC3	Y
1	X	X	X	X	X	X	1
0	0	0	IC0	X	X	X	$\overline{IC0}$
0	0	1	X	IC1	X	X	$\overline{IC1}$
0	1	0	X	X	IC2	X	$\overline{IC2}$
0	1	1	X	X	X	IC3	$\overline{IC3}$

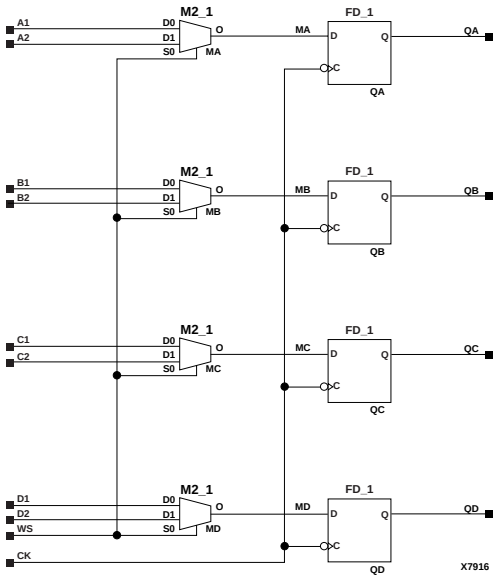
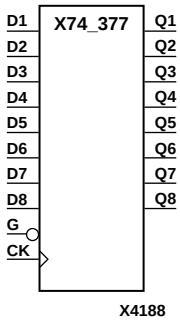


Figure 11-30 X74_352 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_377

8-Bit Data Register with Active-Low Clock Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



When the active-Low clock enable (G) is Low, the data on the eight data inputs (D8 – D1) is transferred to the corresponding data outputs (Q8 – Q1) during the Low-to-High clock (CK) transition. The register ignores clock transitions when G is High.

Inputs			Outputs
G	D8 – D1	CK	Q8 – Q1
1	X	X	No Chg
0	D8 – D1	↑	d8 – d1

dn = state of referenced input one setup time prior to active clock transition

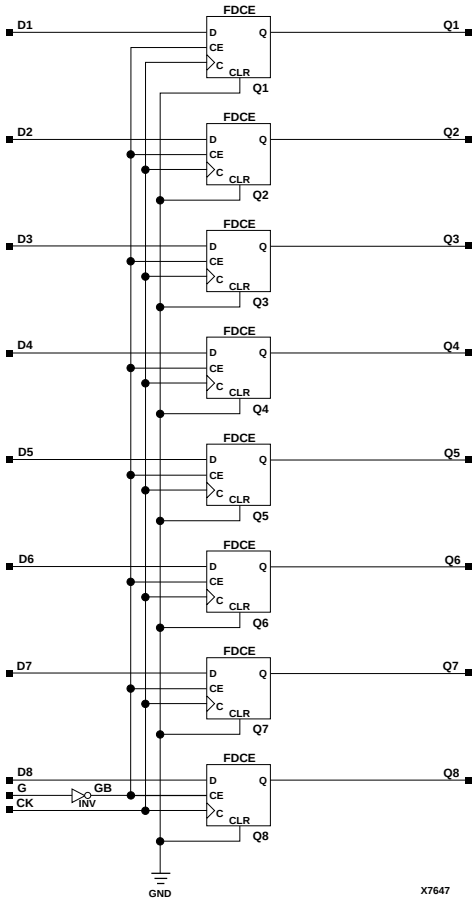
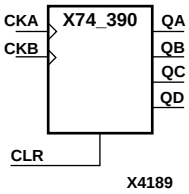


Figure 11-31 X74_377 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_390

4-Bit BCD/Bi-Quinary Ripple Counter with Negative-Edge Clocks and Asynchronous Clear

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_390 is a cascadable, resettable binary-coded decimal (BCD) or bi-quinary counter that can be used to implement cycle lengths equal to whole and / or cumulative multiples of 2 and / or 5. In BCD mode, the output QA is connected to negative-edge clock input (CKB), and data outputs (QD – QA) increment during the High-to-Low clock transition as shown in the truth table, provided asynchronous clear (CLR) is Low. In bi-quinary mode, output QD is connected to the negative-edge clock input (CKA). As shown in the truth table, in bi-quinary mode, QA supplies a divide-by-five output and QB supplies a divide-by-two output, provided asynchronous CLR is Low. When asynchronous CLR is High, the other inputs are overridden, and data outputs (QD – QA) are reset Low.

Larger ripple counters are created by connecting the QD output (BCD mode) or QA output (bi-quinary mode) of the first stage to the appropriate clock input of the next stage and connecting the CLR inputs in parallel.

Count	BCD				Bi-Quinary			
	QD	QC	QB	QA	QD	QC	QB	QA
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	0
2	0	0	1	0	0	1	0	0
3	0	0	1	1	0	1	1	0
4	0	1	0	0	1	0	0	0
5	0	1	0	1	0	0	0	1
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	1	0	1
8	1	0	0	0	0	1	1	1
9	1	0	0	1	1	0	0	1

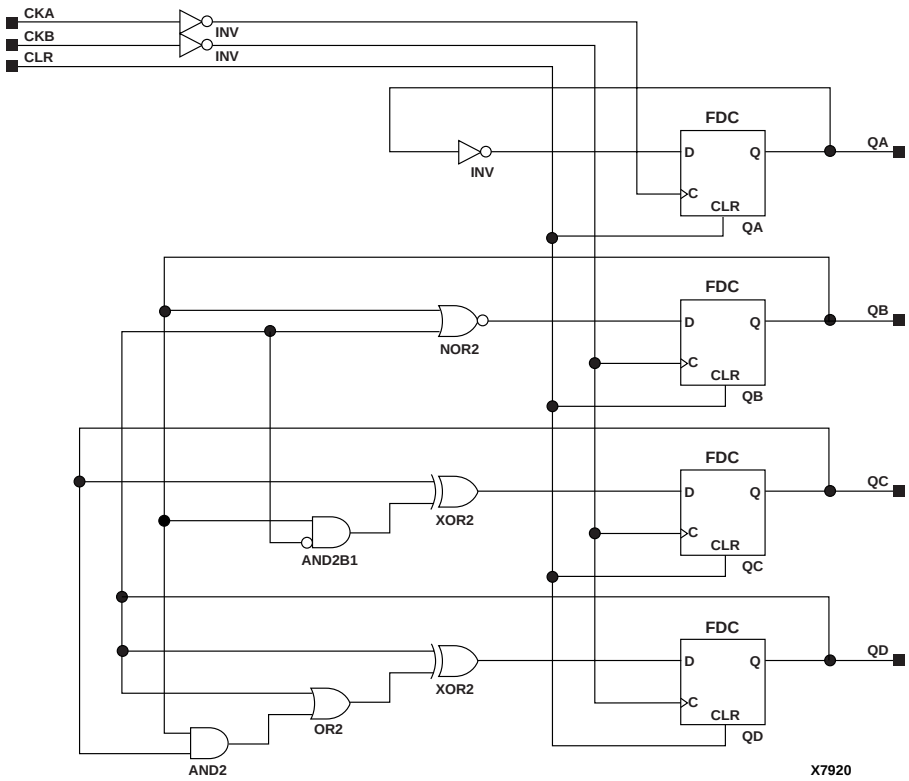
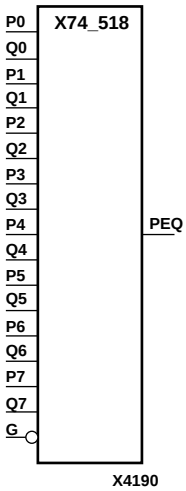


Figure 11-32 X74_390 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_518

8-Bit Identity Comparator with Active-Low Enable

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_518 is an 8-bit identity comparator with 16 data inputs for two 8-bit words (P7 – P0 and Q7 – Q0), data output (PEQ), and active-Low enable (G). When G is High, the PEQ output is Low. When G is Low and the two input words are equal, PEQ is High. Equality is determined by a bit comparison of the two words. When any of the two equivalent bits from the two words are not equal, PEQ is Low.

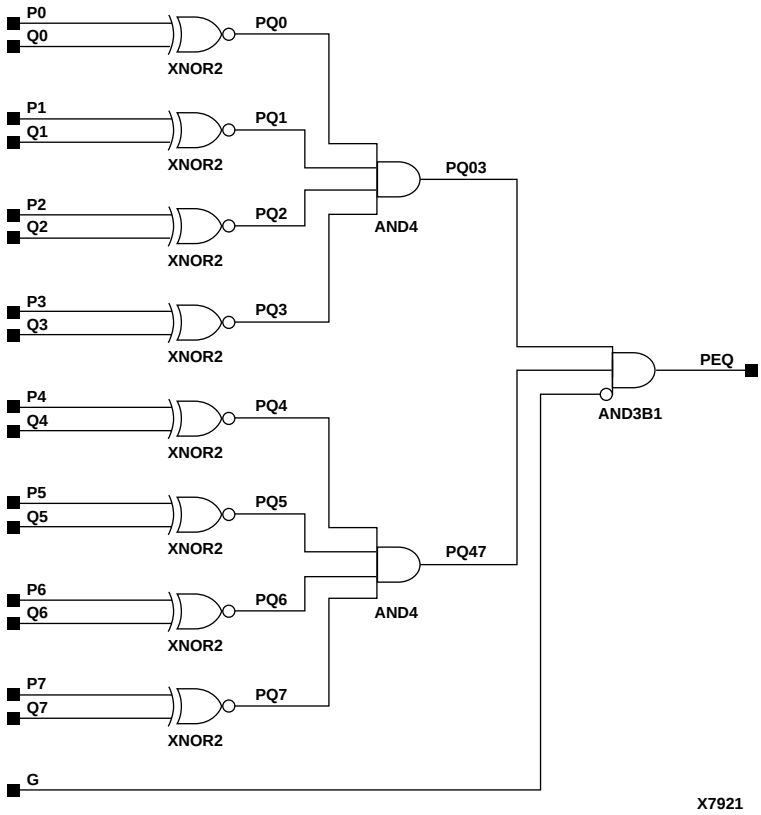
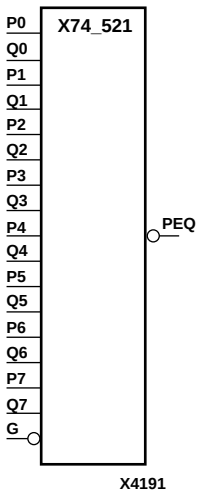


Figure 11-33 X74_518 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II

X74_521

8-Bit Identity Comparator with Active-Low Enable and Output

Spartan-II, Spartan-IIE	Virtex, Virtex-E	Virtex-II, Virtex-II PRO	XC9500/XV/XL	CoolRunner XPLA3	CoolRunner-II
N / A	N / A	N / A	Macro	Macro	Macro



X74_521 is an 8-bit identity comparator with 16 data inputs for two 8-bit words (P7 – P0 and Q7 – Q0), active-Low data output (PEQ), and active-Low enable (G). When G is High, the PEQ output is High. When G is Low and the two input words are equal, PEQ is Low. X74_521 does a bit comparison of the two words to determine equality. When any of the two equivalent bits from the two words are not equal, PEQ is High.

Inputs									Outputs
G	P7, Q7	P6, Q6	P5, Q5	P4, Q4	P3, Q3	P2, Q2	P1, Q1	P0, Q0	PEQ
1	X	X	X	X	X	X	X	X	1
0	P7≠Q7	X	X	X	X	X	X	X	1
0	X	P6≠Q6	X	X	X	X	X	X	1
0	X	X	P5≠Q5	X	X	X	X	X	1
0	X	X	X	P4≠Q4	X	X	X	X	1
0	X	X	X	X	P3≠Q3	X	X	X	1
0	X	X	X	X	X	P2≠Q2	X	X	1
0	X	X	X	X	X	X	P1≠Q1	X	1
0	X	X	X	X	X	X	X	P0≠Q0	1
0	P7=Q7	P6=Q6	P5=Q5	P4=Q4	P3=Q3	P2=Q2	P1=Q1	P0=Q0	0

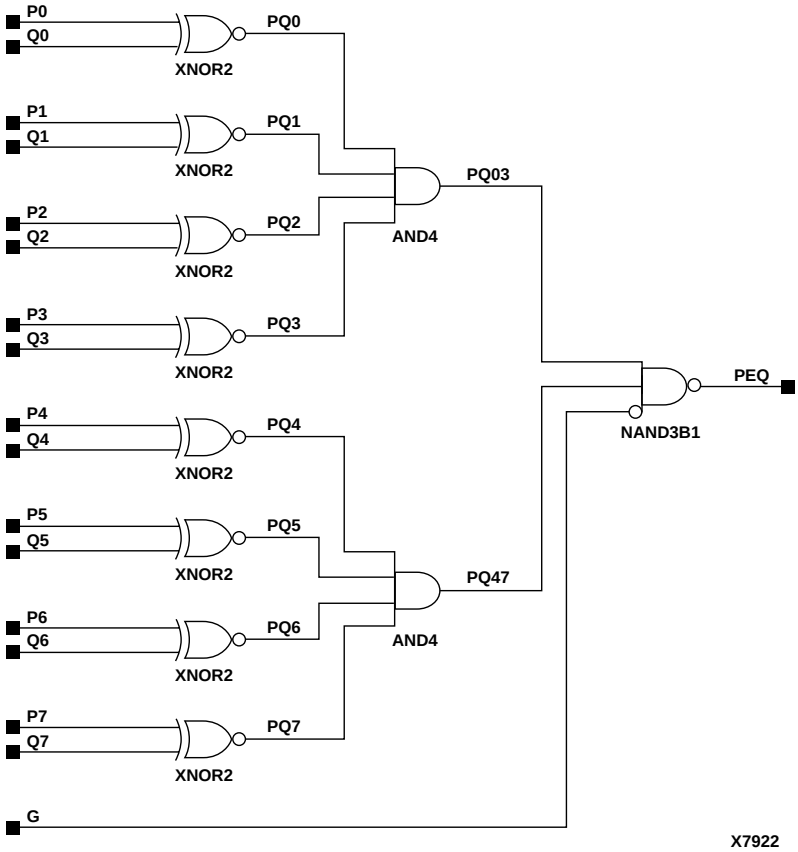


Figure 11-34 X74_521 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II